Harmonic Limiting Standards and Power Factor Correction Techniques

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OUTLINE

- BASICS OF POWER FACTOR CORRECTION
- REVIEW OF HARMONIC STANDARDS
- BASICS OF SINGLE-PHASE PFC TOPOLOGIES AND CONTROL
- CONTROL TECHNIQUES FOR SINGLE-PHASE PFC'S AND COMMERCIAL CONTROL IC'S
- INSULATED TOPOLOGIES
- TECHNIQUES FOR IMPROVING OUTPUT VOLTAGE CONTROL SPEED
- BASICS OF SOFT-SWITCHING TECHNIQUES
- SMALL-SIGNAL MODELING
- SINGLE-PHASE APPLICATION EXAMPLES

POWER FACTOR DEFINITION

Input voltage and current are periodic waveforms with period $\mathbf{T_i}$.

Power factor **PF**:

$$PF \equiv \frac{P}{V_{i,rms} \cdot I_{i,rms}}$$

where **P** is the average power:

$$P = \frac{1}{T_i} \cdot \int_{T_i} v_i \, i_i \, dt$$

and $\mathbf{V_{i,rms}}$ and $\mathbf{I_{i,rms}}$ are :

$$V_{i,\,rms} \equiv \sqrt{\frac{1}{T_i} \int_{T_i} v_i^2 \, dt} \qquad I_{i,\,rms} \equiv \sqrt{\frac{1}{T_i} \int_{T_i} i_i^2 \, dt}$$

POWER FACTOR DEFINITION

Being voltage and current periodic waveforms we can write in Fourier series:

$$v_i = V_0 + \sum_{k=1}^{\infty} \sqrt{2} V_k \sin(k\omega_i + \phi_k)$$

$$i_i = I_0 + \sum_{k=1}^{\infty} \sqrt{2} I_k \sin(k\omega_i + \gamma_k)$$

V_0 , I_0 = average values

V_k , I_k = RMS values of harmonics

The average power is:

$$P = V_0 I_0 + \sum V_k I_k \cos(\phi_k - \gamma_k)$$

CONSEQUENCE:

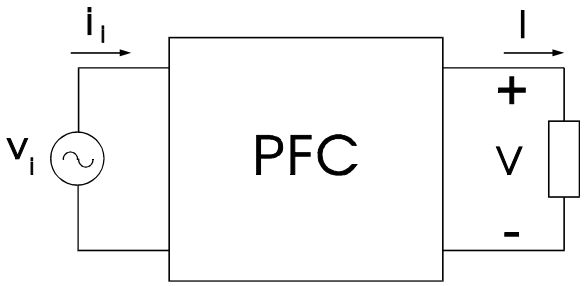
Current harmonic terms contributes to active power only in the presence of voltage harmonic terms of the same frequency.

POWER FACTOR DEFINITION

$0 \leq PF \leq 1$

PF = 1 only if current and voltage are proportional

Power Factor Correction



An ideal Power Factor Corrector (PFC) takes from the supply a current which is proportional to the supply voltage

$$R_{em} = \frac{v_i}{i_i}$$ **emulated resistance**

POWER FACTOR DEFINITION

PARTICULAR CASE: SINUSOIDAL INPUT VOLTAGE

$$PF = \frac{V_1 I_1 \cos(\phi_1)}{V_1 \cdot I_{i,rms}} = \frac{I_1}{I_{i,rms}} \cdot \cos(\phi_1)$$

$$D.F. = \frac{I_1}{I_{i,rms}} = \text{DISTORTION FACTOR}$$

$\cos(\phi_1)$ = DISPLACEMENT FACTOR

$$D.F. = \frac{1}{\sqrt{1 + (THD)^2}}, \qquad THD = \frac{\sqrt{I_{i,rms}^2 - I_1^2}}{I_1}$$

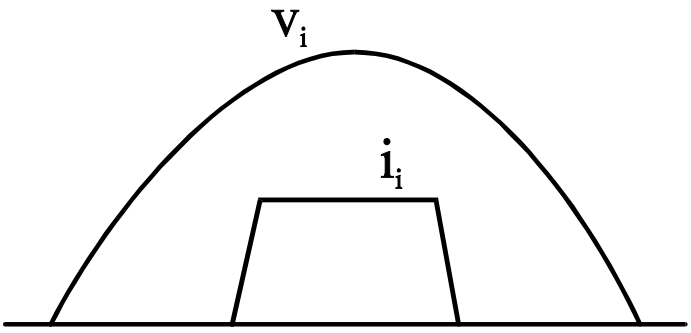
(THD = Total Harmonic Distortion)

POWER FACTOR REQUIREMENTS

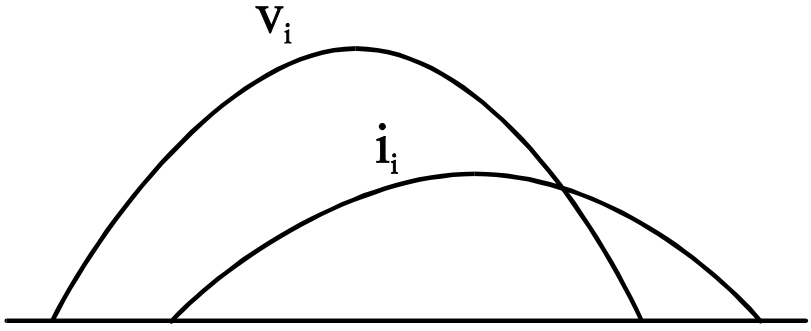
PF = 1 implies*:*

- zero displacement between voltage and current fundamental component ($\phi_1 = 0$)
- zero current harmonic content

EXAMPLES:



$\cos(\phi_1) = 0$, D.F. $\neq 0$



$\cos(\phi_1) \neq 0$, D.F. = 0

In both cases PF<1

WHY POWER FACTOR CORRECTION

- Increased source efficiency
  - lower losses on source impedance
  - lower voltage distortion (cross-coupling)
  - higher power available from a given source

- Reduced low-frequency harmonic pollution

- Compliance with limiting standards (IEC 555-2, IEEE 519 etc.)

BASICS OF ACTIVE POWER FACTOR CORRECTION

POWER FACTOR CORRECTION TECHNIQUES

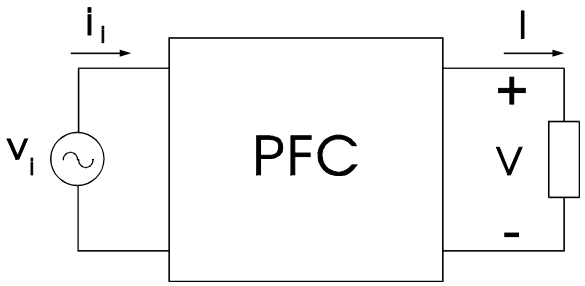
PASSIVE METHODS: LC filters

- power factor not very high
- bulky components
- high reliability
- suitable for very small or high power levels

ACTIVE METHODS: high-frequency converters

- high power factor (approaching unity)
- possibility to introduce a high-frequency insulating transformer
- layout dependent high-frequency harmonics generation (EMI problems)
- suitable for small and medium power levels

ACTIVE POWER FACTOR CORRECTION



DEFINITION:

Power Factor Corrector (PFC):
AC/DC converter with sinusoidal current absorption
(Current Proportional To Supply Voltage)

$$v_i = V_i \operatorname{sen}(\vartheta)$$

$$i_i = I_i \operatorname{sen}(\vartheta), \vartheta = \omega_i t$$

The converter behaves like an equivalent resistance R_{em} given by:

$$R_{em} = \frac{V_i}{I_i}$$

ACTIVE POWER FACTOR CORRECTION: BASIC CONSIDERATIONS

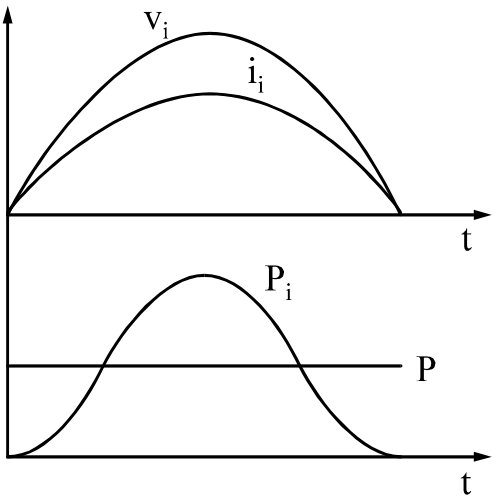
Input power:

$$p_i(\vartheta) = v_i(\vartheta) \cdot i_i(\vartheta) = 2 \cdot V_{i,rms} I_{i,rms} \sin^2(\vartheta) =$$
$$= V_{i,rms} I_{i,rms} (1 - \cos(2\vartheta))$$

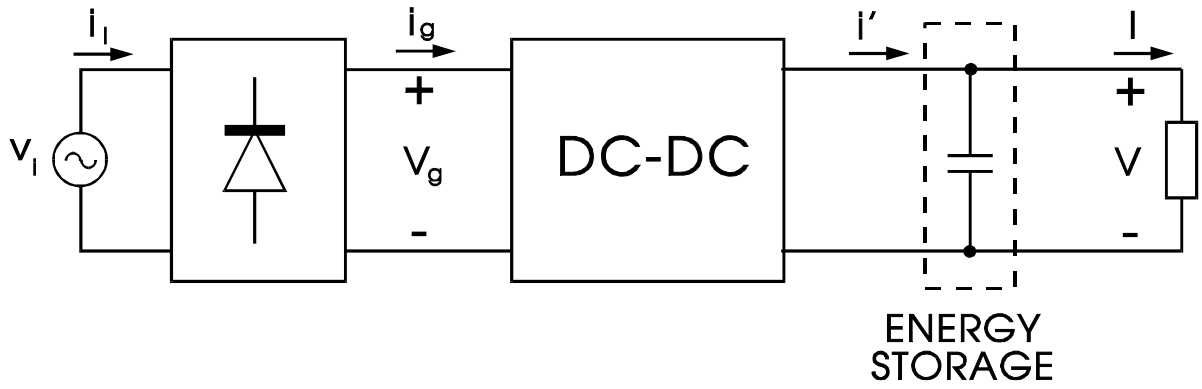
Considering unity efficiency:

$$V_{i,rms} \cdot I_{i,rms} = P = V \cdot I$$

P = output power



PFC WITH CAPACITIVE FILTER



ASSUMPTIONS:

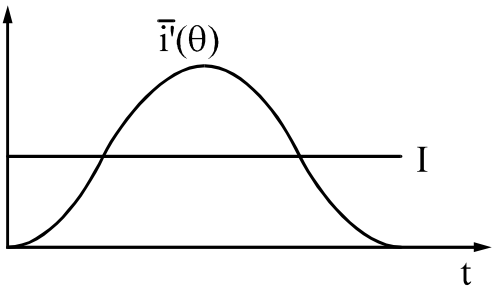
- constant output voltage
- unity efficiency
- no low-frequency pulsating energy stored in the dc/dc stage

$$\Rightarrow \quad p_i(\vartheta) = V \cdot \bar{i}'(\vartheta)$$

PFC WITH CAPACITIVE FILTER

$$\bar{i}'(\vartheta) = \frac{p_i(\vartheta)}{V} = 2I\sin^2(\vartheta)$$

$\bar{i}'(\vartheta)$ = average value of $i'(\vartheta)$ in a switching period



Voltage conversion ratio M':

$$M'(\vartheta) = \frac{V}{v_g(\vartheta)} = \frac{\bar{i}_g(\vartheta)}{\bar{i}'(\vartheta)}$$

Load seen by the dc/dc stage:

$$R'(\vartheta) = \frac{V}{\bar{i}'(\vartheta)} = M'(\vartheta)^2 \cdot \frac{v_g(\vartheta)}{\bar{i}_g(\vartheta)} = M'(\vartheta)^2 \cdot R_{em}$$

PFC WITH CAPACITIVE FILTER

$$R'(\vartheta) = \frac{R}{2 \cdot \sin^2(\vartheta)}$$

$$M'(\vartheta) = \frac{M}{|\sin(\vartheta)|}, M = \frac{V}{V_g}$$

For a PFC we have:

$$\frac{R'(\vartheta)}{M'^2(\vartheta)} = R_{em}$$

a dc/dc converter when used as rectifier operates as a PFC with constant control if : $M'(\vartheta) \propto \sqrt{R'(\vartheta)}$

PFC WITH CAPACITIVE FILTER

OUTPUT FILTER DESIGN

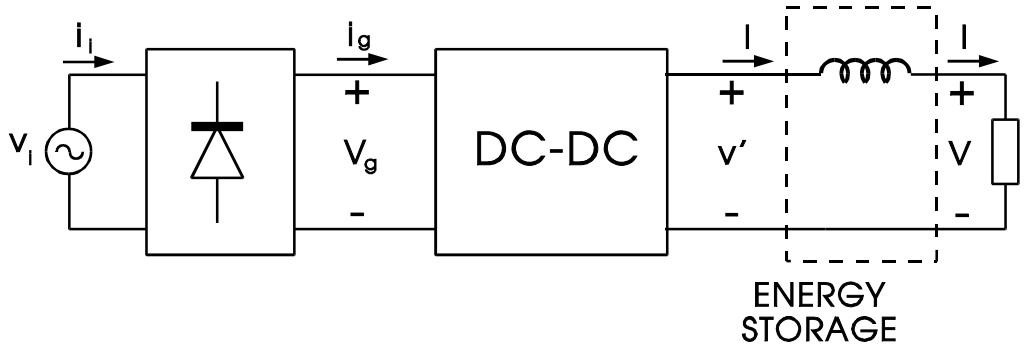
Output filter capacitor current:

$$i_c(\vartheta) = \bar{i}'(\vartheta) - I = -I \cdot \cos(2\vartheta)$$

If ΔV is the desired peak-to-peak output voltage ripple, then:

$$C \geq \frac{I}{\omega_i \, \Delta V}$$

PFC WITH INDUCTIVE FILTER



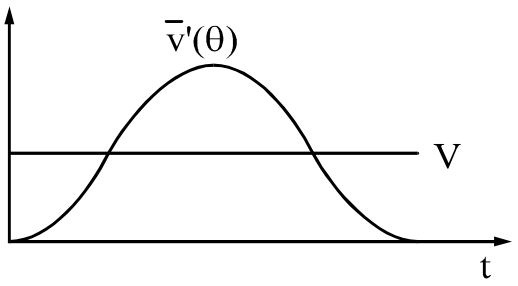
ASSUMPTIONS:

- o constant output current
- o unity efficiency
- o no low-frequency pulsating energy stored in the dc/dc stage

$$\overline{v}'(\vartheta) = \frac{p_i(\vartheta)}{I} = 2V\sin^2(\vartheta)$$

$\overline{v}'(\vartheta)$ = average value of $v'(\vartheta)$ in a switching period

PFC WITH INDUCTIVE FILTER



Voltage conversion ratio M':

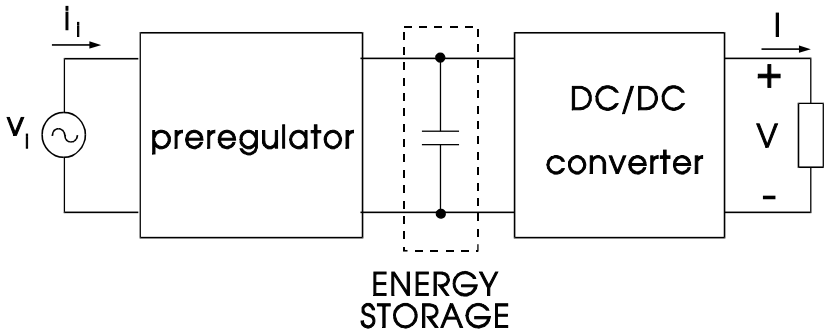
$$M'(\vartheta) = \frac{\overline{v}'(\vartheta)}{v_g(\vartheta)} = \frac{\overline{i}_g(\vartheta)}{I} = 2M\left|\sin(\vartheta)\right|$$

Load seen by the dc/dc stage:

$$R'(\vartheta) = \frac{\overline{v}'(\vartheta)}{I} = 2R\sin^2(\vartheta)$$

POWER FACTOR CORRECTORS: STANDARD CONFIGURATION

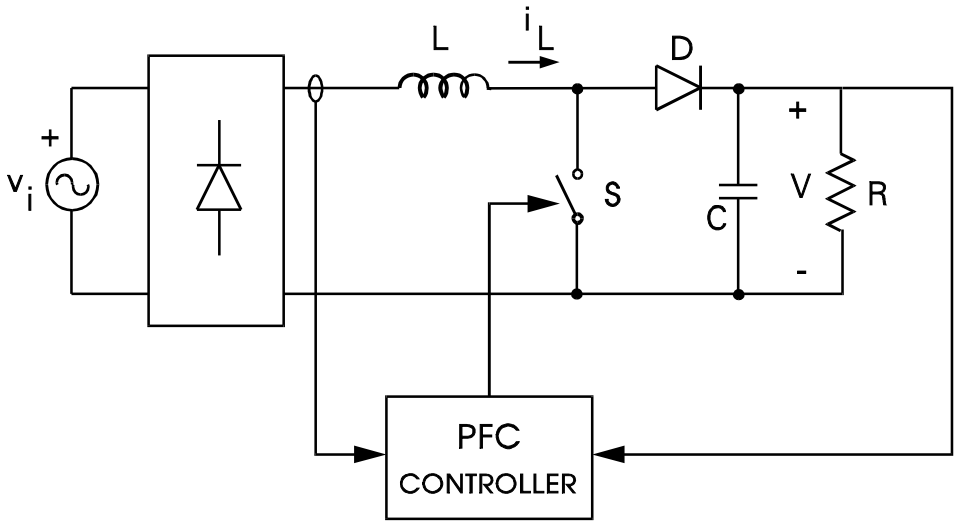
TWO STAGE PFC: CASCADE CONNECTION



PREREGULATORS: AC/DC converters with high power factor and poor output voltage regulation

LOW EFFICIENCY: THE SAME POWER IS PROCESSED TWICE

BASIC PREREGULATORS: BOOST TOPOLOGY



CHARACTERISTICS:

- Inherent input filter (low input current harmonic content)
- Simple topology
- high power factor
- Output voltage greater than peak input voltage
- no start-up or short circuit protection
- no high-frequency insulation

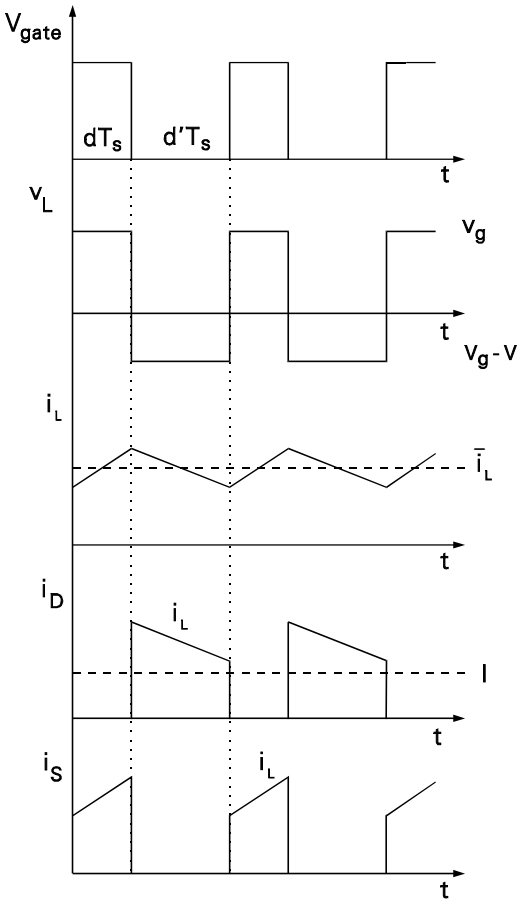
BASIC PREREGULATORS: BOOST TOPOLOGY

CCM OPERATION

Assumption:

switching frequency much greater than line frequency (quasi-stationary approach).

Main waveforms in a switching period



BASIC PREREGULATORS: BOOST TOPOLOGY

OPERATION AS DC/DC CONVERTER

Voltage conversion ratio : $M = \frac{1}{1-d}$

d = duty-cycle

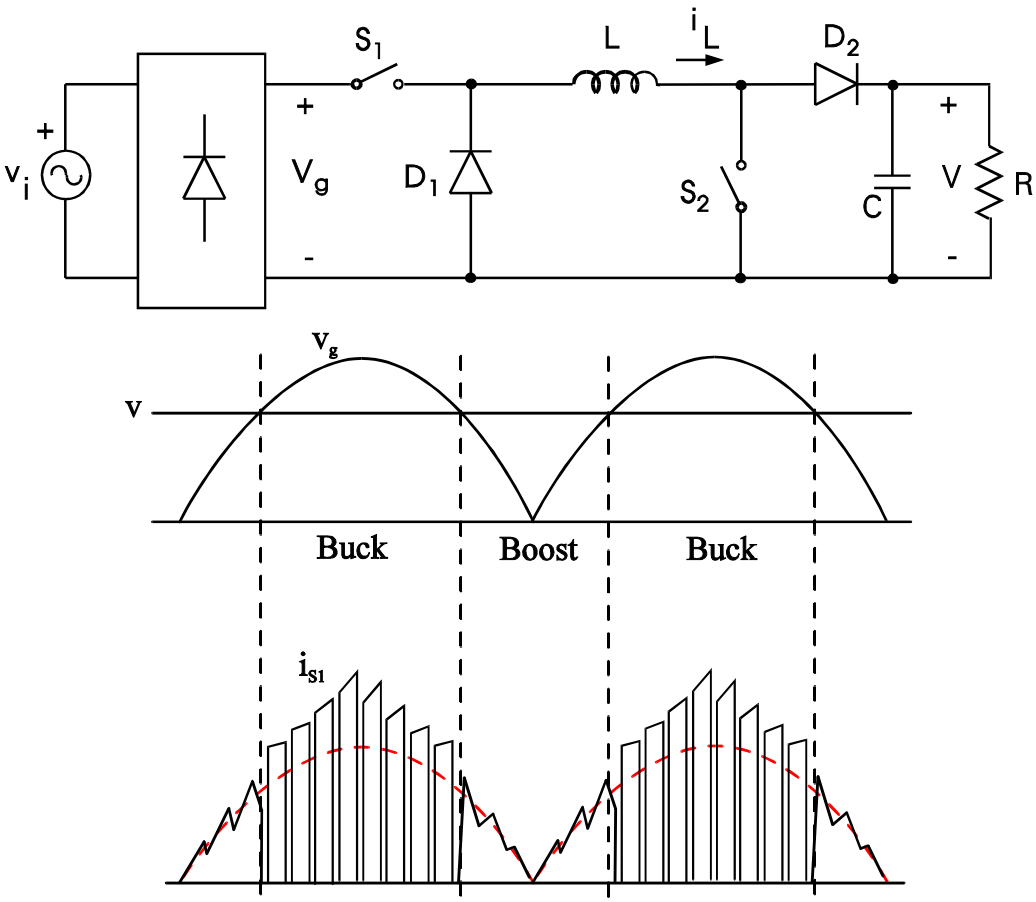
OPERATION AS AC/DC CONVERTER

In order to draw a sinusoidal current the duty-cycle must be modulated during the line period:

$$d(\vartheta) = 1 - \frac{V_g \left|\sin(\vartheta)\right|}{V}$$

(This is an approximation because CCM operation cannot be maintained during the whole line period)

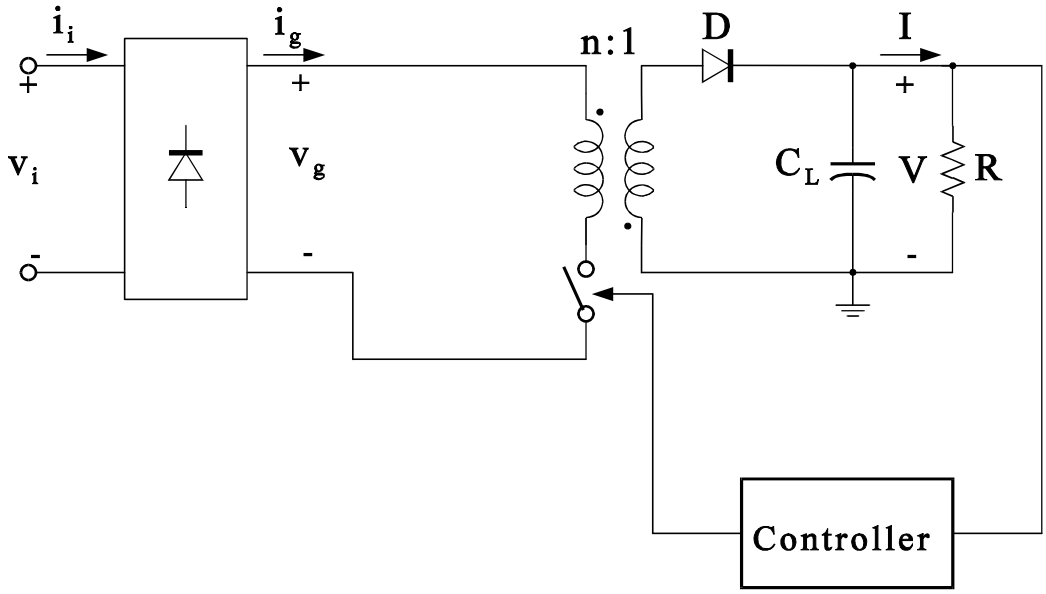
BASIC PREREGULATORS: BUCK + BOOST TOPOLOGY



CHARACTERISTICS:

- o S_1 and D_1 provide start-up and short circuit protection
- o buck-mode operation for v_g higher than output voltage and boost mode-operation for v_g lower than output voltage
- o high conduction losses (four semiconductors in series)

BASIC PREREGULATORS: FLYBACK TOPOLOGY



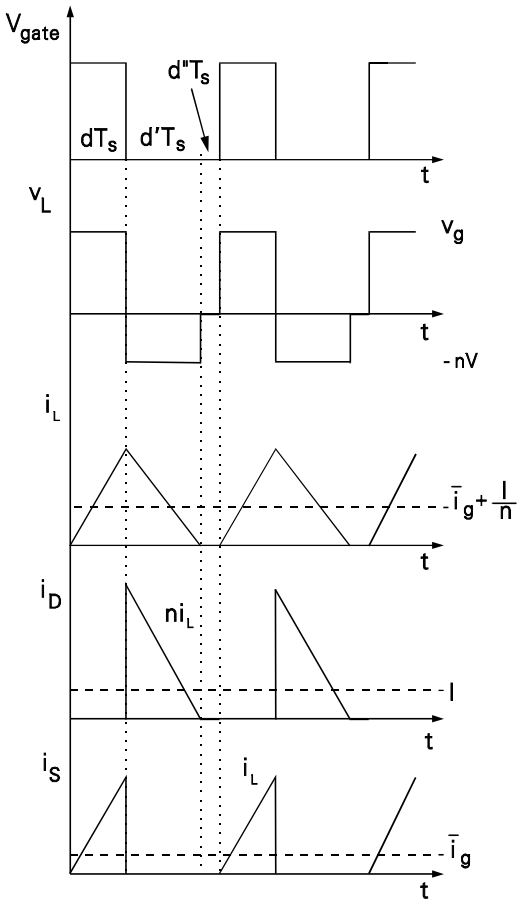
CHARACTERISTICS:

- Simple topology
- high power factor with constant duty-cycle in Discontinuous Conduction Mode (DCM) operation
- inherent start-up and short circuit protection
- high-frequency insulation transformer
- high input current harmonic content

BASIC PREREGULATORS: FLYBACK TOPOLOGY

DCM OPERATION

Main waveforms in a switching period



BASIC PREREGULATORS: FLYBACK TOPOLOGY

DCM OPERATION

OPERATION AS DC/DC CONVERTER

Voltage conversion ratio : $M = \frac{d}{\sqrt{k}}, \qquad k = \frac{2L}{RT_s}$

d = duty-cycle

L = transformer magnetizing inductance (primary side)

R = load resistance

T_S = switching period

$M \propto \sqrt{R} \quad \Rightarrow$ automatic PFC when used as rectifier

OPERATION AS AC/DC CONVERTER

Average input current:

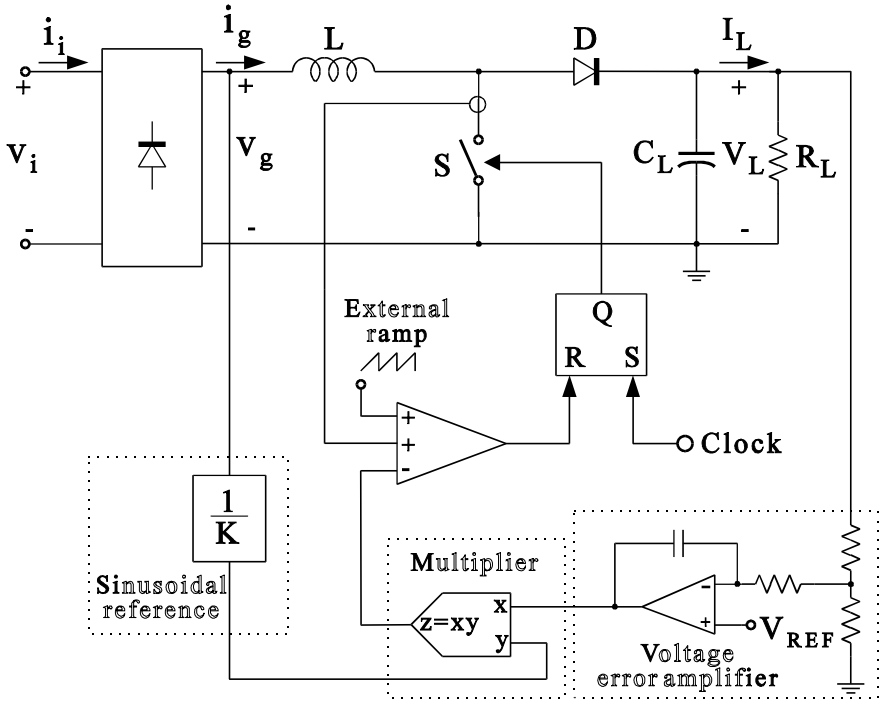
$$\bar{i}_g(\vartheta) = \frac{v_g(\vartheta)}{L} \cdot d^2 T_s$$

At constant duty-cycle and switching frequency the input current is sinusoidal

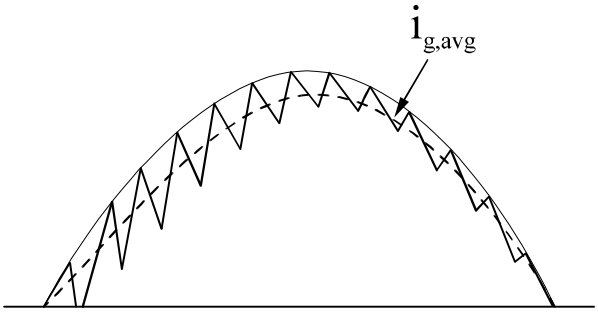
CONTROL TECHNIQUES FOR SINGLE-PHASE PFC'S AND COMMERCIAL CONTROL IC'S

BOOST PREREGULATOR

PEAK CURRENT CONTROL



Input current waveform



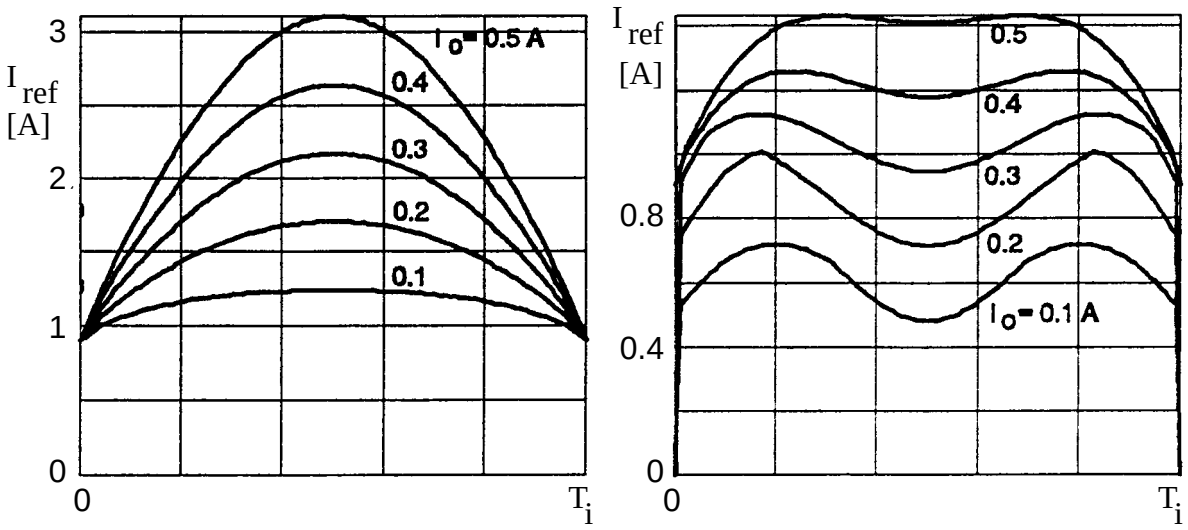
PEAK CURRENT CONTROL

CHARACTERISTICS:

- CONSTANT SWITCHING FREQUENCY
- CONTINUOUS CONDUCTION MODE (CCM) OPERATION
  - low device current stresses
  - low RMS current
  - small EMI filter
- POSSIBILITY TO SENSE ONLY SWITCH CURRENT
  - efficiency improvement
  - possibility to implement a pulse-by-pulse current limit
- SUBHARMONIC OSCILLATIONS (for duty-cycle > 50%)
- LINE CURRENT DISTORTION (increases for high line voltages, light load and high amplitude of compensating ramp)
- COMMUTATION NOISE SENSITIVITY
- HARD REVERSE RECOVERY OF FREEWHEELING DIODE (increased commutation losses and EMI)

PEAK CURRENT CONTROL

IDEAL REFERENCE CURRENT WAVEFORMS



V_i=115V_{rms} V_i=230V_{rms}

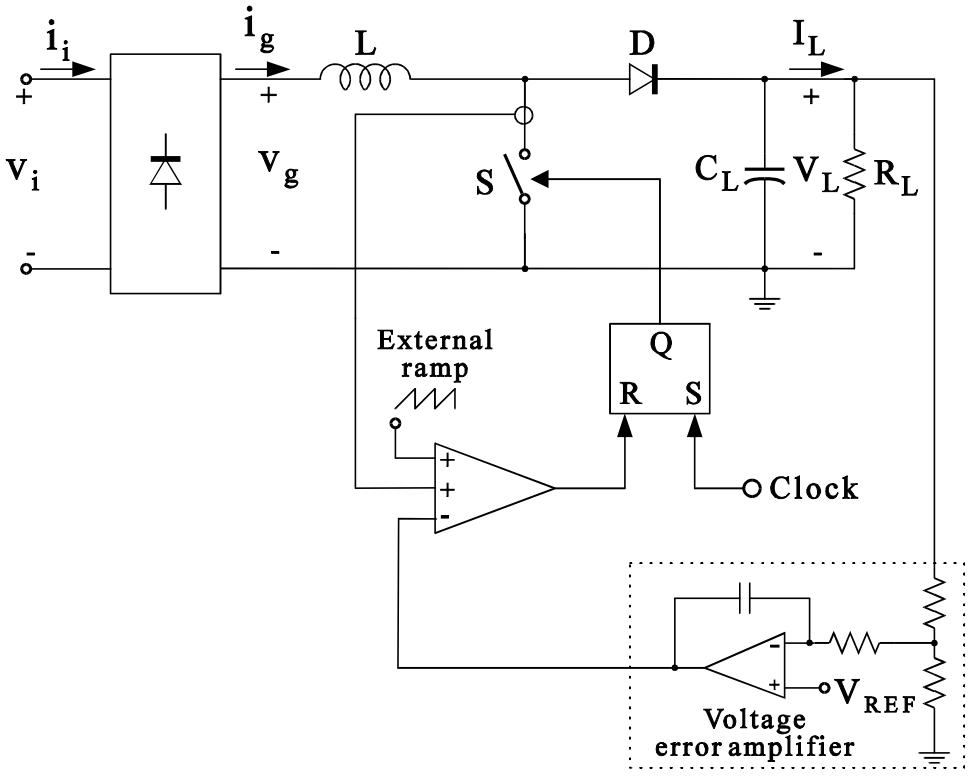
DISTORTION REDUCTION TECHNIQUES

- ADDING A DC OFFSET TO CURRENT REFERENCE

  (function of both line voltage and load current)

- PROGRAMMED DISTORTION CURRENT REFERENCE
  - line dependent DC offset
  - constant offset plus soft clamp

CURRENT CLAMPING CONTROL

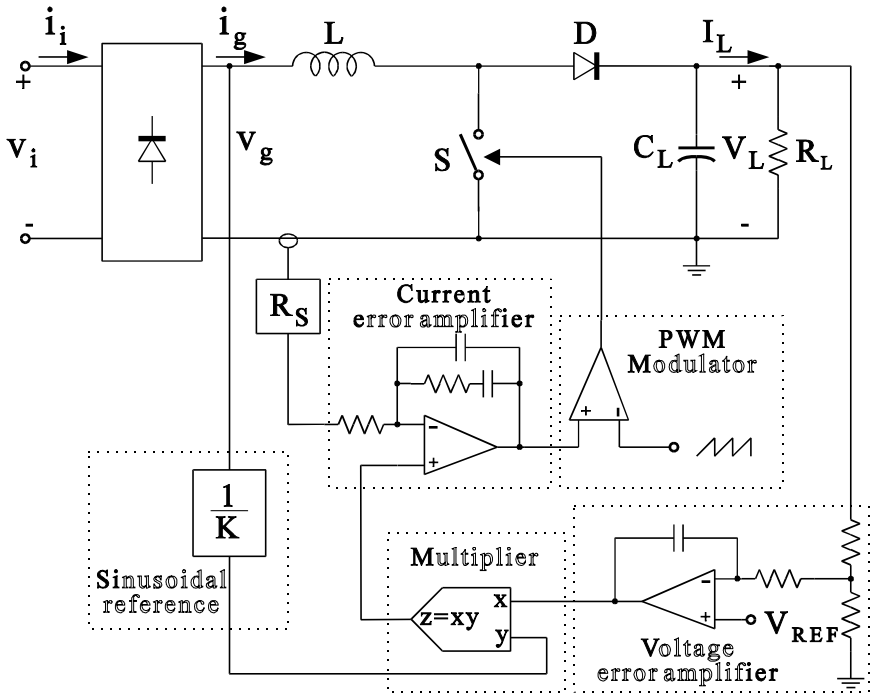


CHARACTERISTICS:

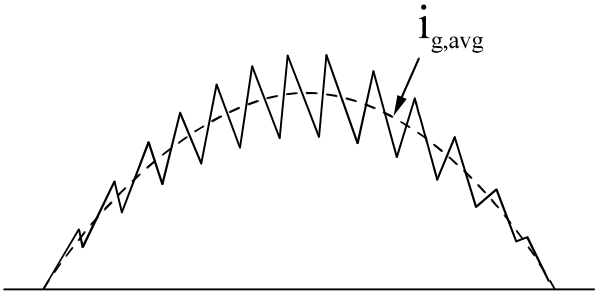
- VERY SIMPLE CONTROL STRUCTURE
- LINE CURRENT DISTORTION BELOW 10% FOR LIMITED LOAD AND LINE VARIATIONS
- UNIVERSAL INPUT VOLTAGE OPERATION CANNOT BE EASILY ACCOMPLISHED

BOOST PREREGULATOR

AVERAGE CURRENT CONTROL



Input current waveform



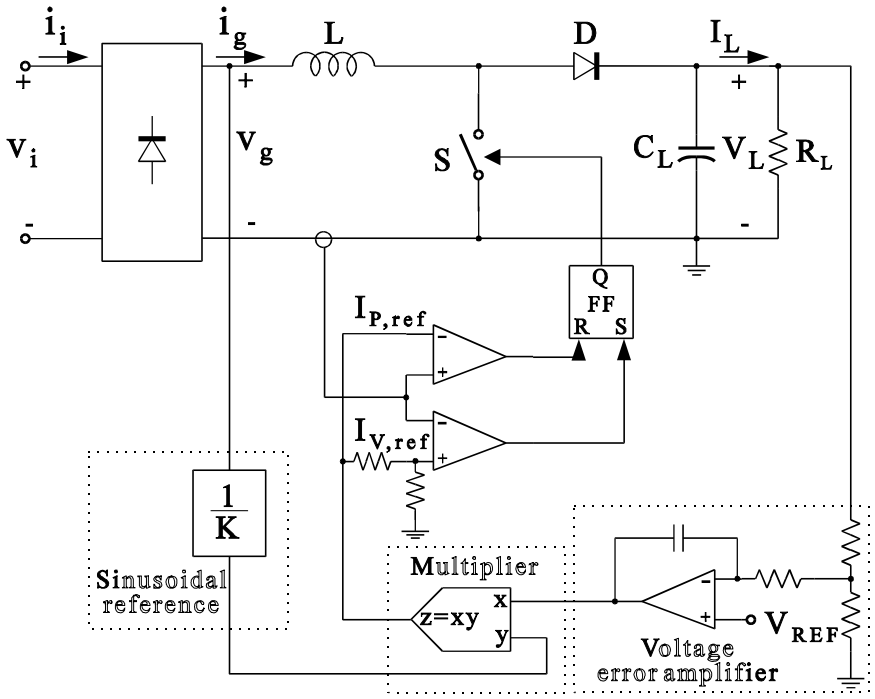
AVERAGE CURRENT CONTROL

CHARACTERISTICS:

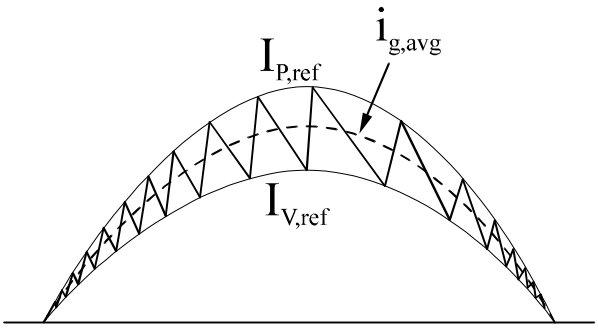
- CONSTANT SWITCHING FREQUENCY
- CONTINUOUS CONDUCTION MODE (CCM) OPERATION
  - low device current stresses
  - low RMS current
  - small EMI filter
- COMPLEX CONTROL SCHEME
  - need of inductor current sensing
  - need of a multiplier
- COMMUTATION NOISE IMMUNITY
- HARD REVERSE RECOVERY OF FREEWHEELING DIODE (increased commutation losses and EMI)
- SEVERAL CONTROL IC's AVAILABLE

BOOST PREREGULATOR

HYSTERETIC CURRENT CONTROL



Input current waveform



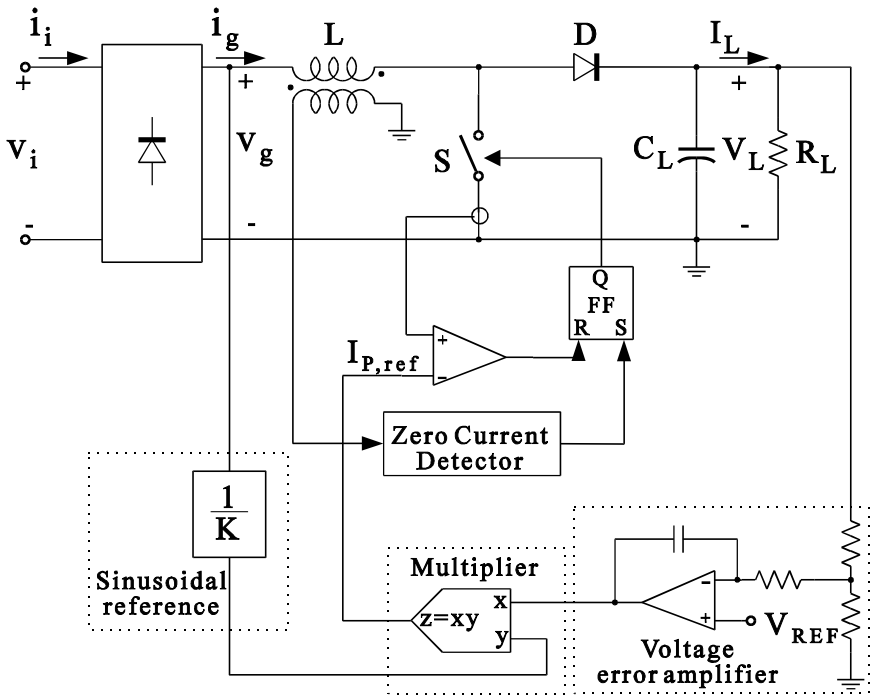
HYSTERETIC CURRENT CONTROL

CHARACTERISTICS:

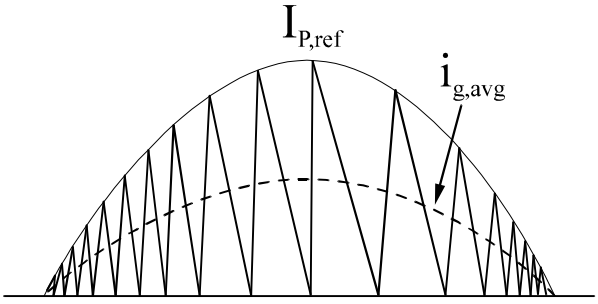
- WIDE SWITCHING FREQUENCY VARIATION
- CONTINUOUS CONDUCTION MODE (CCM) OPERATION
  - low device current stresses
  - low RMS current
  - small EMI filter
- COMPLEX CONTROL SCHEME
  - need of inductor current sensing
  - need of a multiplier
- COMMUTATION NOISE SENSITIVITY
- HARD REVERSE RECOVERY OF FREEWHEELING DIODE (increased commutation losses and EMI)
- SMALL INPUT CURRENT DISTORTION NEAR ZERO CROSSING OF LINE VOLTAGE TO AVOID HIGH SWITCHING FREQUENCY

BOOST PREREGULATOR

BORDERLINE CONTROL
(Operation at the boundary between DCM and CCM)



Input current waveform



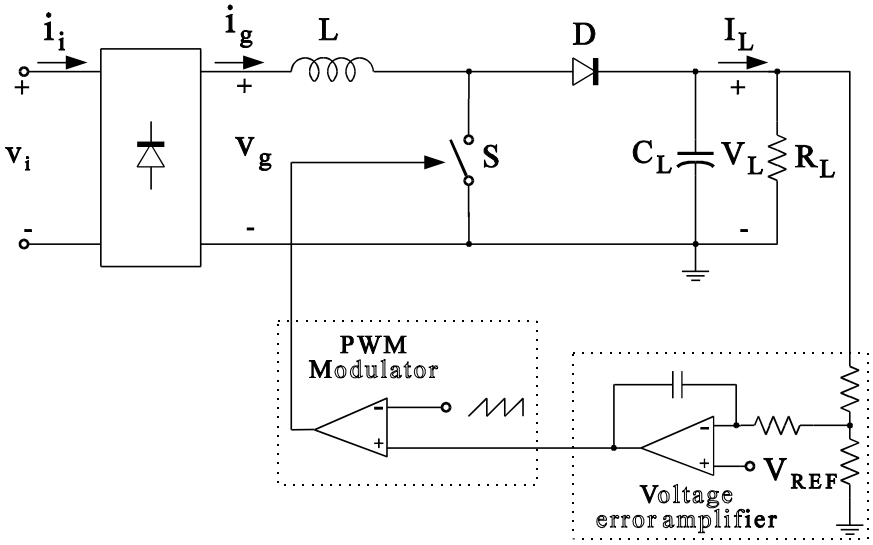
BORDERLINE CONTROL

CHARACTERISTICS:

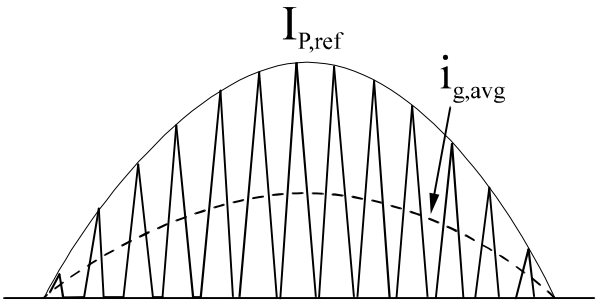
- AUTOMATIC PFC (CONSTANT SWITCH ON TIME)
- VARIABLE SWITCHING FREQUENCY (function of load current and instantaneous line voltage)
- DISCONTINUOUS CONDUCTION MODE (DCM) OPERATION
  - high device current stresses
  - high RMS current
  - large EMI filter
  - reduced switch turn on losses and increased turn off losses
- SIMPLE CONTROL SCHEME
  - no need for a multiplier (however some IC's make use of it)
  - need for sensing the instant of inductor current zeroing
- SOFT RECOVERY OF FREEWHEELING DIODE

BOOST PREREGULATOR

DISCONTINUOUS CURRENT PWM CONTROL



Input current waveform



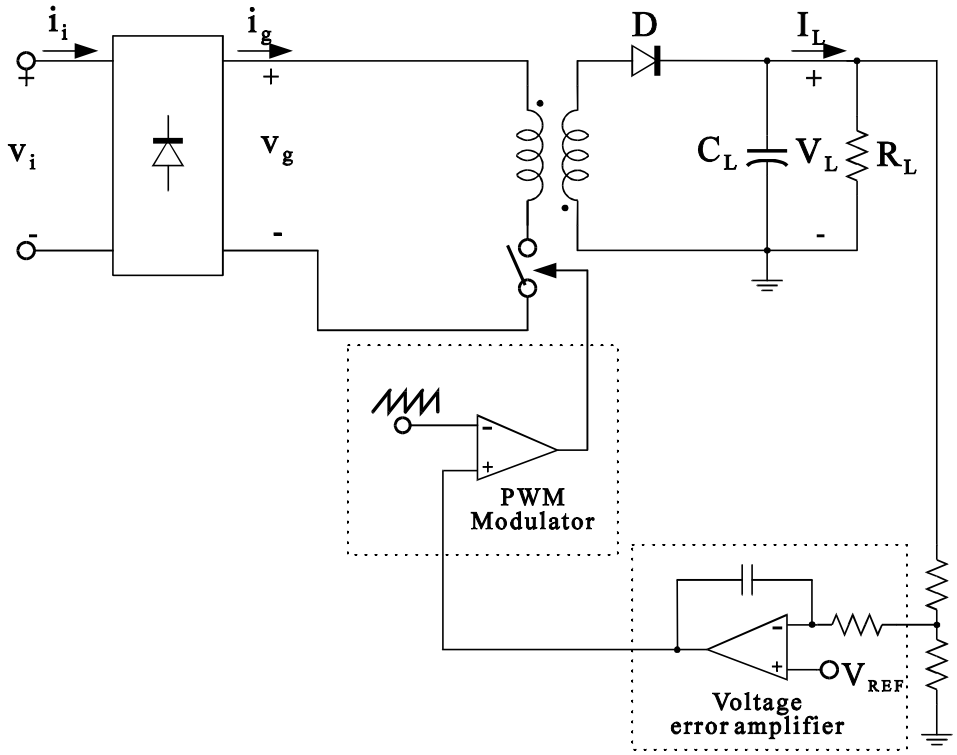
DISCONTINUOUS CURRENT PWM CONTROL

CHARACTERISTICS:

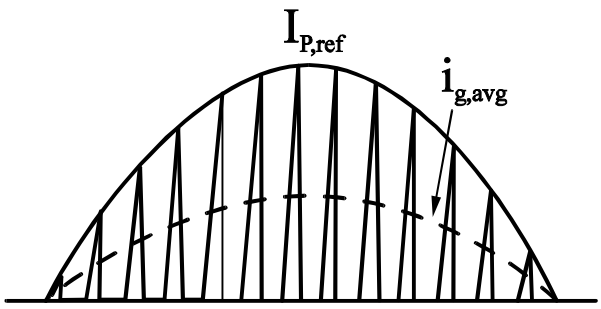
- CONSTANT SWITCHING FREQUENCY
- DISCONTINUOUS CONDUCTION MODE (DCM) OPERATION
  - high device current stresses
  - high RMS current
  - large EMI filter
  - reduced switch turn on losses and increased turn off losses
- NO NEED OF CURRENT SENSING
- SIMPLE PWM CONTROL
- INPUT CURRENT DISTORTION (WITH BOOST CONVERTER)
  - distortion can be reduced by subtracting a fraction of rectified line voltage from the error voltage or by modulating the clock frequency with rectified line voltage
- SOFT RECOVERY OF FREEWHEELING DIODE

FLYBACK PREREGULATOR

DCM OPERATION



Input current waveform



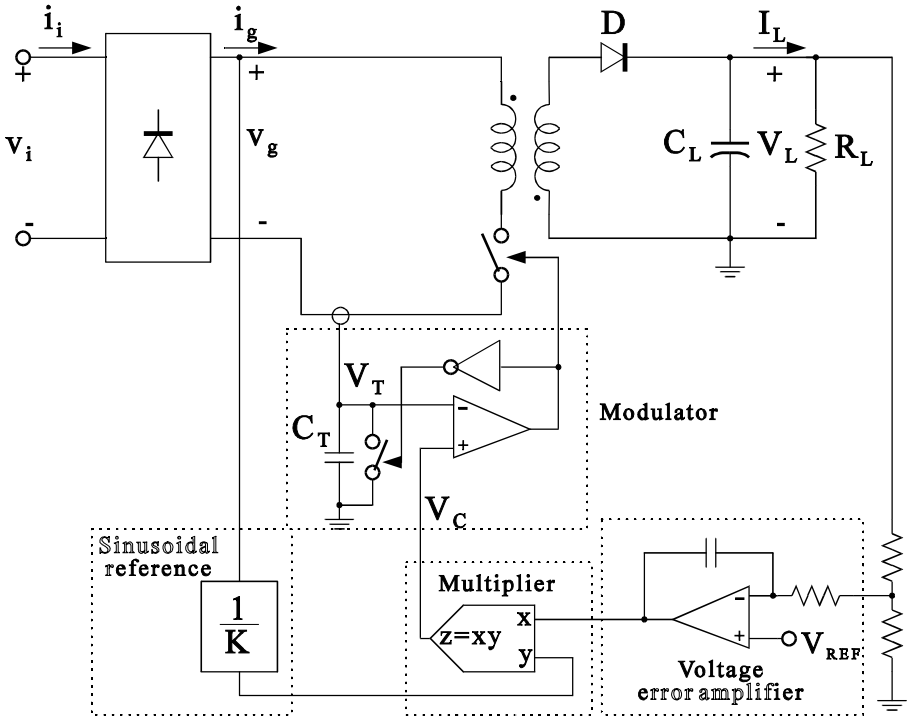
DCM OPERATION

CHARACTERISTICS:

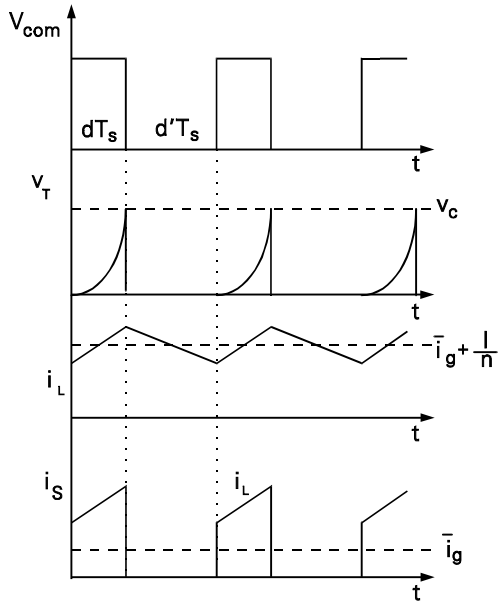
- AUTOMATIC PFC (CONSTANT SWITCH ON TIME)
- CONSTANT SWITCHING FREQUENCY
- DCM OPERATION
  - high device current stresses
  - high RMS current
  - large EMI filter
  - reduced switch turn on losses and increased turn off losses
- NO NEED OF CURRENT SENSING
- SIMPLE PWM CONTROL
- SOFT OF RECOVERY OF FREEWHEELING DIODE

FLYBACK PREREGULATOR

CCM OPERATION - CHARGE CONTROL



Main waveforms



CCM OPERATION - CHARGE CONTROL

CHARACTERISTICS:

- CONSTANT SWITCHING FREQUENCY
- CONTINUOUS CONDUCTION MODE (CCM) OPERATION
  - low device current stresses
  - low RMS current
  - relatively large EMI filter (current ripple is small, but input current is discontinuous)
- SUBHARMONIC OSCILLATIONS (for duty-cycle > 50%)
- COMPLEX CONTROL SCHEME
  - need of inductor current sensing
  - need of a multiplier
- COMMUTATION NOISE IMMUNITY
- HARD REVERSE RECOVERY OF FREEWHEELING DIODE (increased commutation losses and EMI)

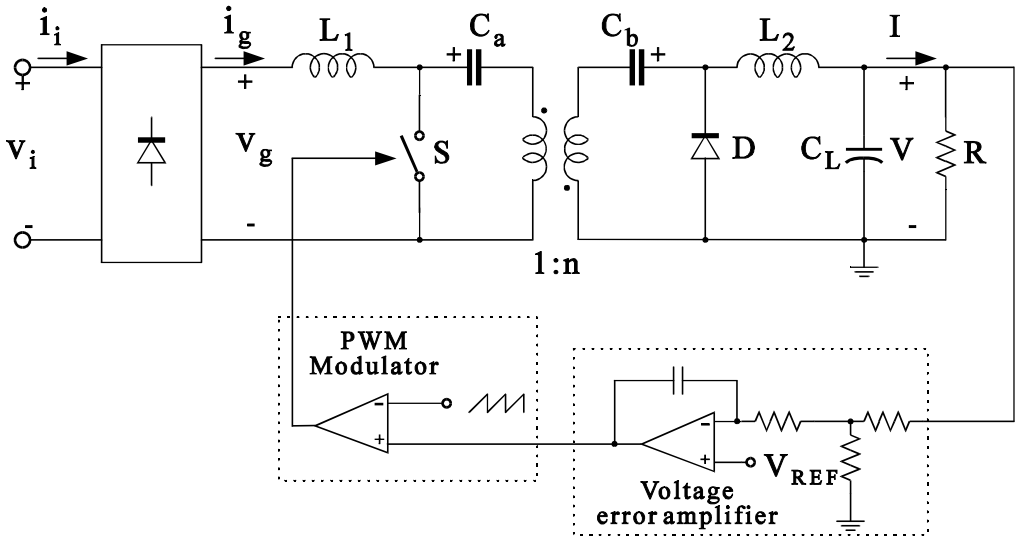
CONTROL IC'S

Constant frequency peak current control	ML4812 (Micro Linear) TK84812 (Toko)
Constant frequency average current control	UC1854/A/B family (Unitrode) UC1855 (Unitrode) TK3854A (Toko) ML4821 (Micro Linear) TDA4815, TDA4819 (Siemens) TA8310 (Toshiba) L4981A/B (SGS-Thomson) LT1248, LT1249 (Linear Tech.)
Hysteretic control	CS3810 (Cherry Semic.)
Borderline control	TDA4814, TDA4816, TDA4817, TDA4818 (Siemens) SG3561 (Silicon General) UC1852 (Unitrode) MC33261, MC33262(Motorola) L6560 (SGS-Thomson)
Two stage PFC with average-current control	UC1891/2/3/4 family (Unitrode) ML4824, ML4826 (Micro Linear) TK65030 (Toko)
Two stage PFC with peak-current control	ML4819 (Micro Linear) TK84819 (Toko)
Buck-boost constant frequency automatic control	ML4813 (Micro Linear)

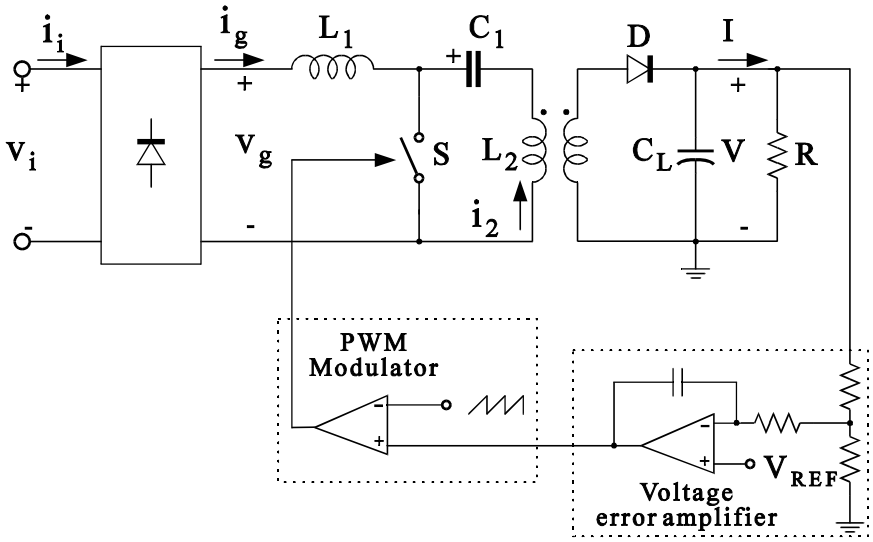
INSULATED POWER FACTOR CORRECTOR TOPOLOGIES

PREREGULATORS BASED ON CUK AND SEPIC CONVERTERS

DCM OPERATION



Cuk converter

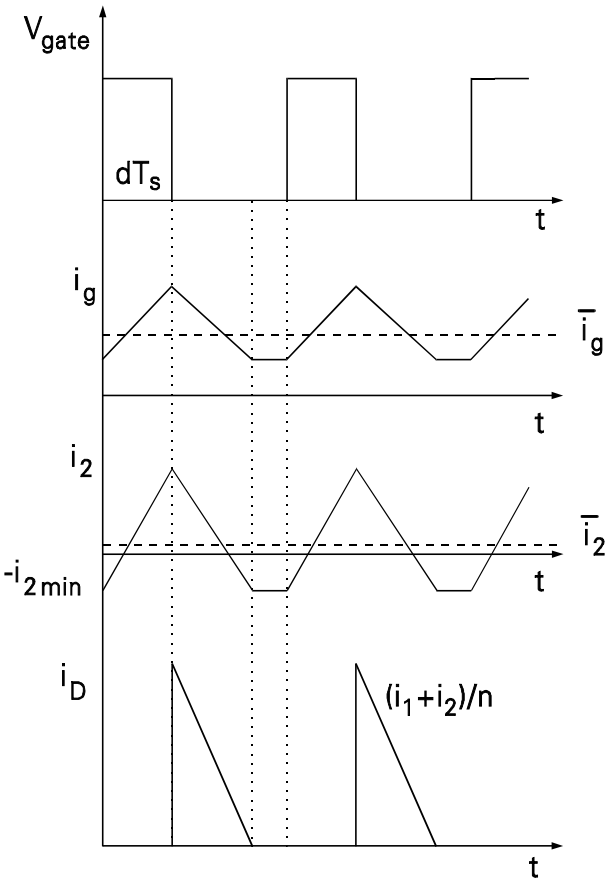


Sepic converter

PREREGULATORS BASED ON CUK AND SEPIC CONVERTERS

DCM OPERATION

Inductor and diode current waveforms
during a switching period for a Sepic converter



DCM operation = diode current zeroes during switch turn off interval

PREREGULATORS BASED ON CUK AND SEPIC CONVERTERS

DCM OPERATION

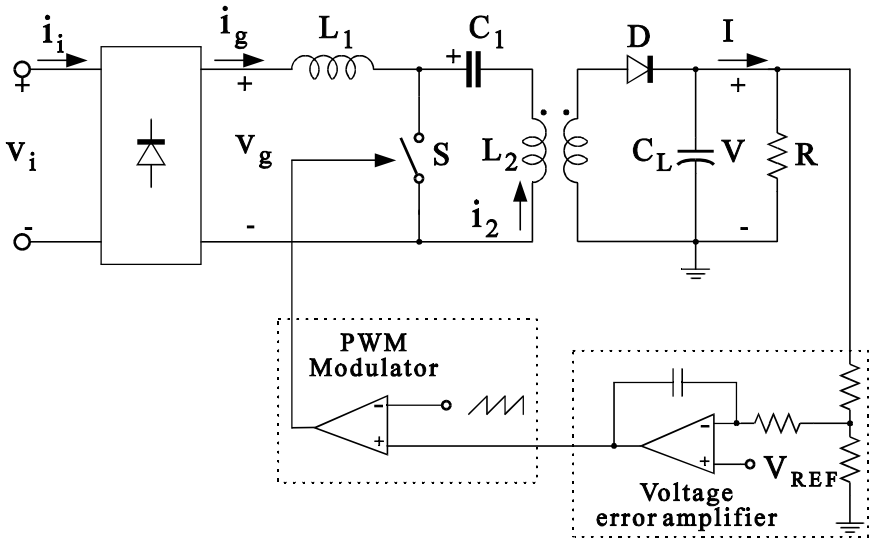
Diode current = sum of inductor currents

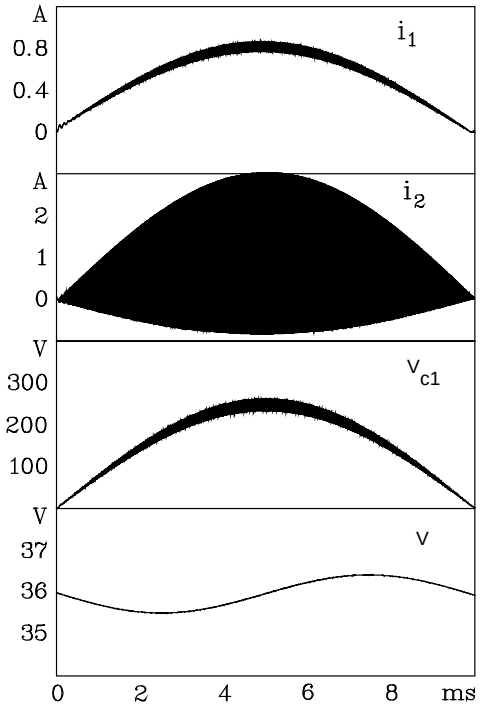
CONSEQUENCE:

By choosing suitable values for inductors L_1 and L_2 it is possible to obtain a low high-frequency input current ripple

PREREGULATORS BASED ON CUK AND SEPIC CONVERTERS

Simulated waveforms of a Sepic preregulator





CUK PREREGULATORS

CHARACTERISTICS:

- o CONSTANT SWITCHING FREQUENCY
- o GOOD TRANSFORMER EXPLOITATION
- o DCM OPERATION
  - - high device current stresses
  - - small EMI filter
  - - reduced switch turn on losses and increased turn off losses
  - - soft diode turn off
- o SIMPLE CONTROL SCHEME
  - - no need of current sensing
  - - no need of multiplier
- o POSSIBILITY OF MAGNETIC COUPLING (REDUCTION OF MAGNETIC STRUCTURE SIZE AND INPUT CURRENT RIPPLE)

SEPIC PREREGULATORS

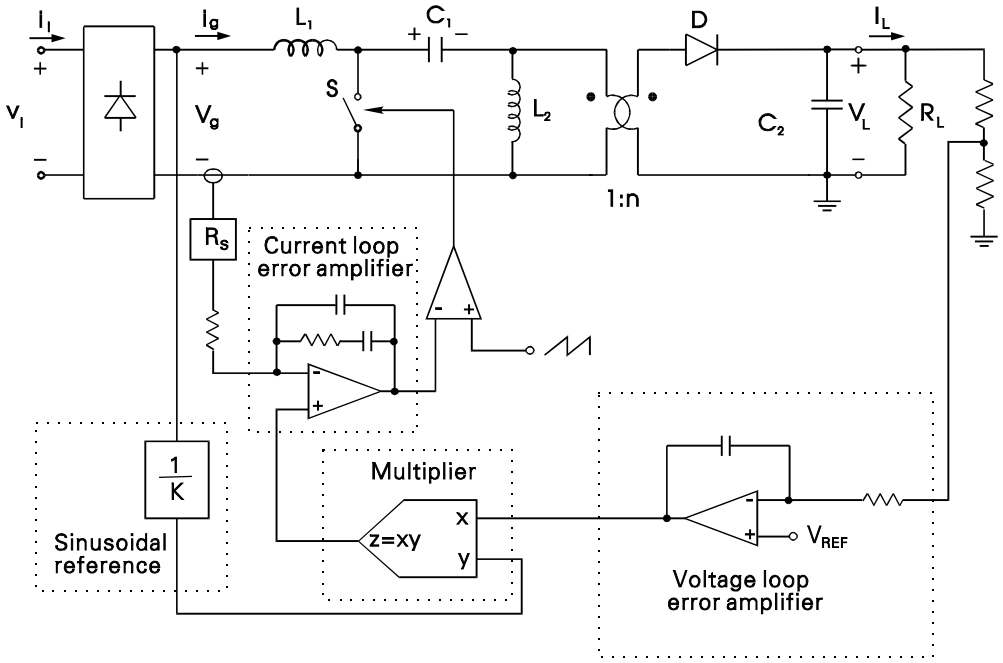
CHARACTERISTICS:

- CONSTANT SWITCHING FREQUENCY
- POOR TRANSFORMER EXPLOITATION
- DCM OPERATION
  - high device current stresses
  - small EMI filter
  - reduced switch turn on losses and increased turn off losses
  - soft diode turn off
- SIMPLE CONTROL SCHEME
  - no need of current sensing
  - no need of multiplier
- POSSIBILITY OF MAGNETIC COUPLING (REDUCTION OF MAGNETIC STRUCTURE SIZE AND INPUT CURRENT RIPPLE)

PREREGULATORS BASED ON CUK AND SEPIC CONVERTERS

CCM OPERATION

EXAMPLE: Sepic converter with average current mode control



PROBLEM: design of the inner current loop

PREREGULATORS BASED ON CUK AND SEPIC CONVERTERS

CCM OPERATION

Transfer function between duty-cycle and input current:

$$G_{id}(s) = \frac{DV_D}{D'^2 L_2' + D^2 L_1} \cdot \frac{1 + \frac{I_c}{V_D}\frac{D'}{D} L_2' \cdot s + \frac{L_2' C_1'}{D} \cdot s^2}{s \cdot \left(1 + \frac{L_1 L_2' C_1'}{D'^2 L_2' + D^2 L_1} \cdot s^2 \right)}$$

where D'=1-D.

APPROXIMATION: $G_{id}(s) \approx \frac{V_D}{sL_1}$ V_D depends on input voltage

(for the boost preregulator is: $G_{id}(s) \approx \frac{V}{sL}$, i.e. constant gain)

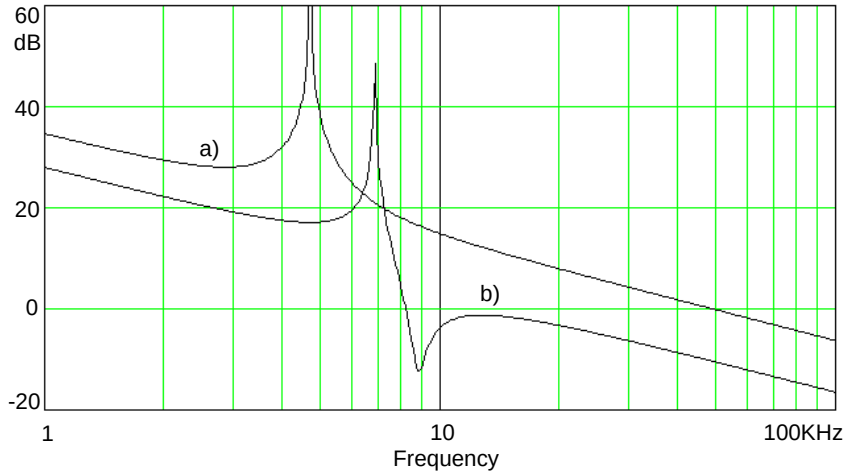
	Sepic	Cuk
V_D	$V_g + V/n$	$V_g + V/n$
I_c	$I_1 + I_2$	$I_1 + n I_2$
C_1'	C_1	$\frac{C_a \cdot n^2 C_b}{C_a + n^2 C_b}$
L_2'	L_2	L_2 / n^2

PREREGULATORS BASED ON CUK AND SEPIC CONVERTERS

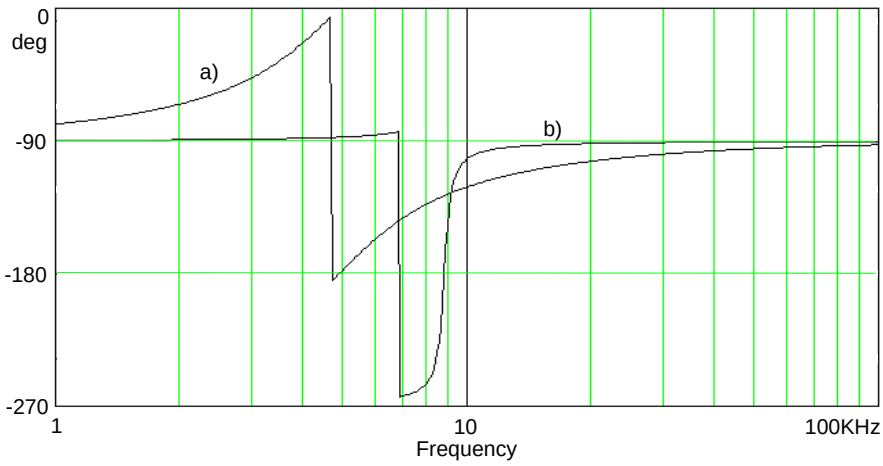
CCM OPERATION

Transfer function plot

$|G_{id}(s)|$



$\angle G_{id}(s)$



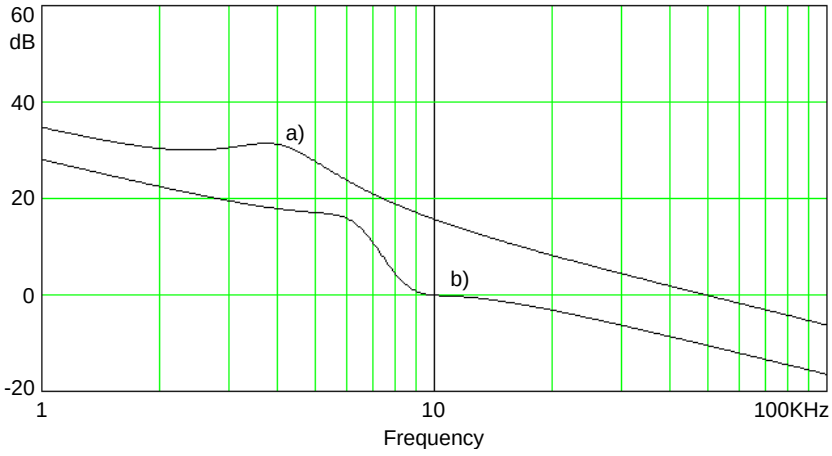
a) $\pi=\pi/2$, b) $\pi=\pi/18$

PREREGULATORS BASED ON CUK AND SEPIC CONVERTERS

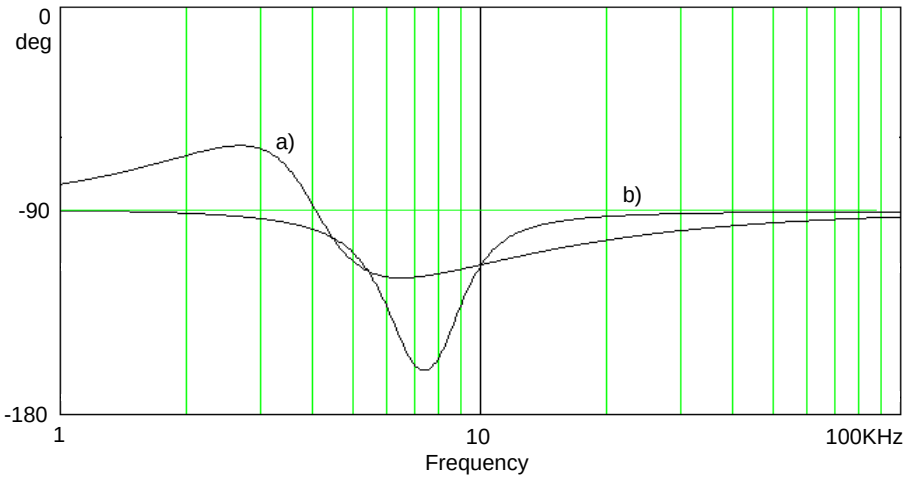
CCM OPERATION

A damping R_d-C_d network across energy transfer capacitor C_1 is used to properly shape the transfer function

$|G_{id}(s)|$



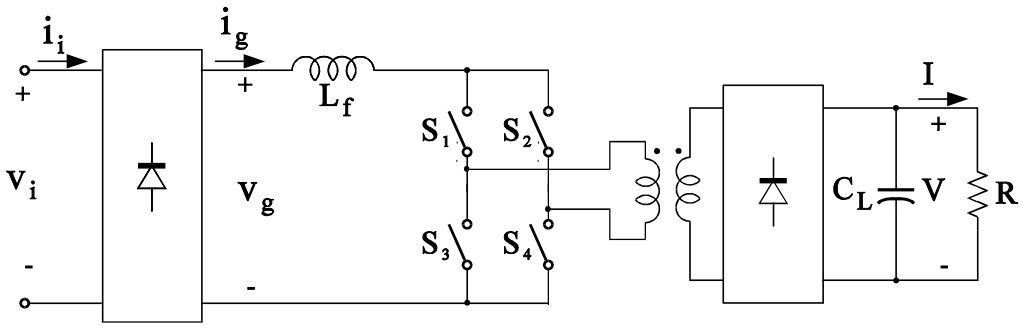
$\angle G_{id}(s)$



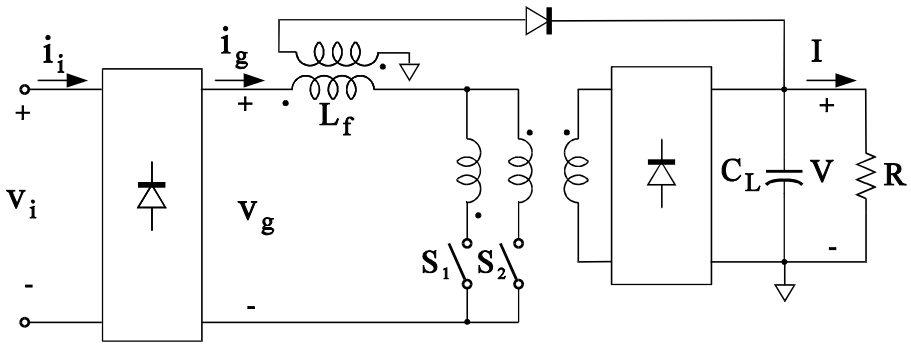
a) π=π2, b) π=π/18

INSULATED BOOST PREREGULATORS

FULL-BRIDGE BOOST CONVERTER



TWO-SWITCH BOOST CONVERTER



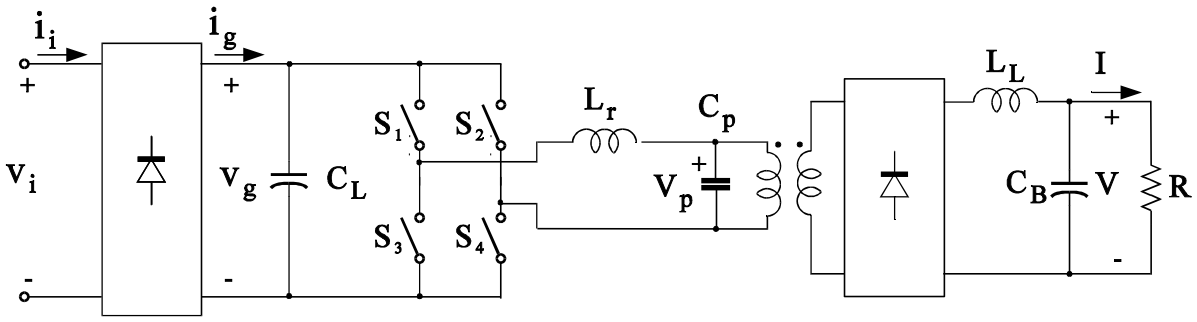
A coupling winding to the input inductor is added to implement start-up and overload protection: during these conditions the converter operates in **flyback mode**

INSULATED BOOST PREREGULATORS

CHARACTERISTICS:

- DIFFICULT TRANSFORMER IMPLEMENTATION
  - low leakage inductance is essential
- NEED OF A SUITABLE CLAMP CIRCUIT
- HIGH VOLTAGE STRESS IN THE TWO-SWITCH IMPLEMENTATION

PARALLEL RESONANT PREREGULATOR



OPERATION AS DC/DC CONVERTER

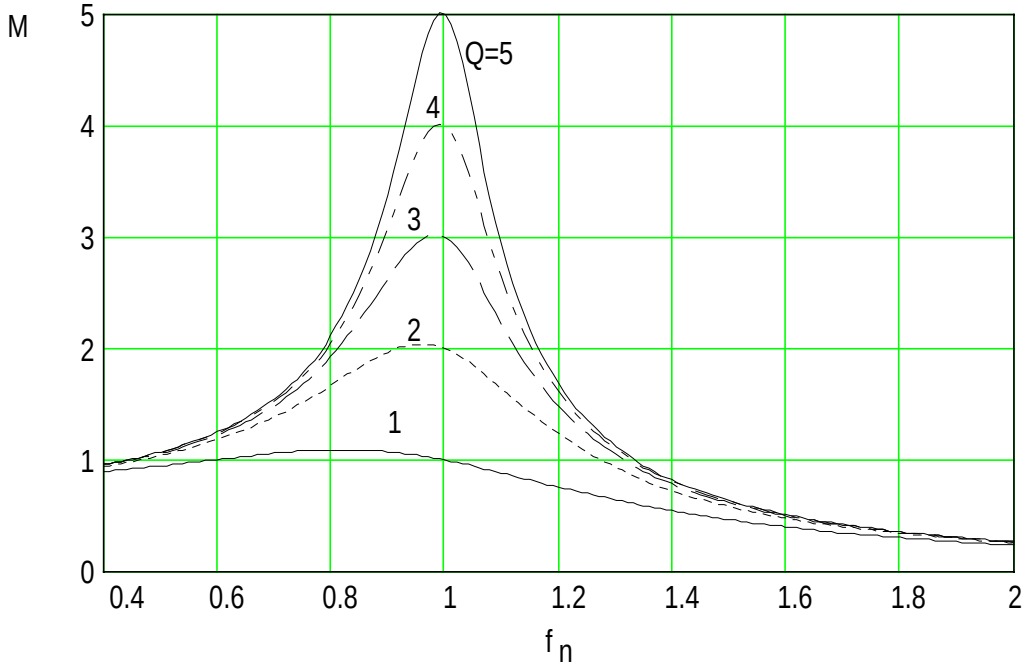
Voltage conversion ratio:

$$M = \frac{v_p}{v_g} = \frac{1}{\frac{\pi^2}{8}\cdot\left[1-f_n^2\right]+\frac{j}{Q}\cdot f_n}, \qquad f_n = \frac{f}{f_r}$$

$$f_r = \frac{1}{2\pi\sqrt{L_r C_p}}, \qquad Q = R\sqrt{\frac{C_p}{L_r}}$$

PARALLEL RESONANT PREREGULATOR

GAIN CHARACTERISTICS

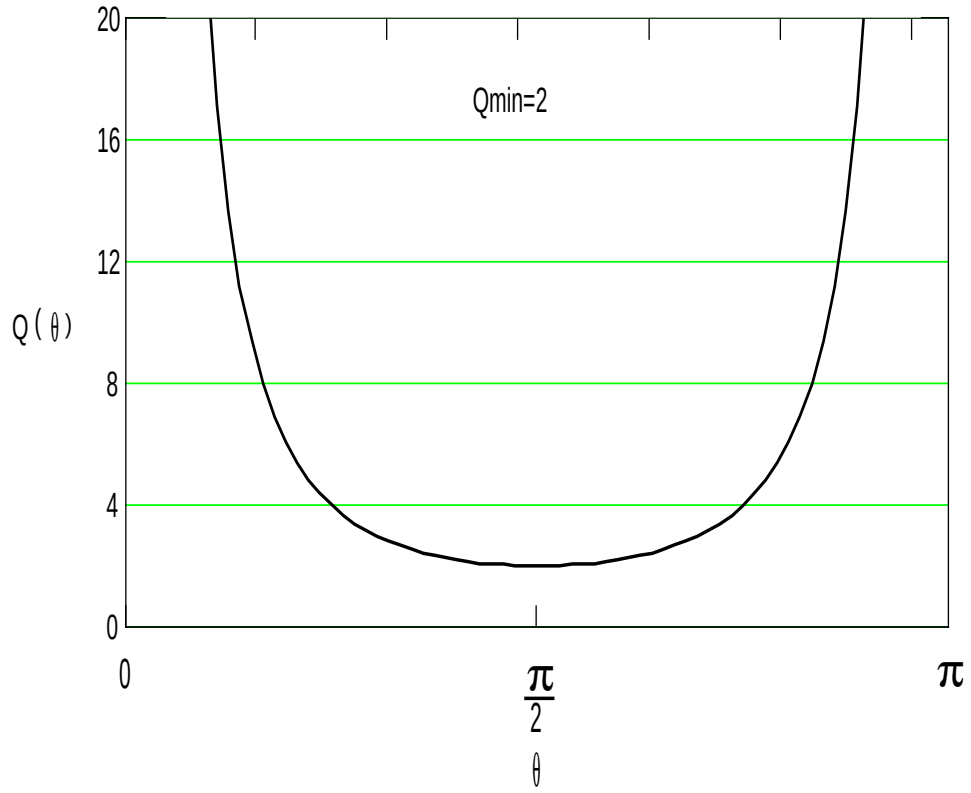


PARALLEL RESONANT PREREGULATOR

OPERATION AS AC/DC CONVERTER

$$Q(\theta) = \frac{R'(\theta)}{Z_r} = \frac{R}{2\sin^2(\theta)} \cdot \frac{1}{Z_r}$$

Q factor variation during a half line cycle



- Near the zero crossing the circuit is lightly damped
  - ➢ HIGH GAIN
- Near the peak of ac line the circuit is heavily damped
  - ➢ LOW GAIN

PARALLEL RESONANT PREREGULATOR

OPERATION AS AC/DC CONVERTER

CONSEQUENCE:

Good power factor (>90%) is obtained without active control of the line current.

NOTE:

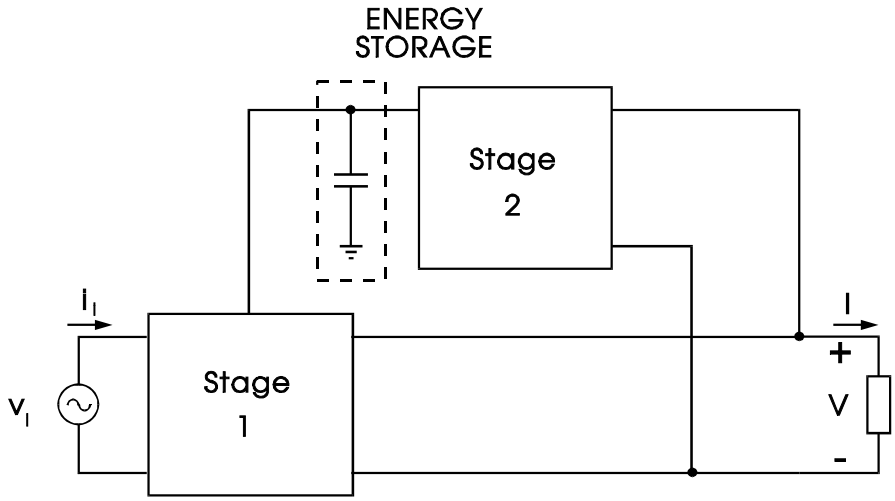
The same result holds also for the series/parallel (LCC) resonant converter. For this converter, an active control is necessary to maintain zero voltage switching condition (operation must remain on the right side of resonant peaks in all operating conditions)

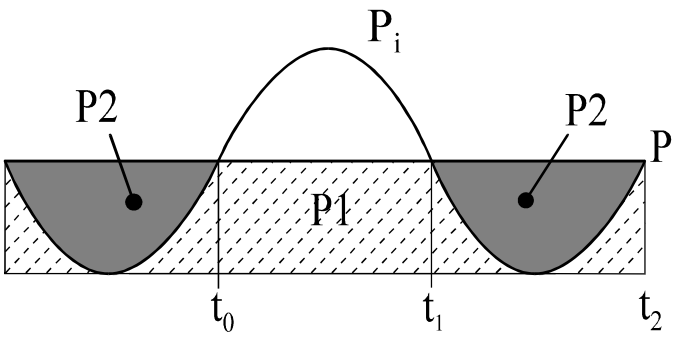
FAST RESPONDING POWER FACTOR CORRECTOR TOPOLOGIES

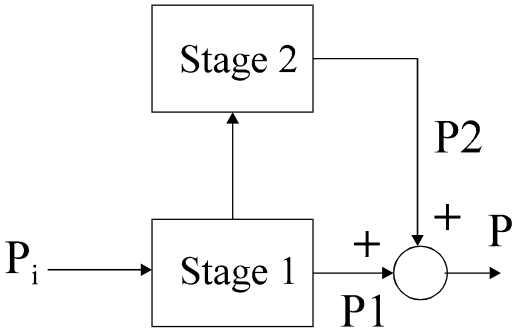
OBJECTIVES:

- COMPACTNESS
- HIGH POWER FACTOR
- TIGHT AND FAST OUTPUT VOLTAGE REGULATION
- HIGH-FREQUENCY INSULATION

TWO STAGE PFC: PARALLEL CONNECTION

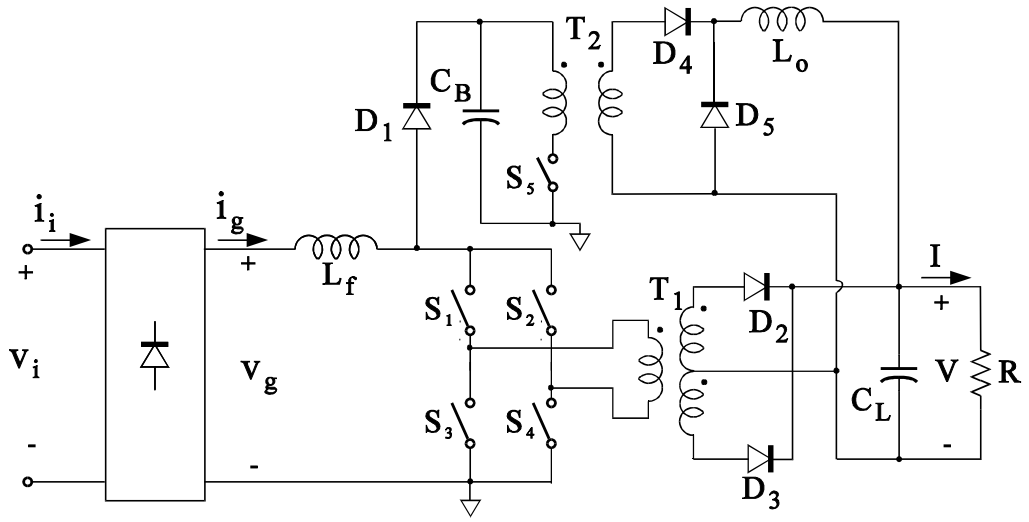


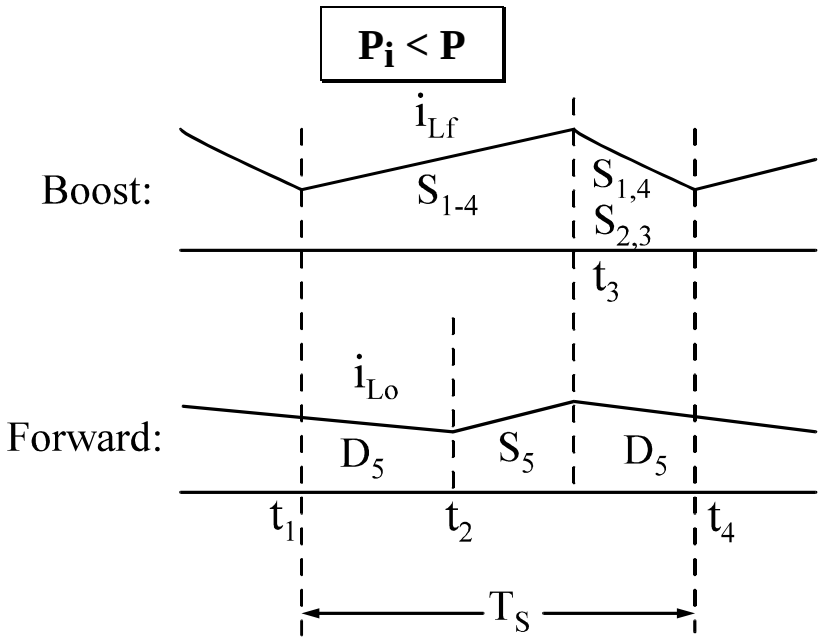




About 68% of input power goes directly to the output through stage 1, while stage 2 processes only 32% of input power

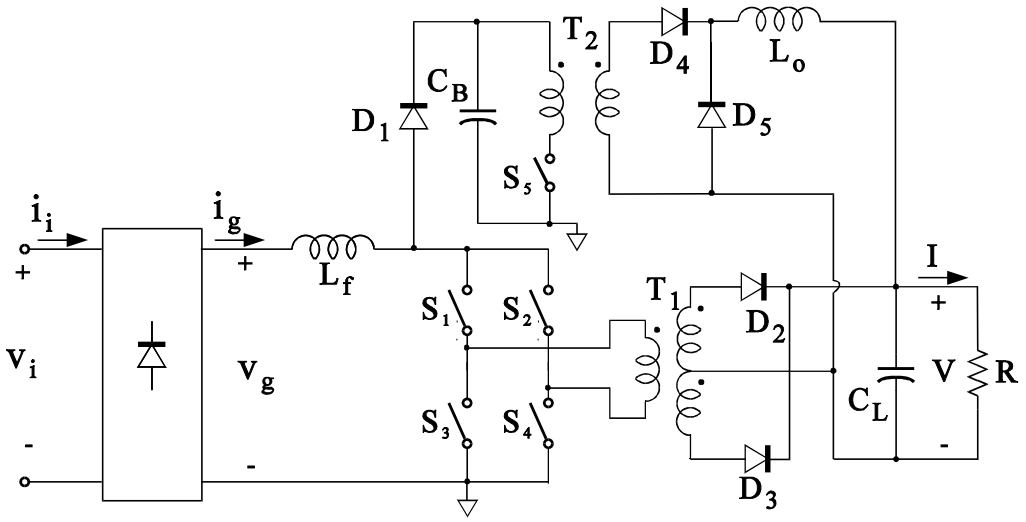
TWO STAGE PFC: PARALLEL CONNECTION



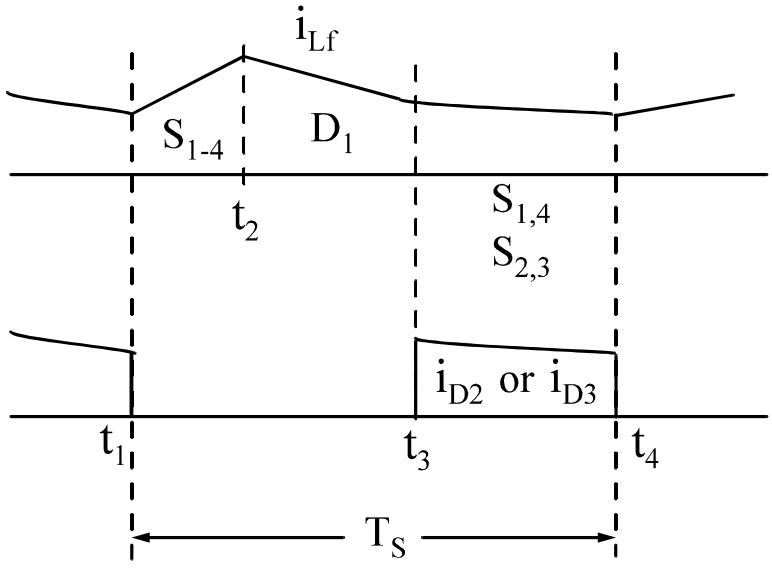


- Boost converter controls power factor
- Forward converter regulates output
- C_B stores energy
- C_L is small

TWO STAGE PFC: PARALLEL CONNECTION

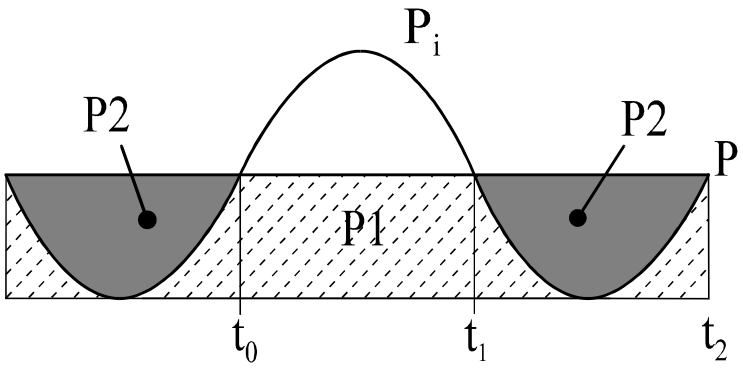


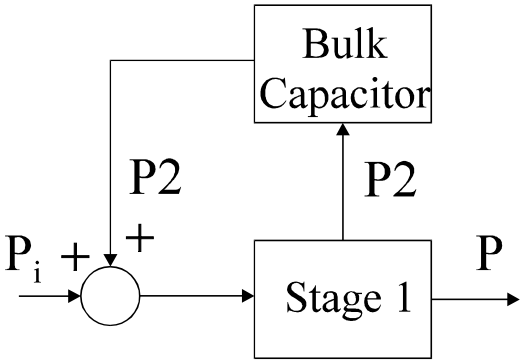
$P_i > P$



- t_2 controls power factor
- t_3 regulates output

SINGLE STAGE PFC: PARALLEL POWER PROCESSING

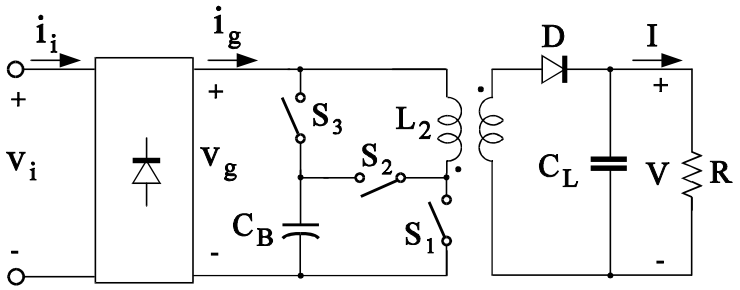




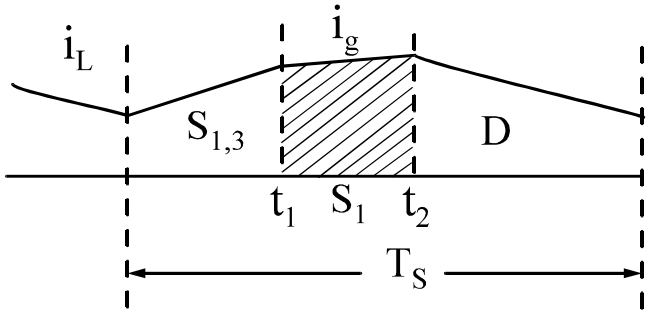
- need for several switches
- complex control
- discontinuous input current at least for a part of the line cycle (large EMI filter)

SINGLE STAGE PFC: PARALLEL POWER PROCESSING

EXAMPLE: FLYBACK CONVERTER



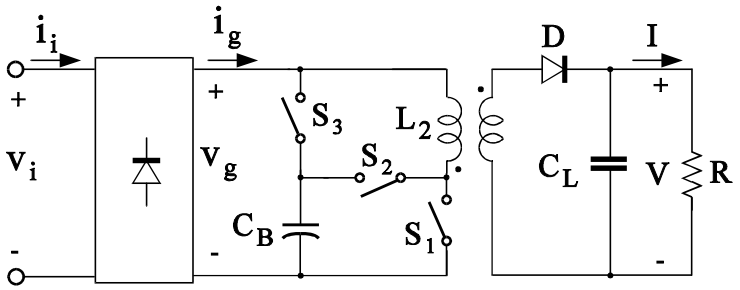
$$P_i < P$$



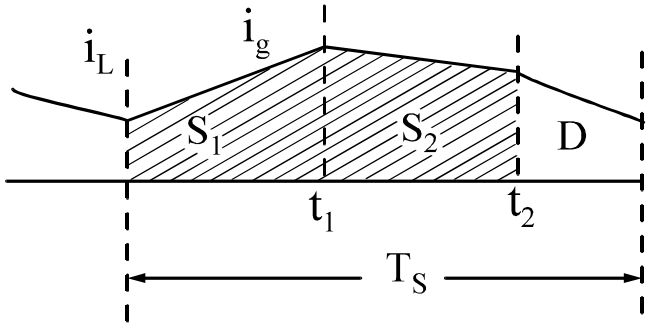
- t_2 controls power factor
- t_1 regulates output
- C_B stores energy
- C_L is small

SINGLE STAGE PFC: PARALLEL POWER PROCESSING

EXAMPLE: FLYBACK CONVERTER



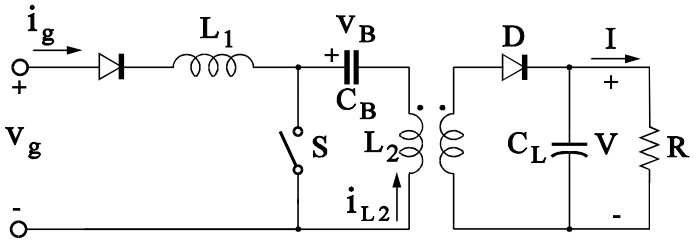
$$P_i > P$$



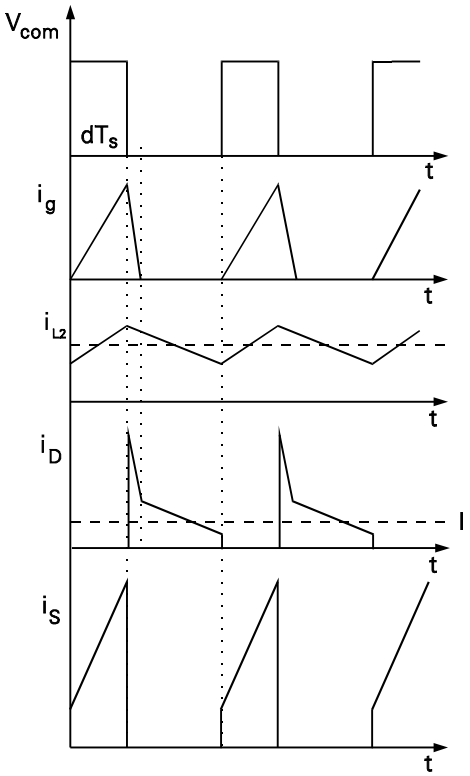
- t_1 controls power factor
- t_2 regulates output

SINGLE STAGE PFC: BIFRED

(Boost Integrated with Flyback Rectifier/Energy storage/DC-DC converter)



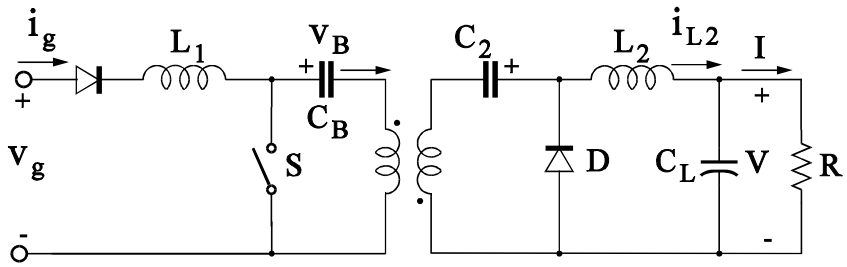
Main waveforms



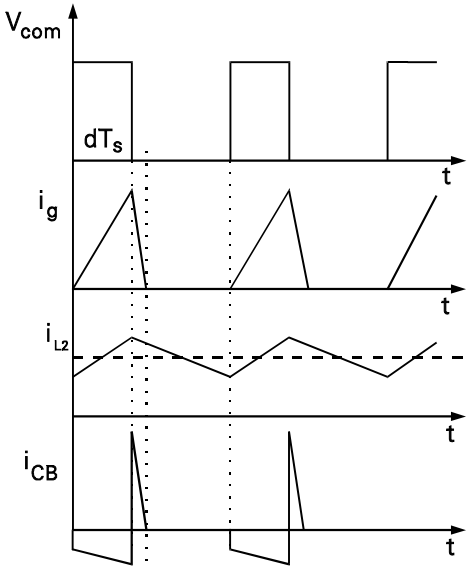
- DCM input current ensures high power factor
- duty-cycle regulates output
- C_B stores energy
- C_L is small

SINGLE STAGE PFC: BIBRED

(Boost Integrated with Buck Rectifier/Energy storage/DC-DC converter)



Main waveforms



- DCM input current ensures high power factor
- duty-cycle regulates output
- C_B stores energy
- C_L is small

SINGLE STAGE PFC: BIFRED, BIBRED

CHARACTERISTICS:

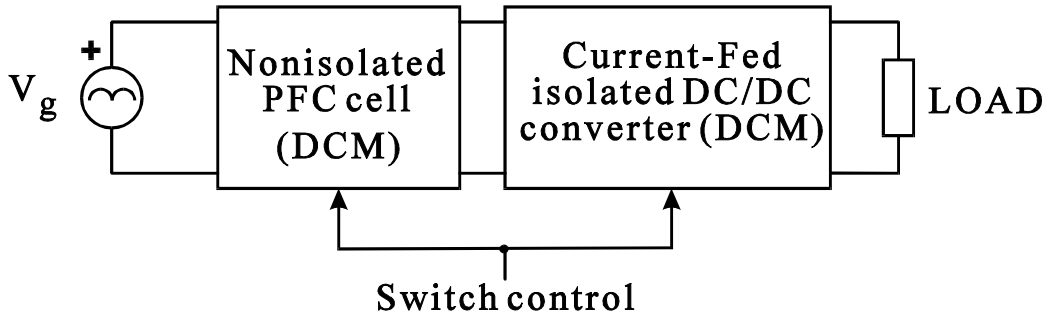
- DCM OPERATION
  - high device current stresses
  - big EMI filter
- TANK CAPACITOR VOLTAGE V_B IS LOAD AND LINE DEPENDENT
  - high device voltage stresses
  - limited load range

SOLUTIONS:

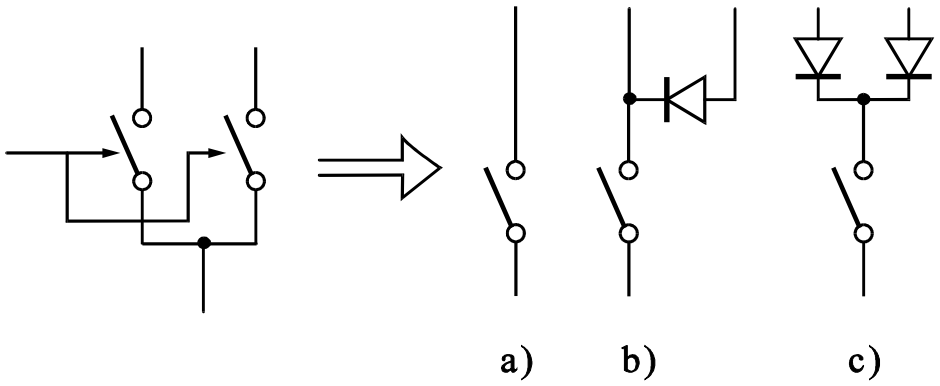
- VARIABLE FREQUENCY CONTROL
  - trade-off between voltage stress and frequency range of control
- DISCONTINUOUS OUTPUT CURRENT OPERATION

SINGLE STAGE PFC: S²IP² FAMILY

(Single-Stage Isolated Power-factor corrected Power supplies)



COMBINING SWITCHES



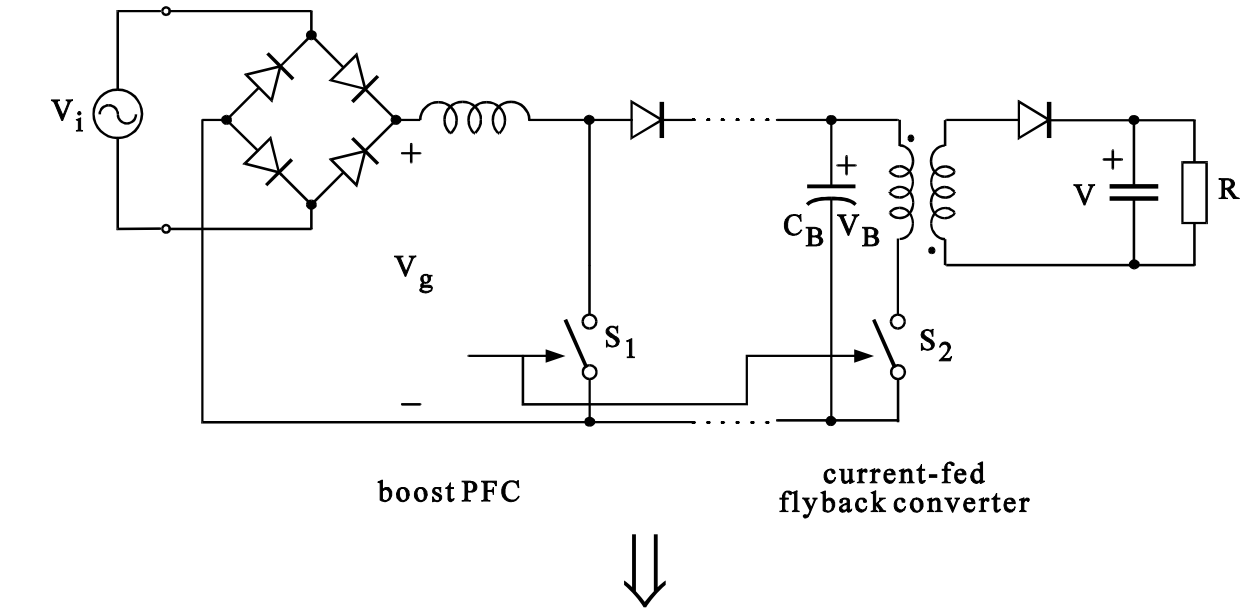
a) when the off voltages are the same

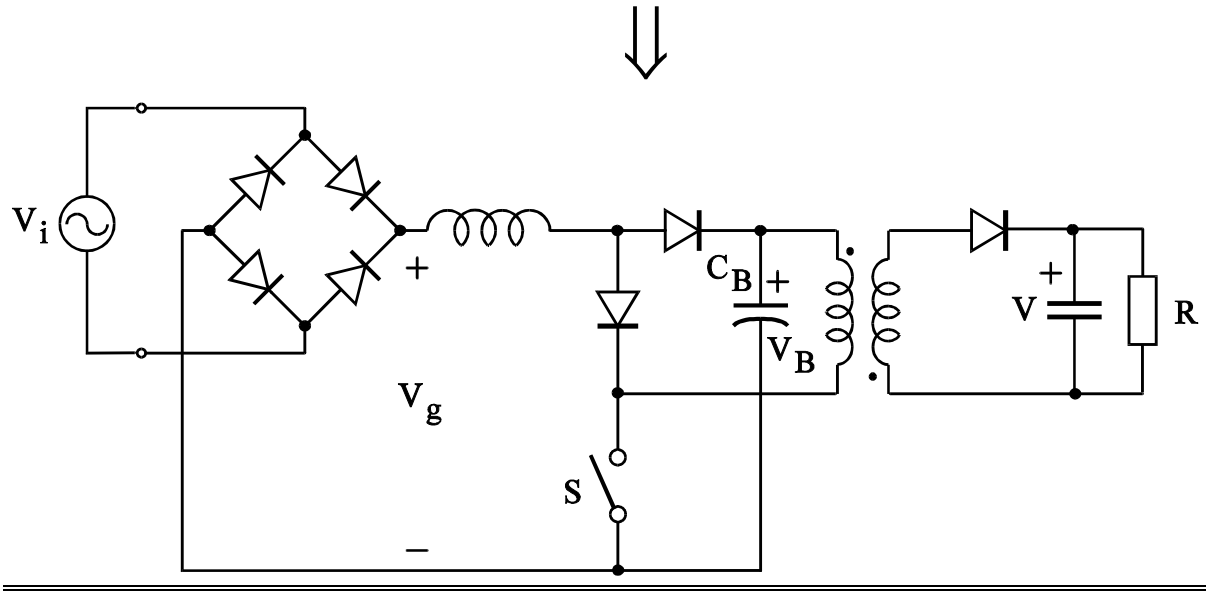
b) when the off voltage of the left switch is always higher than the off voltage of the right switch

c) when the off voltage of a switch can be higher or lower than the off voltage of the other switch

SINGLE STAGE PFC: S²IP² FAMILY

EXAMPLE: BOOST+FLYBACK





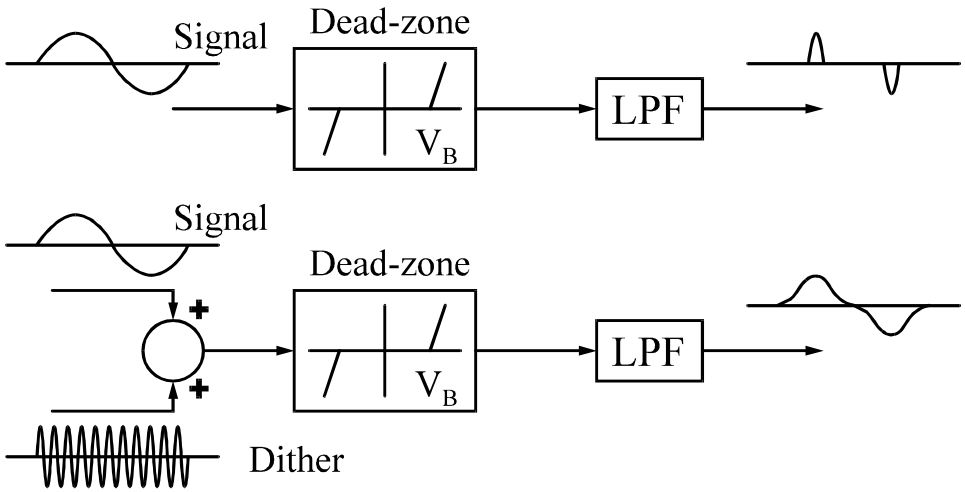
SINGLE STAGE PFC: S^2IP^2 FAMILY

CHARACTERISTICS:

- SINGLE POWER STAGE WITH SINGLE HIGH-SPEED CONTROL LOOP (PWM CONTROL)
- TANK CAPACITOR VOLTAGE V_B INDEPENDENT OF LOAD CURRENT
- DCM OPERATION OF BOTH PFC AND CURRENT-FED DC/DC CONVERTER STAGES
  - high device current stresses
  - big EMI filter

SINGLE STAGE PFC: DITHER RECTIFIERS

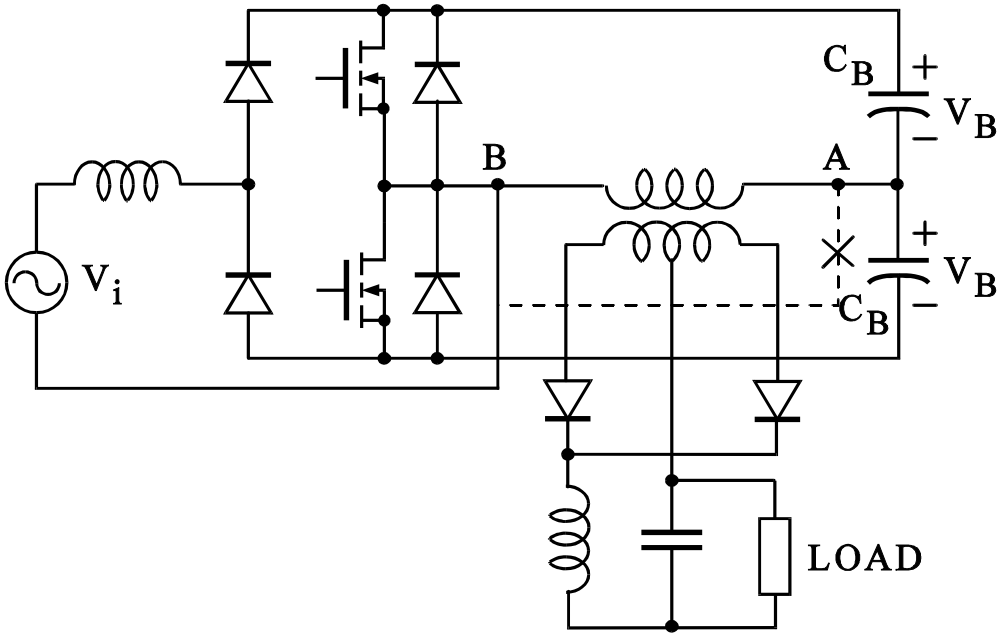
CONCEPT



Adding to the low-frequency input signal a high-frequency signal with amplitude higher than V_B increases the conduction interval of the dead-zone element (diode-capacitor rectifier)

SINGLE STAGE PFC: DITHER RECTIFIERS

EXAMPLE: VOLTAGE DOUBLER + HALF-BRIDGE CONVERTER



The connection is moved from point A to point B. In this way, the high-frequency signal present on the inverter leg is added to the input voltage. An inductor is needed to smooth the input current.

SINGLE STAGE PFC: DITHER RECTIFIERS

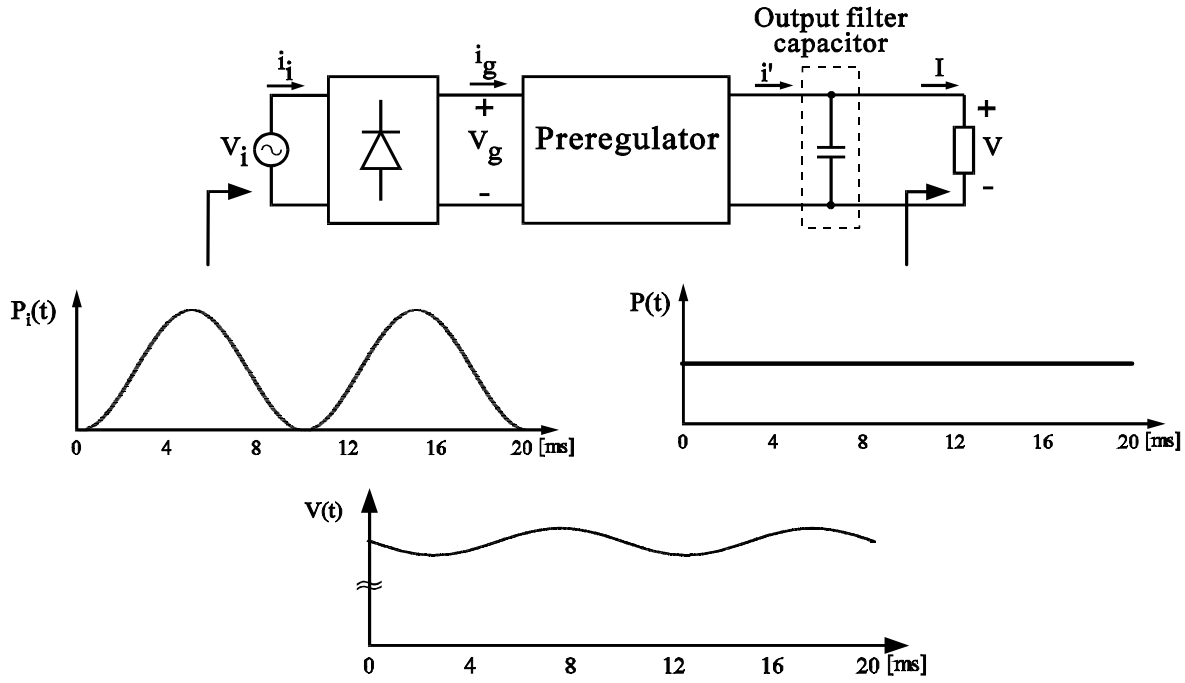
EXAMPLE: VOLTAGE DOUBLER + HALF-BRIDGE CONVERTER

CHARACTERISTICS:

- o DCM OPERATION
  - high device current stresses
  - big EMI filter
- o TANK CAPACITOR VOLTAGE V_B IS LOAD AND LINE DEPENDENT
  - high device voltage stresses
  - limited load range
- o VARIABLE FREQUENCY CONTROL

TECHNIQUES FOR IMPROVING OUTPUT VOLTAGE CONTROL SPEED

NATURE OF THE PROBLEM - 1



GOAL:

To improve the dynamic response of power factor preregulators by manipulation of the output voltage feedback signal without additional sensing and with limited increase of control complexity

NATURE OF THE PROBLEM - 2

Output voltage behavior:

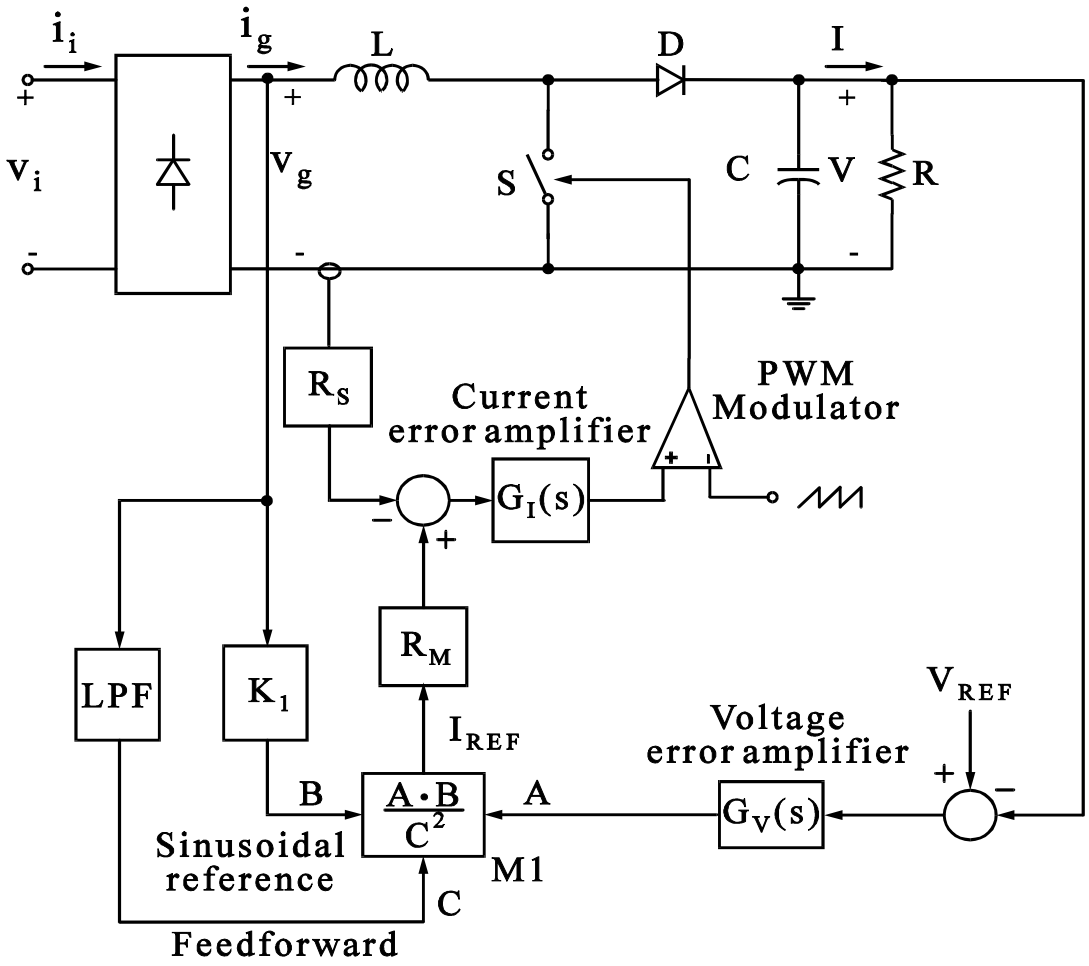
$$v(t) = V_{DC} + \Delta v(t) = V_{DC} - \frac{P}{2\omega_i CV} \cdot \sin(2\omega_i t)$$

The voltage error signal contains a low-frequency ripple at twice the line frequency

CONSEQUENCE:

the bandwidth of the voltage loop must be kept below the line frequency in order to avoid input current distortion

LINE FEEDFORWARD

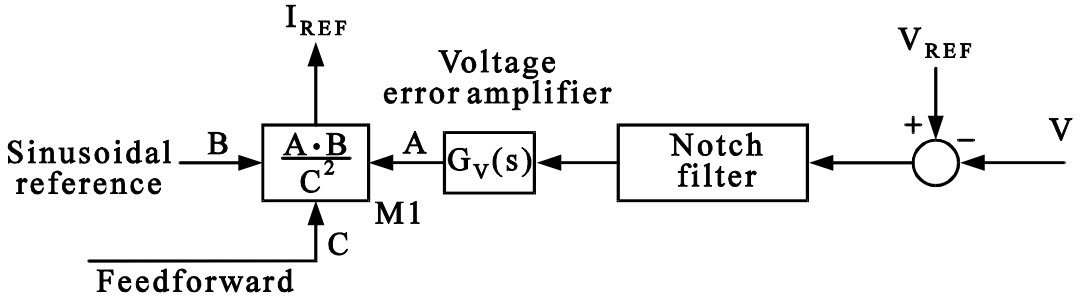


The low-pass filter provides a voltage proportional to the RMS input voltage which is squared and used in the multiplier to divide the current reference

⇓

this avoids heavy compensating actions by the voltage error amplifier during line transients

CONTROL SCHEME WITH NOTCH FILTER

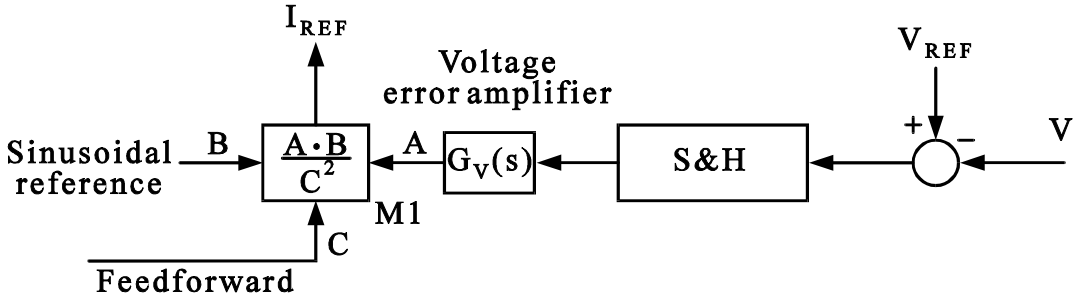


A notch filter tuned at twice the line frequency is inserted in the feedback path in order to remove the output voltage low-frequency ripple from the feedback signal

COMMENTS:

- the filter must be well tuned with high quality factor
- the bandwidth is limited below twice the line frequency

CONTROL SCHEME WITH SAMPLE & HOLD



By sampling the output voltage error signal at a rate equal to the voltage ripple near zero crossing of the line voltage, the average output voltage is sensed.

COMMENTS:

- a high power factor is maintained in both transient and steady-state conditions
- the bandwidth is limited below twice the line frequency

CONTROL SCHEME WITH RIPPLE COMPENSATION

$$\Delta v(t) = -\frac{P}{2\omega_i CV} \cdot \sin(2\omega_i t)$$

The output voltage ripple is estimated and subtracted to the feedback signal so that the error amplifier processes a ripple-free signal

Under unity power factor condition, input power is given by:

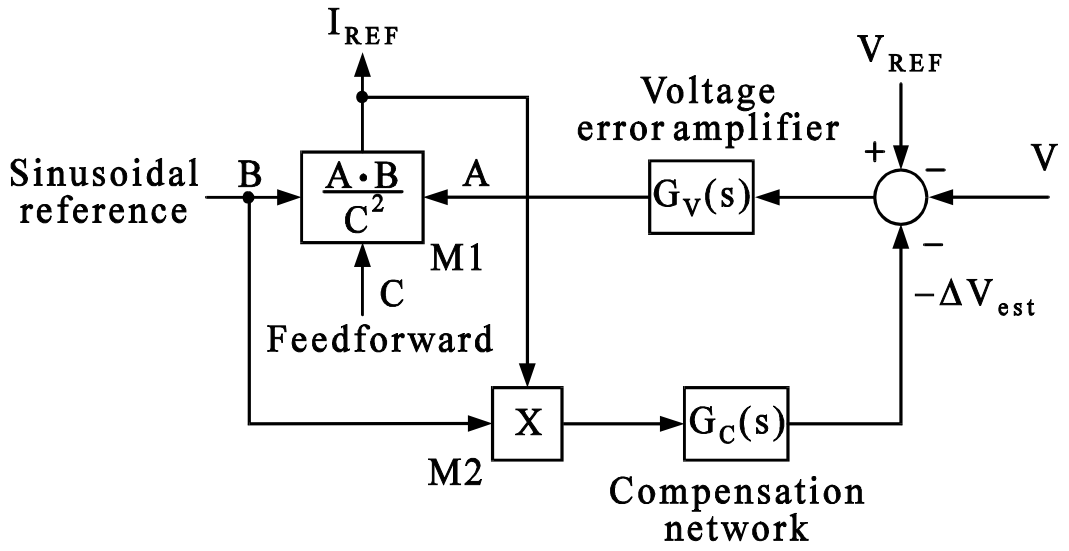
$$p_i(t) = \eta P - \frac{\eta P}{2} \cdot \cos(2\omega_i t)$$

where h is converter efficiency.

Error signal $\Delta v(t)$ can be estimated from input power signal through:

- Elimination of DC component
- Phase shifting of ninety degrees
- Multiplication by a proper gain

CONTROL SCHEME WITH RIPPLE COMPENSATION



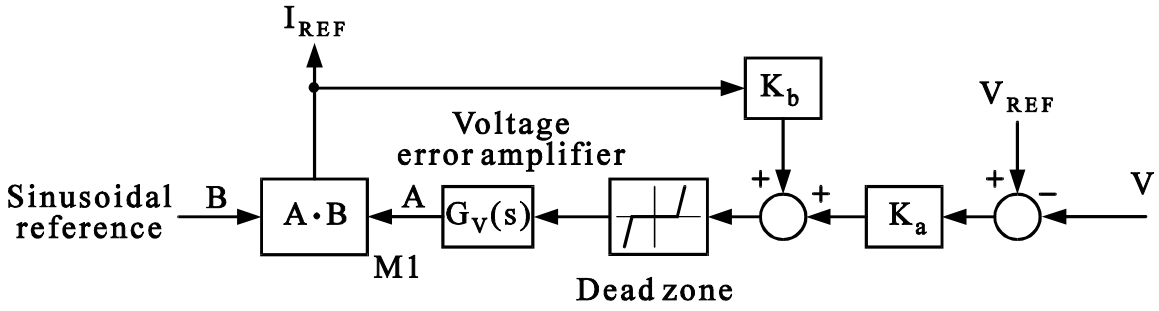
$$G_c(s) = K_c \cdot s$$

COMMENTS:

- in the presence of distorted input voltage, network $G_C(s)$ turns out to be complicated
- a second multiplier is needed
- the bandwidth can be increased above twice the line frequency

CONTROL SCHEME WITH "REGULATION BAND"

REGULATION BAND APPROACH TYPE 1



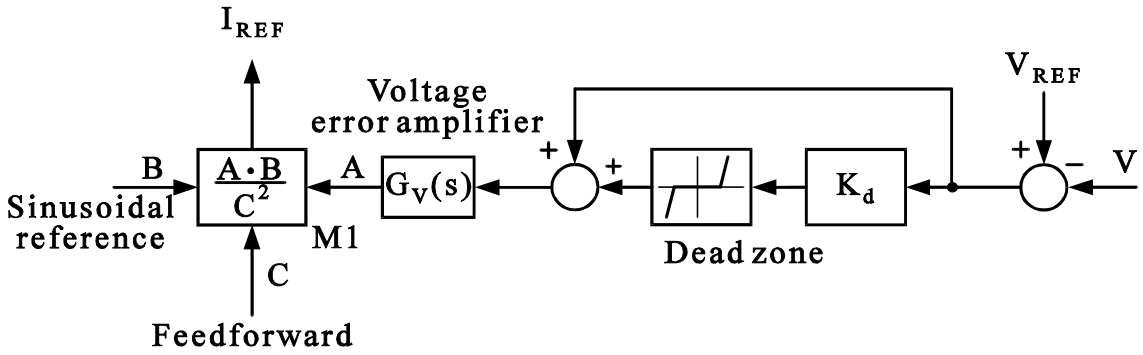
The current reference amplitude is kept constant as long as the output voltage remains within a defined regulation band. When the output voltage goes outside of this band a high gain controller changes rapidly the current reference amplitude so as to bring the output voltage back into the regulation band

COMMENTS:

- correct average output voltage is obtained only at nominal condition in which the voltage ripple amplitude is equal to the dead zone amplitude
- slow input current dynamic response at load step changes

CONTROL SCHEME WITH "REGULATION BAND"

REGULATION BAND APPROACH TYPE 2



In order to overcome the problem represented by the steady-state error on the output voltage of the previous control technique, a low-bandwidth PI controller can be used which ensures stability and no DC errors. When the output voltage goes outside the band, the gain of the voltage error amplifier is increased in order to enhance the corrective action

COMPARISON OF CONTROL STRATEGIES

BOOST POWER FACTOR PREREGULATOR

TABLE 1 - Converter parameters

V_g=220V_{RMS}	V=380V	f_S=50kHz
L=2mH	C=470μF	P=600W

Error voltage amplifier transfer function

$$G_v(s) = \frac{K_I}{s}\left(1 + \frac{s}{\omega_z}\right)$$

TABLE 2 - Error voltage amplifier parameter values

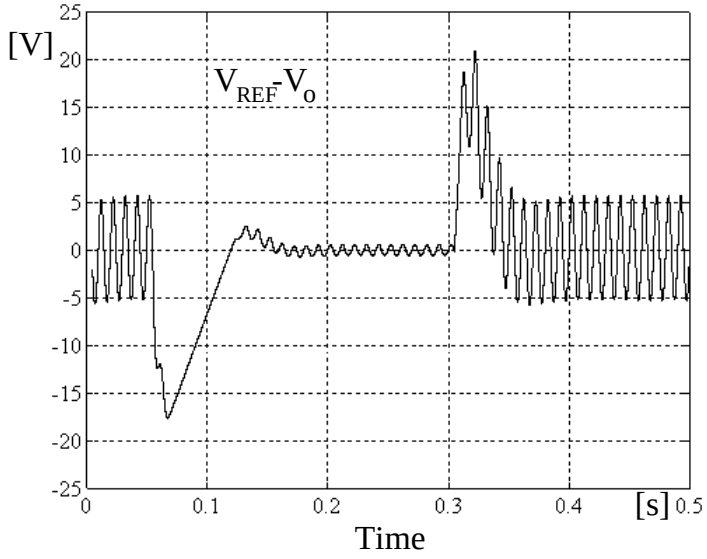
	S.C.	N.F.	S.H.	B.#1	B.#2	R.C.
K_I	8.8	73.4	8.7	100·K_a	8.8·K_d	223
ω_z	69.2	188.5	62.8	166.7	69.2	354.4

(K_a=13.8, K_b=1, K_d=21.4)

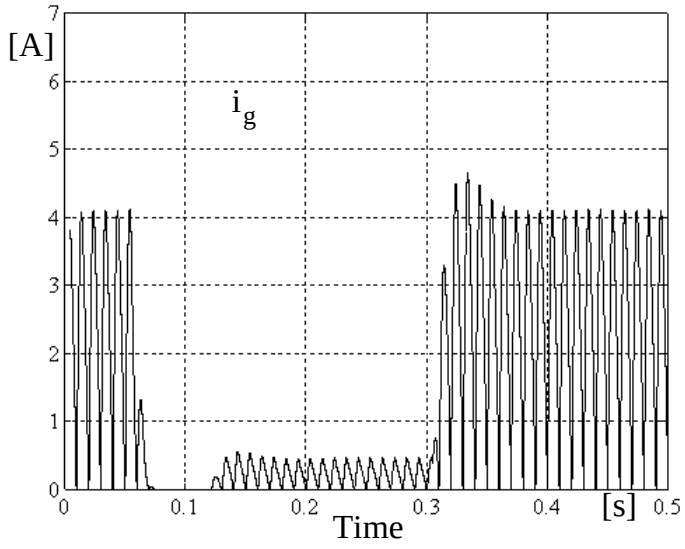
S.C. = Standard Control
N.F. = Notch Filter
S.H. = Sample & Hold
B.#1 = Regulation Band TYPE 1
B.#2 = Regulation Band TYPE 2
R.C. = Ripple Compensation

STANDARD CONTROL

LOAD STEP CHANGE FROM 100% TO 10% OF RATED POWER AND VICE VERSA (SIMULATED RESULTS)



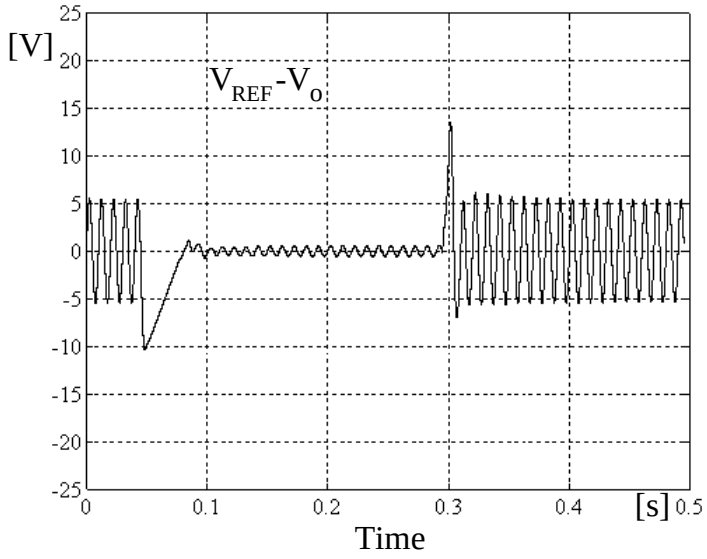
Output voltage error signal



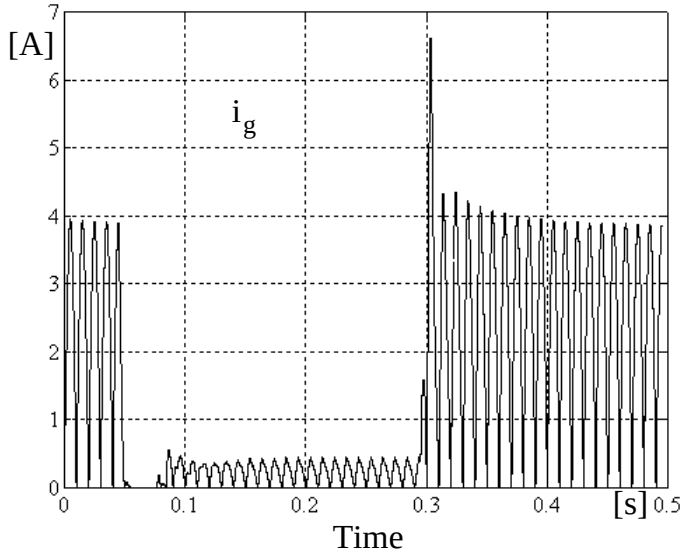
Rectified input current

NOTCH FILTER

LOAD STEP CHANGE FROM 100% TO 10% OF RATED POWER AND VICE VERSA (SIMULATED RESULTS)



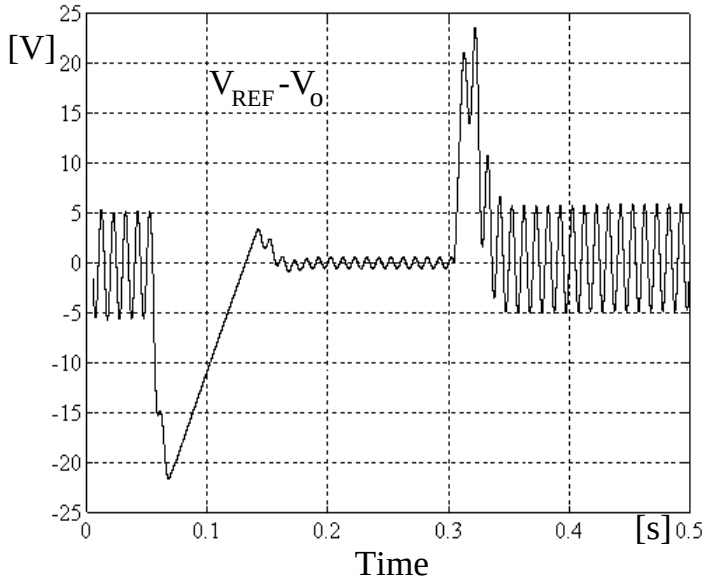
Output voltage error signal



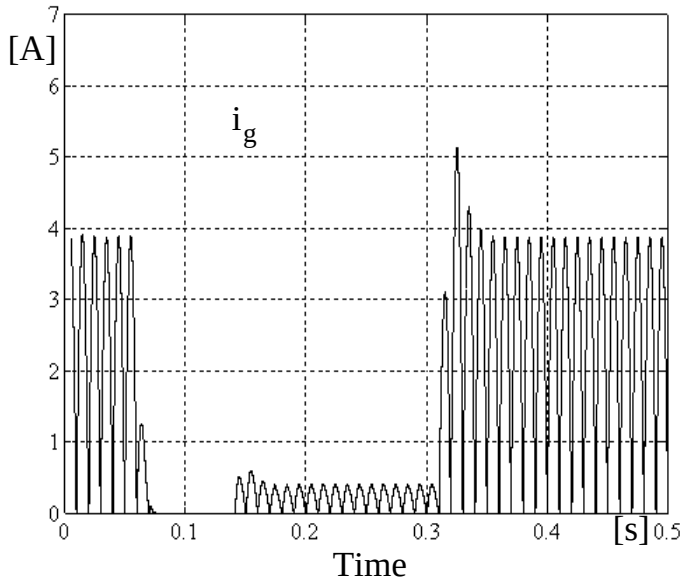
Rectified input current

SAMPLE & HOLD

LOAD STEP CHANGE FROM 100% TO 10% OF RATED POWER AND VICE VERSA (SIMULATED RESULTS)



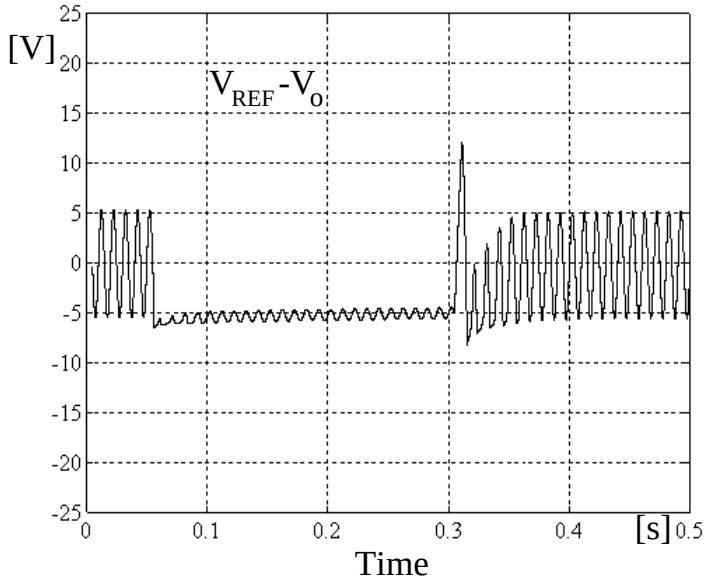
Output voltage error signal



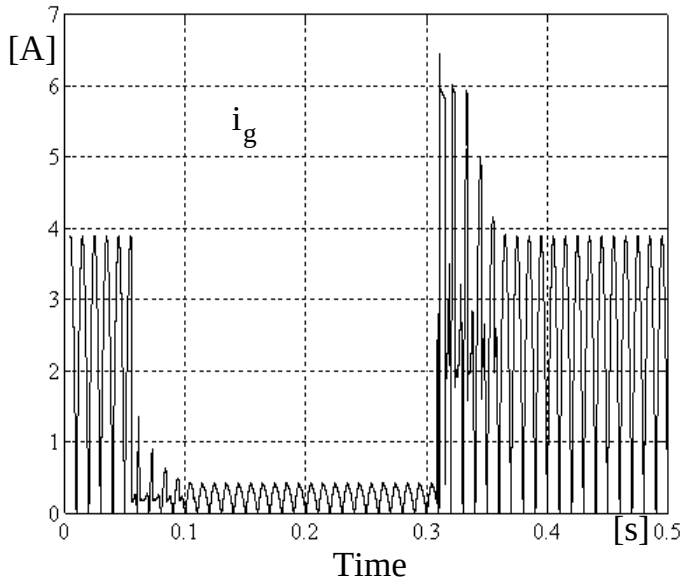
Rectified input current

REGULATION BAND TYPE 1

LOAD STEP CHANGE FROM 100% TO 10% OF RATED POWER AND VICE VERSA (SIMULATED RESULTS)



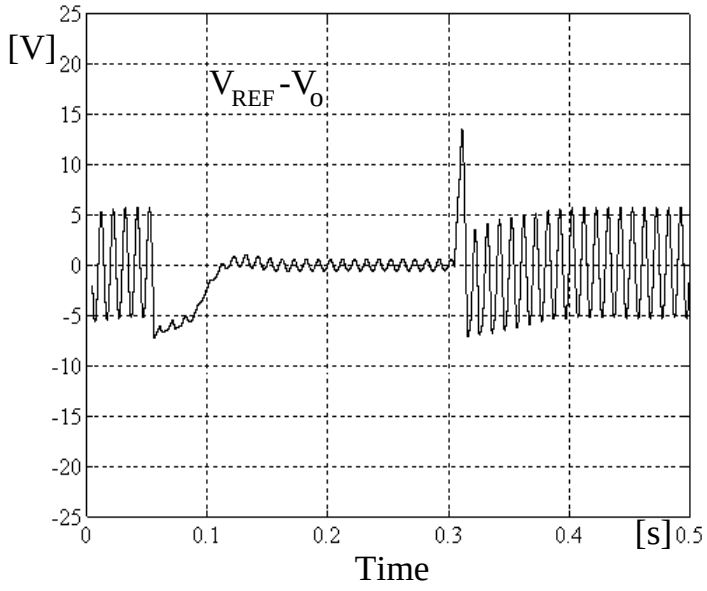
Output voltage error signal



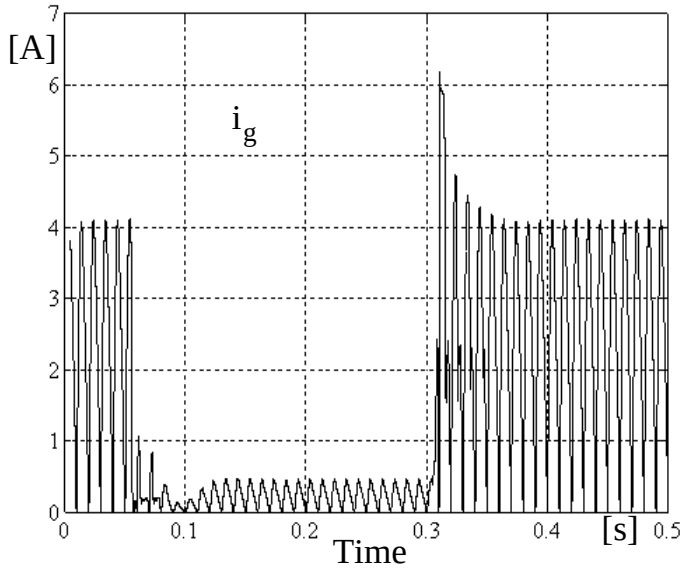
Rectified input current

REGULATION BAND TYPE 2

LOAD STEP CHANGE FROM 100% TO 10% OF RATED POWER AND VICE VERSA (SIMULATED RESULTS)



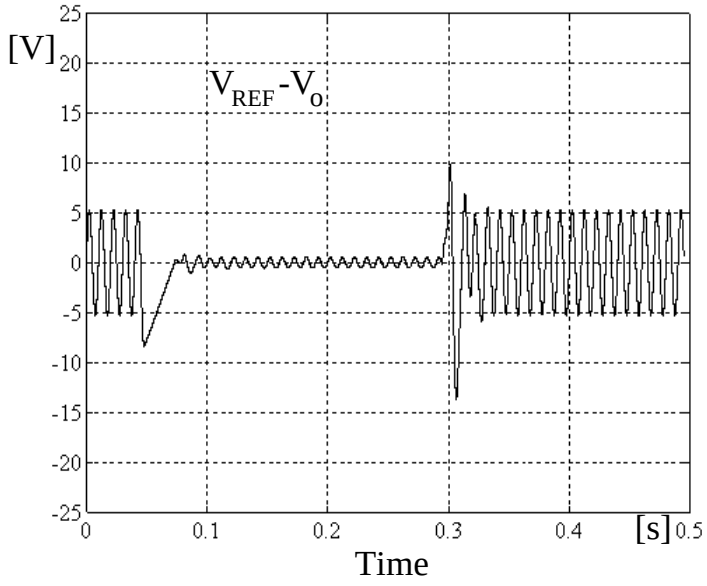
Output voltage error signal



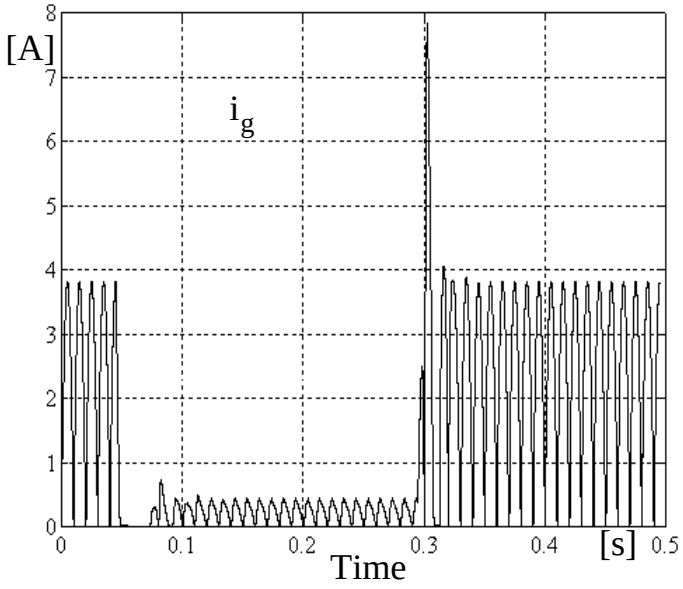
Rectified input current

RIPPLE COMPENSATION

LOAD STEP CHANGE FROM 100% TO 10% OF RATED POWER AND VICE VERSA (SIMULATED RESULTS)



Output voltage error signal



Rectified input current

BASICS OF SOFT-SWITCHING TECHNIQUES

WHY SOFT TRANSITIONS?

- EMI (ELECTRO-MAGNETIC INTERFERENCE) REDUCTION
  - compliance with EMC (Elettro-Magnetic Compatibility) standards
  - input filter size reduction

- INCREASE OF SWITCHING FREQUENCY
  - converter size reduction
  - fast dynamic (high loop bandwidth)

- INCREASE OF EFFICIENCY

SOFT SWITCHING SOLUTIONS

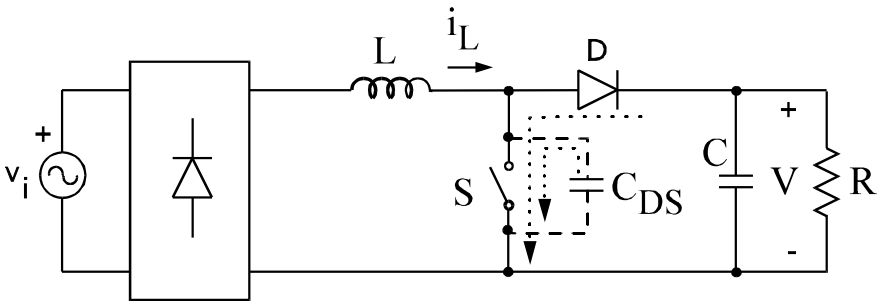
o QUASI-RESONANT OR RESONANT TOPOLOGIES

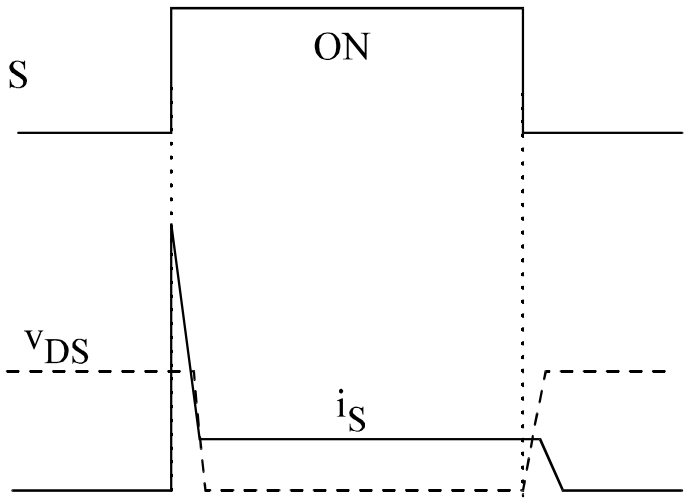
- increased current and/or voltage stresses
- increased conduction losses (resonant components in series with main power path)
- difficulties to maintain soft-switching condition for wide line and load ranges

o AUXILIARY CIRCUIT

- "PWM like" current and voltage waveforms
- need of an auxiliary switch
- little increase of control complexity
- soft-switching condition easily maintained for wide line and load ranges

REVERSE RECOVERY PROBLEM IN BOOST RECTIFIERS

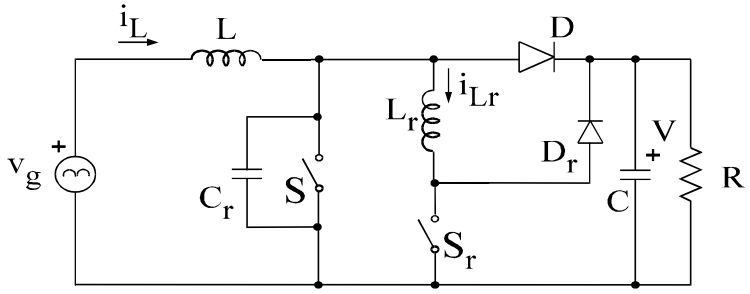




- INCREASED SWITCHING LOSSES
- INCREASED EMI
- INCREASED DEVICE CURRENT STRESSES

ZVT-PWM BOOST CONVERTER - 1

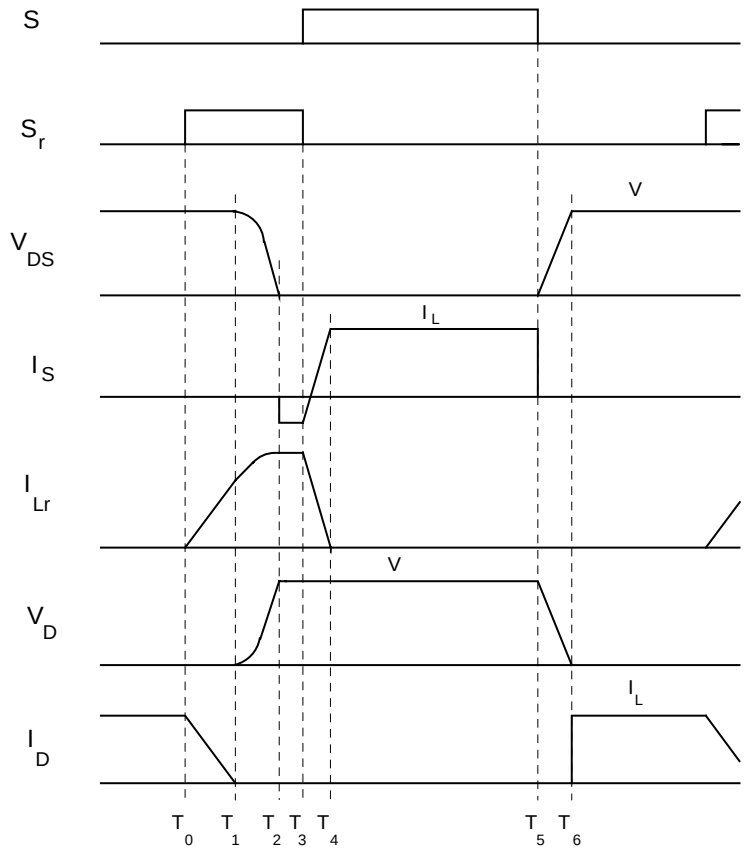
(ZVT: Zero Voltage Transition)



ASSUMPTIONS:

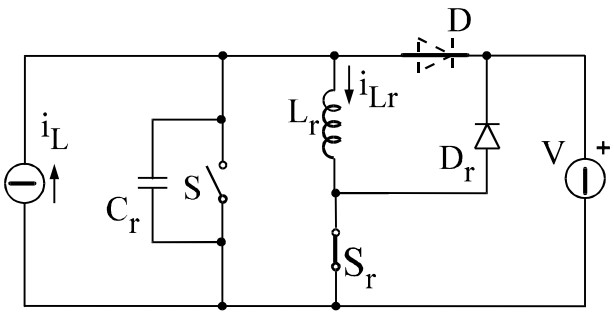
- constant boost inductor current during commutation
- constant output voltage

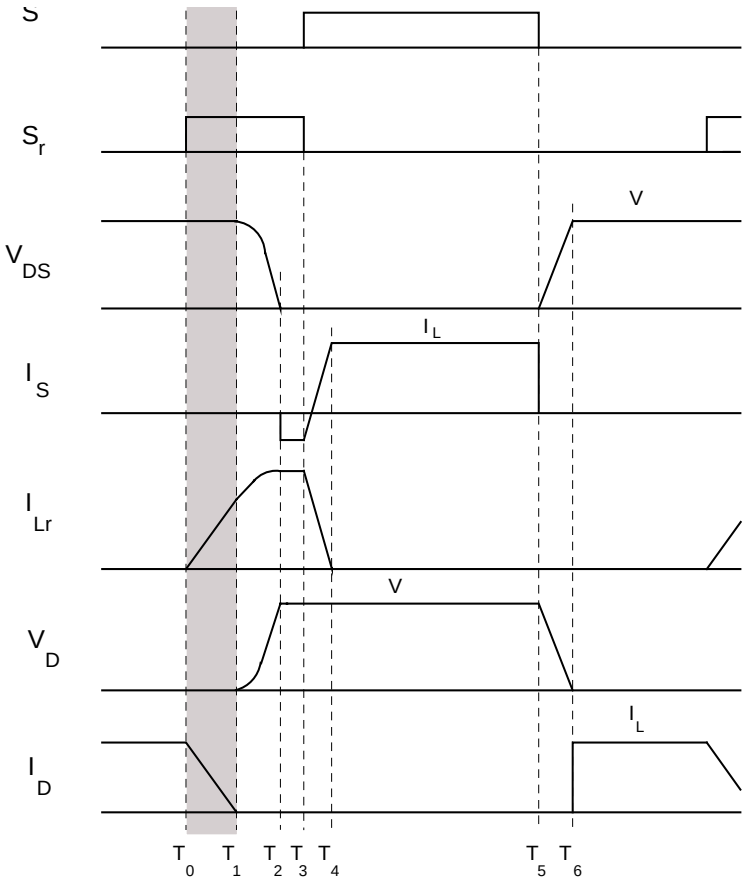
Main waveforms in a switching period



ZVT-PWM BOOST CONVERTER - 1

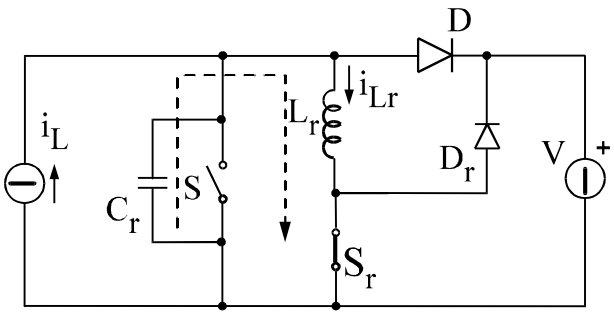
PRINCIPLE OF OPERATION (T_0-T_1)

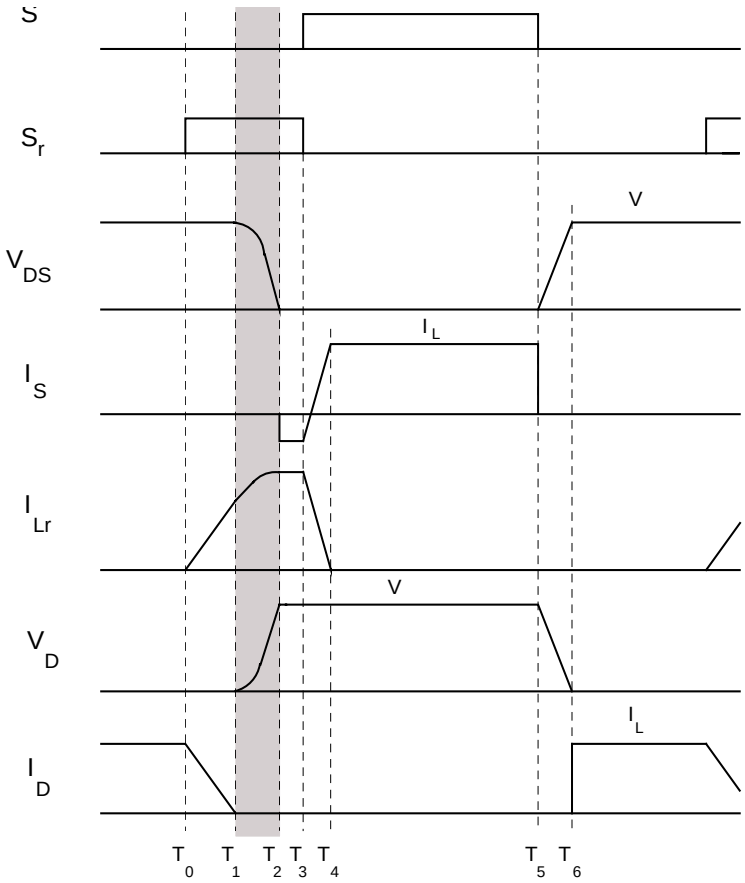




ZVT-PWM BOOST CONVERTER - 1

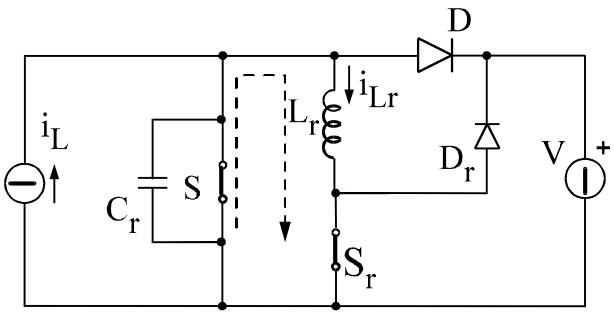
PRINCIPLE OF OPERATION (T_1-T_2)

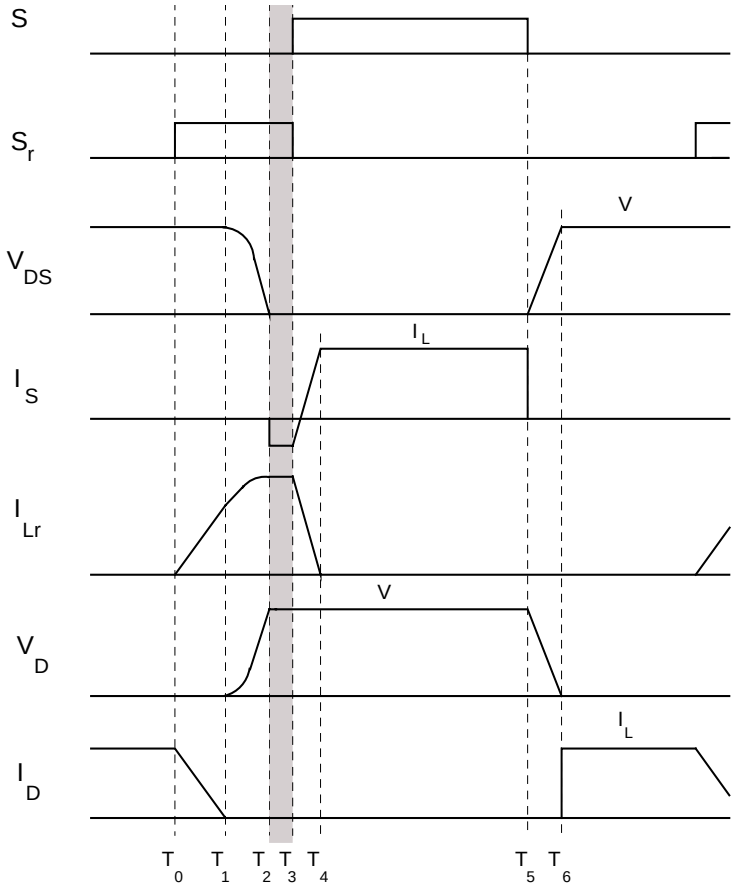




ZVT-PWM BOOST CONVERTER - 1

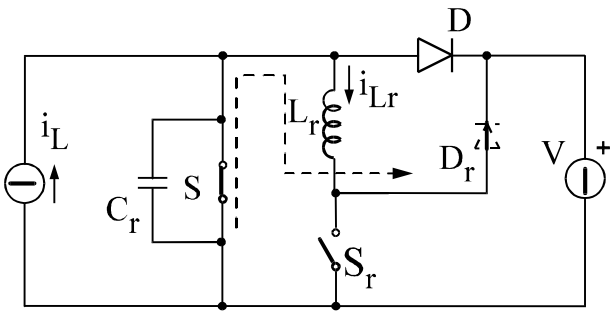
PRINCIPLE OF OPERATION (T_2-T_3)

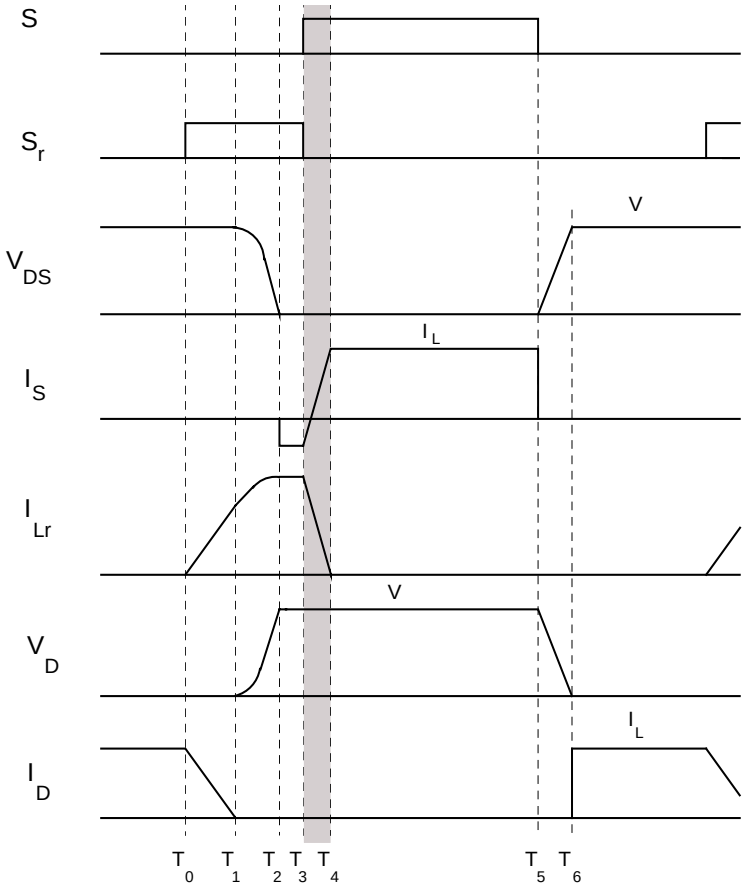




ZVT-PWM BOOST CONVERTER - 1

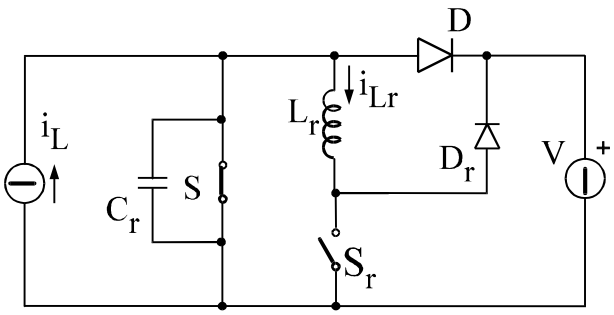
PRINCIPLE OF OPERATION (T_3-T_4)

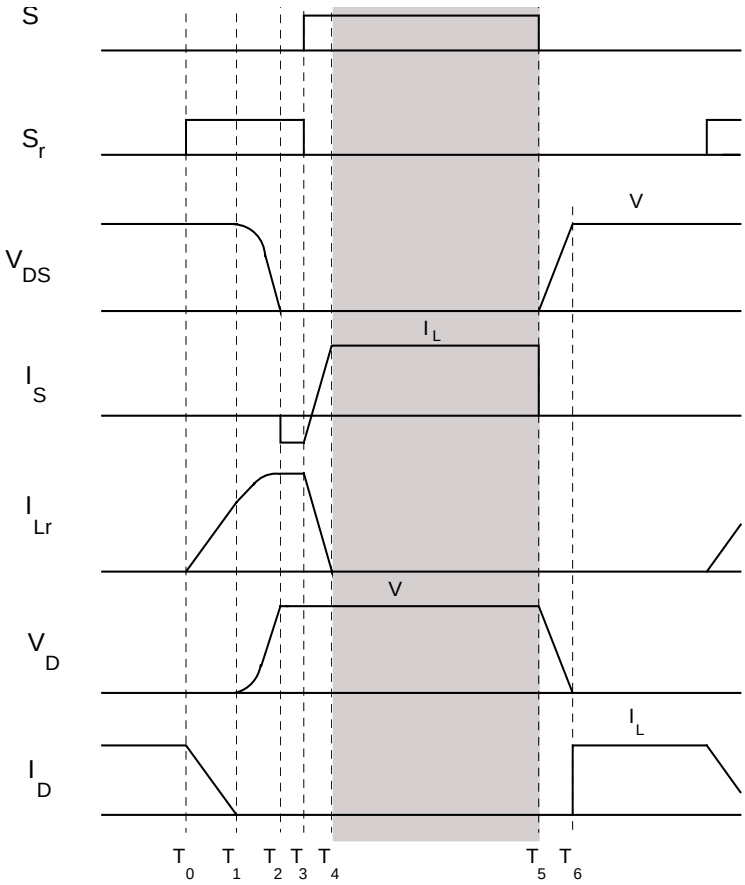




ZVT-PWM BOOST CONVERTER - 1

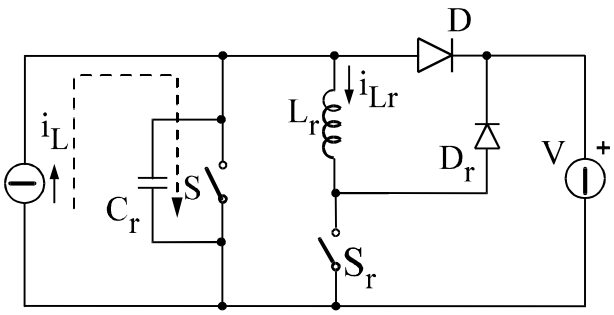
PRINCIPLE OF OPERATION (T_4-T_5)

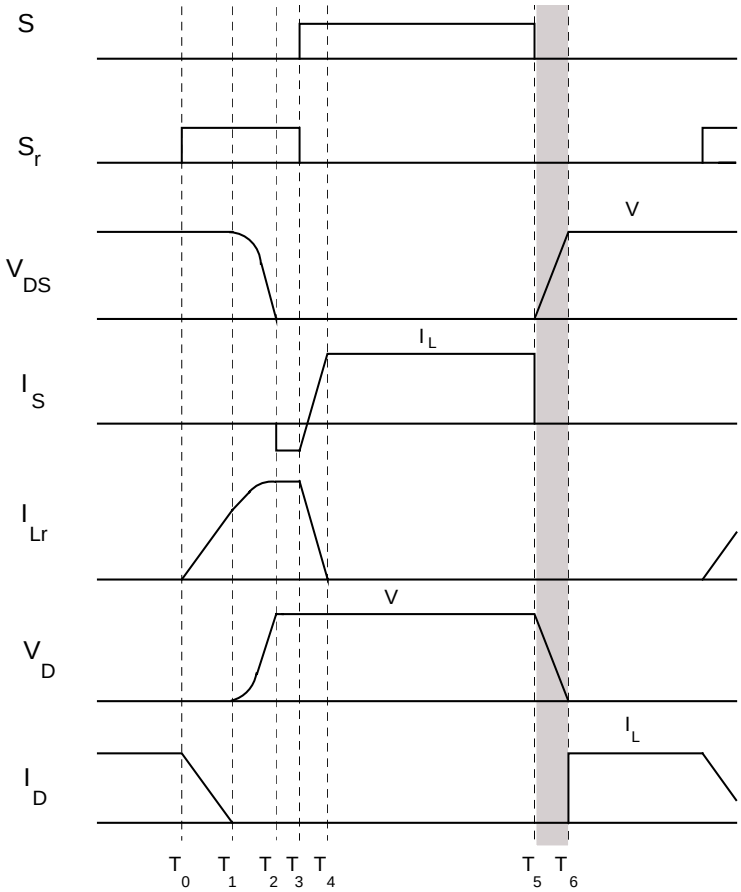




ZVT-PWM BOOST CONVERTER - 1

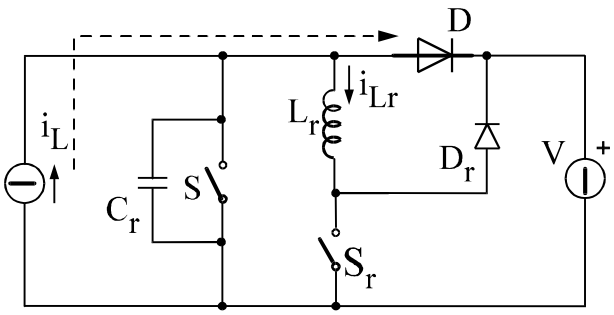
PRINCIPLE OF OPERATION (T_5-T_6)

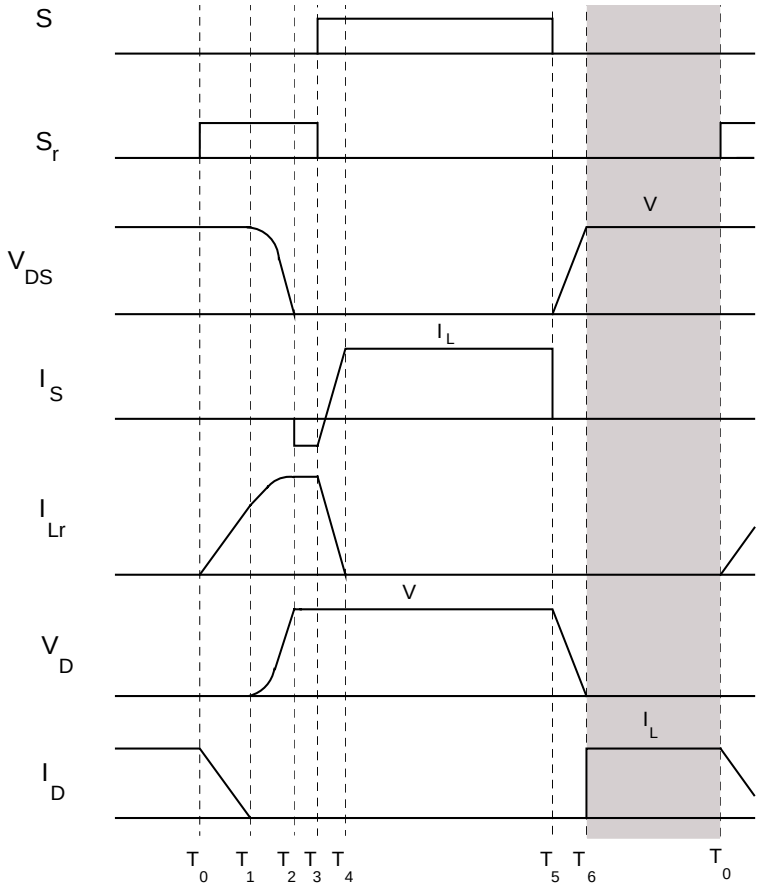




ZVT-PWM BOOST CONVERTER - 1

PRINCIPLE OF OPERATION (T_6-T_0)





ZVT-PWM BOOST CONVERTER - 1

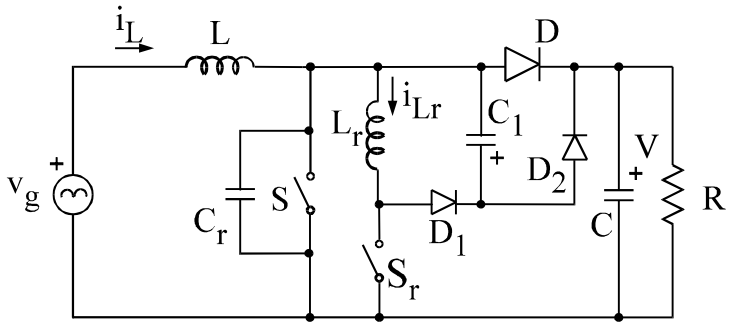
CHARACTERISTICS:

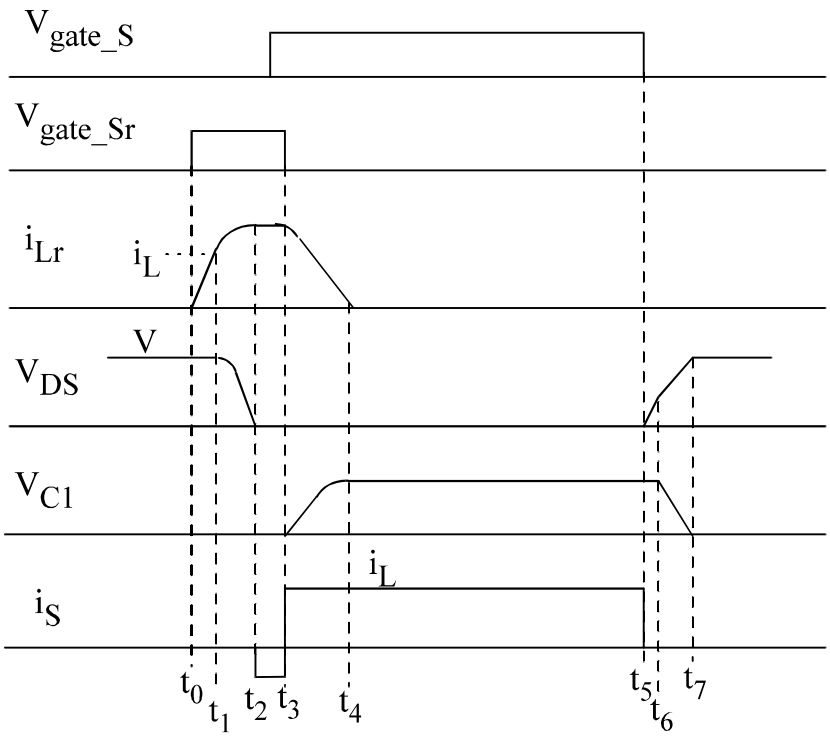
- SOFT-SWITCHING FOR BOTH MAIN SWITCH AND RECTIFIER
- CONSTANT FREQUENCY OPERATION
- HIGH EFFICIENCY
- ZERO-CURRENT TURN ON OF THE AUXILIARY SWITCH
- HARD TURN OFF OF THE AUXILIARY SWITCH

ZVT-PWM BOOST CONVERTER - 2

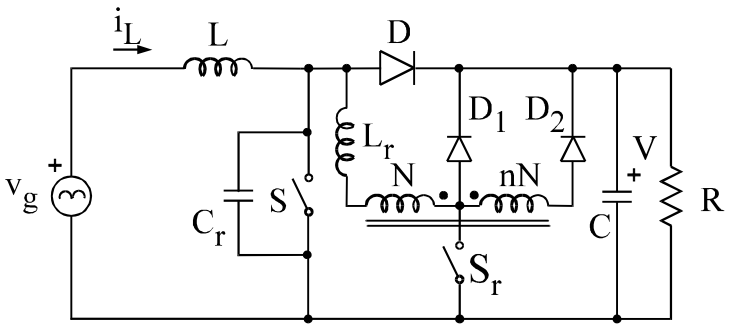
A "flying" capacitor C_1 is added in order to achieve soft turn off of the auxiliary switch.

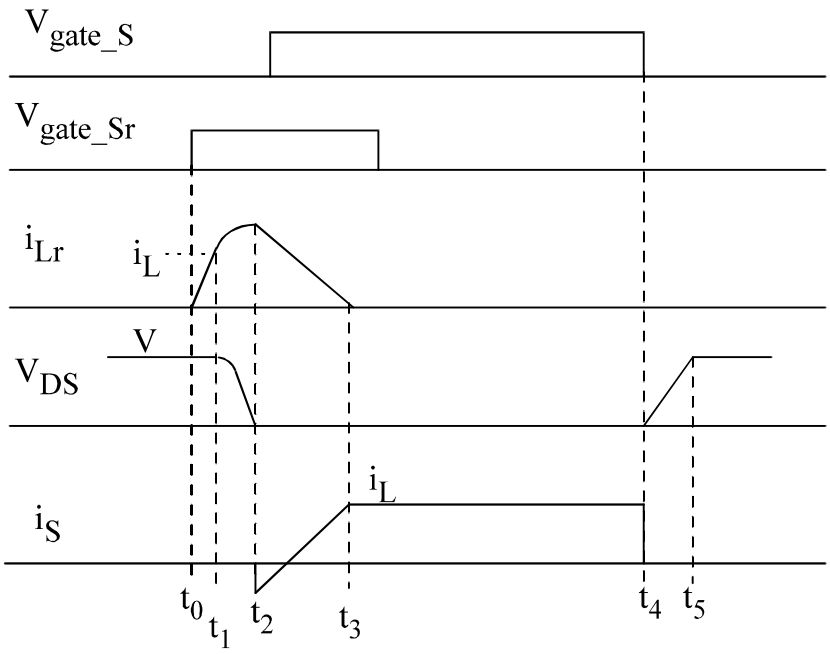
Mode 1 (V_{C1max}<V)





ZVT-PWM BOOST CONVERTER - 3



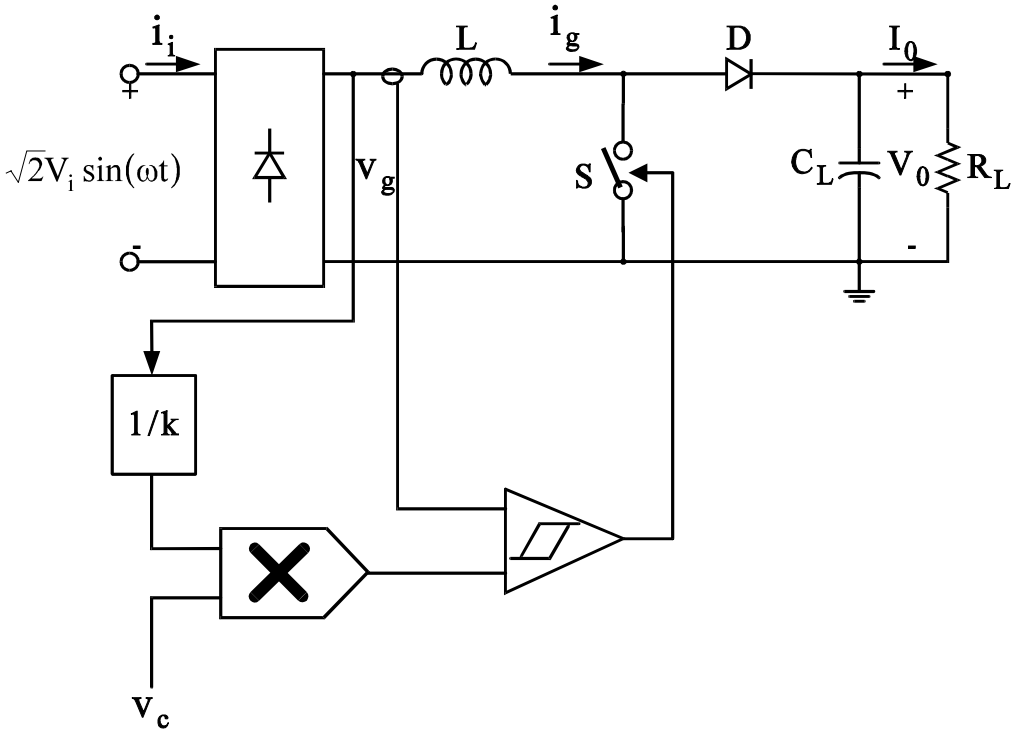


An autotransformer is added in series to the resonant inductor acting like a voltage source to bring the resonant current to zero after the commutation

$\Rightarrow$ S_r turns off at zero current

SMALL-SIGNAL MODELING

SMALL-SIGNAL MODEL OF A PFC OPERATING IN CCM



Power balance: $v_i \cdot i_i = v_0 \cdot i_0$

where $\begin{cases} v_i = V_i + \hat{v}_i \\ i_i = I_i + \hat{i}_i \end{cases}$ (RMS values)

$\begin{cases} v_0 = V_0 + \hat{v}_0 \\ i_0 = I_0 + \hat{i}_0 \end{cases}$

SMALL-SIGNAL MODEL FOR A PFC OPERATING IN CCM

Under PFC conditions the input current is sinusoidal and its RMS value depends on control voltage V_c:

$$i_i = \frac{v_i}{k} \cdot v_c$$

Substituting we obtain:

$$\frac{v_i^2}{k} \cdot v_c = v_0 \cdot i_0$$

After perturbation and linearization (small-signal approximation):

$$\hat{i}_0 = \frac{2V_i V_c}{kV_0} \cdot \hat{v}_i + \frac{V_i^2}{kV_0} \cdot \hat{v}_c - \frac{I_0}{V_0} \cdot \hat{v}_0$$

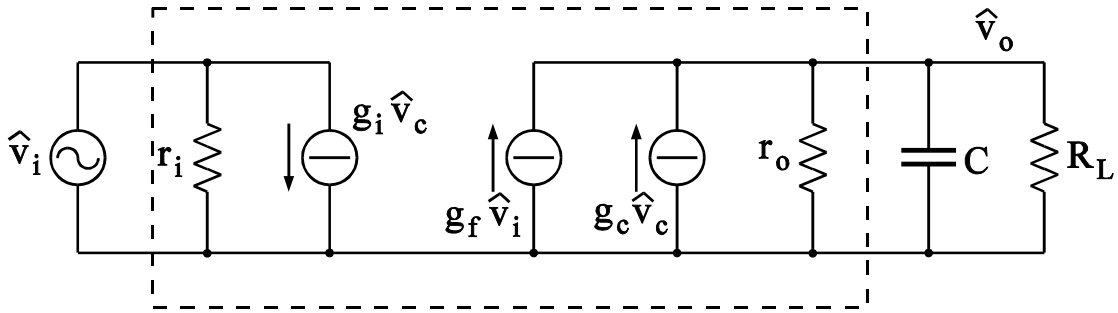
$$\hat{i}_0 = \frac{2M}{r_0} \cdot \hat{v}_i + \frac{V_i}{kM} \cdot \hat{v}_c - \frac{1}{r_0} \cdot \hat{v}_0$$

where $M = \frac{V_0}{V_i}$, $r_0 = \frac{V_0}{I_0}$

SMALL-SIGNAL MODEL FOR A PFC OPERATING IN CCM

In the same way, from the power balance, we obtain:

$$\hat{i}_i = \frac{V_i}{k} \cdot \hat{v}_c + \frac{M^2}{r_0} \cdot \hat{v}_i$$



M	r_i	g_i	r_0	g_f	g_c
$\frac{V_0}{V_i}$	$\frac{r_o}{M^2}$	$\frac{V_i}{k}$	$\frac{V_0}{I_0}$	$\frac{2M}{r_o}$	$\frac{V_i}{kM}$

SMALL-SIGNAL MODEL FOR A PFC OPERATING IN CCM

TRANSFER FUNCTION BETWEEN CONTROL VOLTAGE AND OUTPUT VOLTAGE

$$G_{vc}(s) = \frac{\hat{v}_0}{\hat{v}_c} = g_c \cdot \frac{r_p}{1 + sCr_p}$$

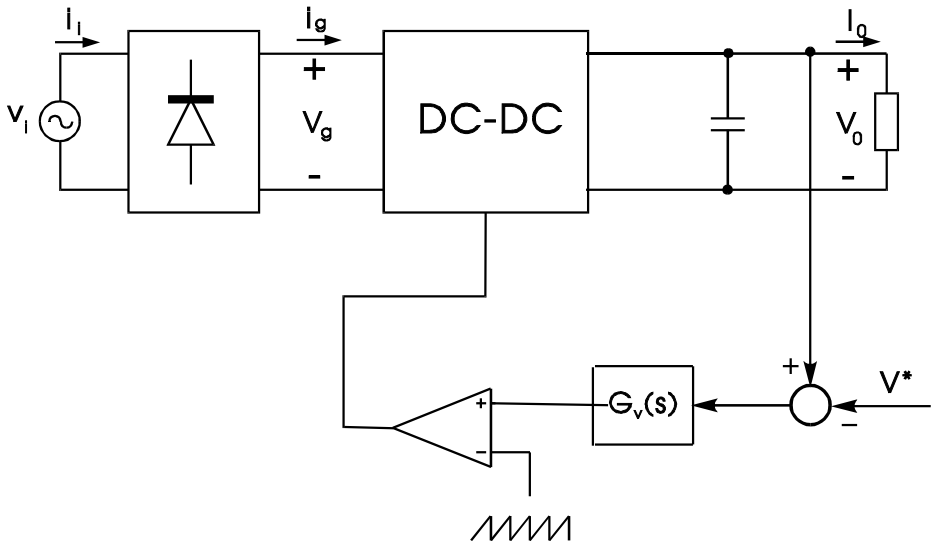
$$r_p = \frac{r_0 \cdot R_L}{r_0 + R_L}$$

$r_p = R_L/2$ resistive load

$r_p = R_L$ constant current load

$r_p = \infty$ constant power load

SMALL-SIGNAL MODEL FOR A PFC OPERATING IN DCM (FLYBACK, CUK, SEPIC)



Power balance: $v_i \cdot i_i = v_0 \cdot i_0$

where $\begin{cases} v_i = V_i + \hat{v}_i \\ i_i = I_i + \hat{i}_i \end{cases}$ (RMS values)

$\begin{cases} v_0 = V_0 + \hat{v}_0 \\ i_0 = I_0 + \hat{i}_0 \end{cases}$

SMALL-SIGNAL MODEL FOR A PFC OPERATING IN DCM

Under PFC conditions the input current is sinusoidal and its RMS value depends on duty-cycle δ:

$$i_i = \frac{T_s v_i}{2L_{eq}} \cdot \delta^2$$

where L_{eq} depends on converter topology.
Substituting we obtain:

$$\frac{v_i^2 T_s}{2L_{eq}} \cdot \delta^2 = v_0 \cdot i_0$$

After perturbation and linearization (small-signal approximation):

$$\hat{i}_0 = \frac{2V_i Y_i D^2}{V_0} \cdot \hat{v}_i + \frac{2V_i^2 Y_i D}{V_0} \cdot \hat{\delta} - \frac{I_0}{V_0} \cdot \hat{v}_0$$

where $Y_i = \frac{T_s}{2L_{eq}}$

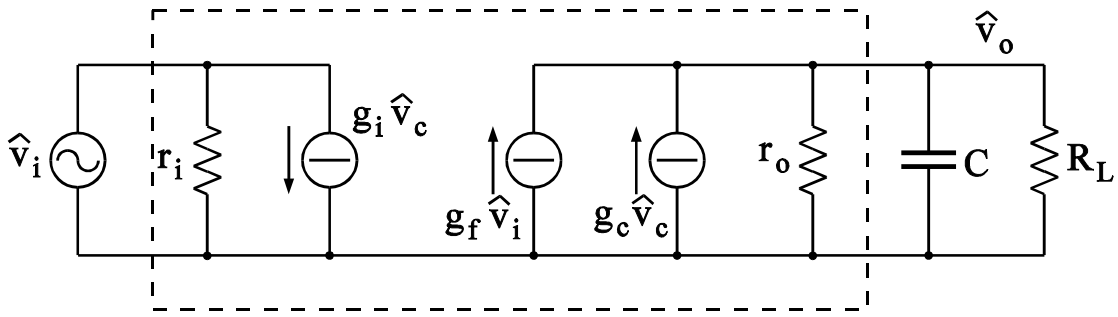
SMALL-SIGNAL MODEL FOR A PFC OPERATING IN DCM

$$\hat{i}_0 = \frac{2Y_i D^2}{M} \cdot \hat{v}_i + \frac{2V_i Y_i D}{M} \cdot \hat{\delta} - \frac{1}{r_0} \cdot \hat{v}_0$$

where $M = \frac{V_0}{V_i}$, $r_0 = \frac{V_0}{I_0}$

In the same way, from the power balance, we obtain:

$$\hat{i}_i = 2V_i Y_i D \cdot \hat{\delta} + D^2 Y_i \cdot \hat{v}_i$$



SMALL-SIGNAL MODEL FOR A PFC OPERATING IN DCM

MODEL PARAMETERS

M	r_i	g_i	r_0	g_f	g_c
$\frac{V_0}{V_i}$	$\frac{1}{D^2 Y_i}$	$2DV_iY_i$	$\frac{V_0}{I_0}$	$\frac{2Y_iD^2}{M}$	$\frac{2V_iY_iD}{M}$

	FLYBACK	CUK	SEPIC
L_{eq}	L	$\frac{L_1 \cdot L_2}{n^2 L_1 + L_2}$	$\frac{L_1 \cdot L_2}{L_1 + L_2}$

n=transformer turns ratio (N_2/N_1)

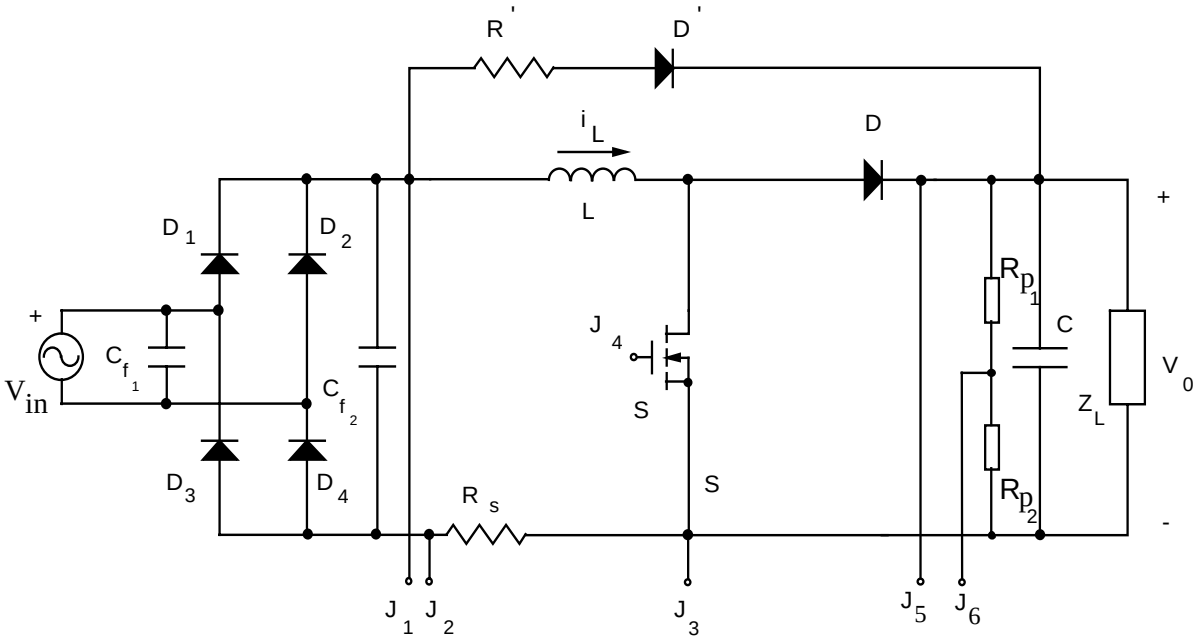
TRANSFER FUNCTION BETWEEN DUTY-CYCLE AND OUTPUT VOLTAGE

$$G_v(s) = \frac{\hat{v}_0}{\hat{\delta}} = g_c \cdot \frac{r_p}{1 + sCr_p}$$

$$r_p = \frac{r_0 \cdot R_L}{r_0 + R_L}$$

DESIGN OF BOOST PFC OPERATING IN CCM WITH AVERAGE CURRENT MODE CONTROL

POWER STAGE SCHEME



CHARACTERISTICS:

Input voltage:	V_{in} = 90-260V_{RMS}
Output voltage:	V_o = 380V
Output power:	P_o = 600W
Switching frequency:	f_S = 70kHz

POWER STAGE DESIGN

1) Inductor peak current (average value in a switching period)

$$P_o = \eta \cdot P_g$$

where η is converter efficiency

$$\eta \cdot \frac{\hat{I}_L \cdot \hat{V}_g}{2} = P_o \qquad \Rightarrow \qquad \hat{I}_L = \frac{2P_o}{\eta \hat{V}_g} \tag{1}$$

Worst case: minimum input voltage

$$\hat{I}_L = \frac{2 \cdot 600}{0.95 \cdot \sqrt{2} \cdot 90} = 9.92\,A$$

POWER STAGE DESIGN

2) Input inductor value

Duty-cycle in CCM:

$$\delta(\vartheta) = 1 - \frac{V_g(\vartheta)}{V_o}, \delta = \frac{t_{on}}{T_s}; \vartheta = \omega_i t \qquad (2)$$

Peak-to-peak input current ripple:

$$\Delta i_L(\vartheta) = \frac{V_g(\vartheta)}{L} \cdot t_{on} = \frac{V_g(\vartheta)}{f_s \cdot L} \cdot \delta(\vartheta) \qquad (3)$$

The maximum ripple occurs at half the input voltage peak. From the allowed ripple the input inductor value is found.

(example: relative ripple = 30% $\Rightarrow$ L = 0.46 mH.

POWER STAGE DESIGN

3) Output capacitor value

$$C = \frac{I_o}{\omega_i \Delta V_o} \tag{4}$$

where ΔV_o is the desired peak-to-peak voltage ripple and I_o is the output current.
(Example:

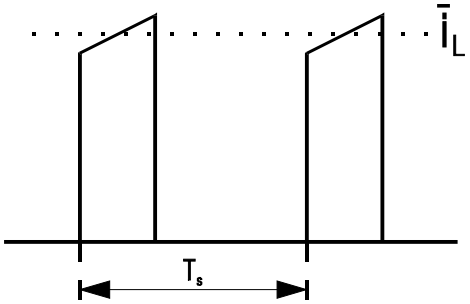
relative ripple <5% $\Longrightarrow$ C > 260 μF, we use C=470μF)

4) Switch peak current

$$\hat{i}_s = \hat{I}_L + \frac{\Delta i_L (\pi/2)}{2} = 10.9\text{A} \tag{5}$$

POWER STAGE DESIGN

5) Switch RMS current



RMS current is determined by first averaging the switch current over a switching period and second averaging over the line period. Neglecting the inductor current ripple we obtain:

$$\frac{I_{s,rms}}{I_o} \cong 2M\sqrt{\frac{1}{2} - \frac{1}{M}\cdot\frac{4}{3\pi}} \qquad (6)$$

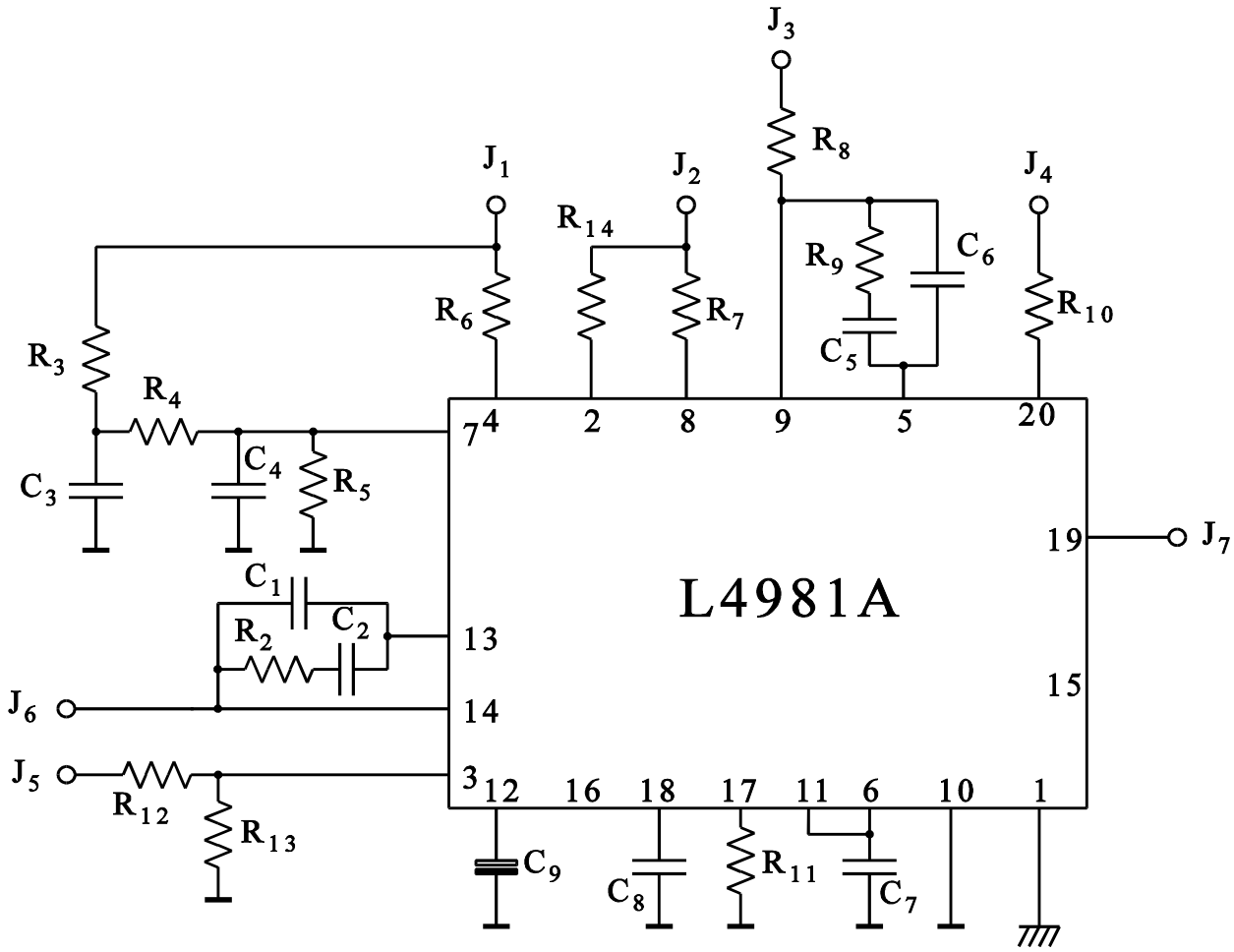
where $M = \frac{V_o}{V_g}$ is voltage conversion ratio

Considering the minimum input voltage we obtain: $I_{s,rms} = 5.63A.$

6) Freewheeling diode peak current (average value)

$$\hat{I}_{D,avg} = 2 \cdot I_o = 3.16A \qquad (7)$$

CONTROL STAGE DESIGN



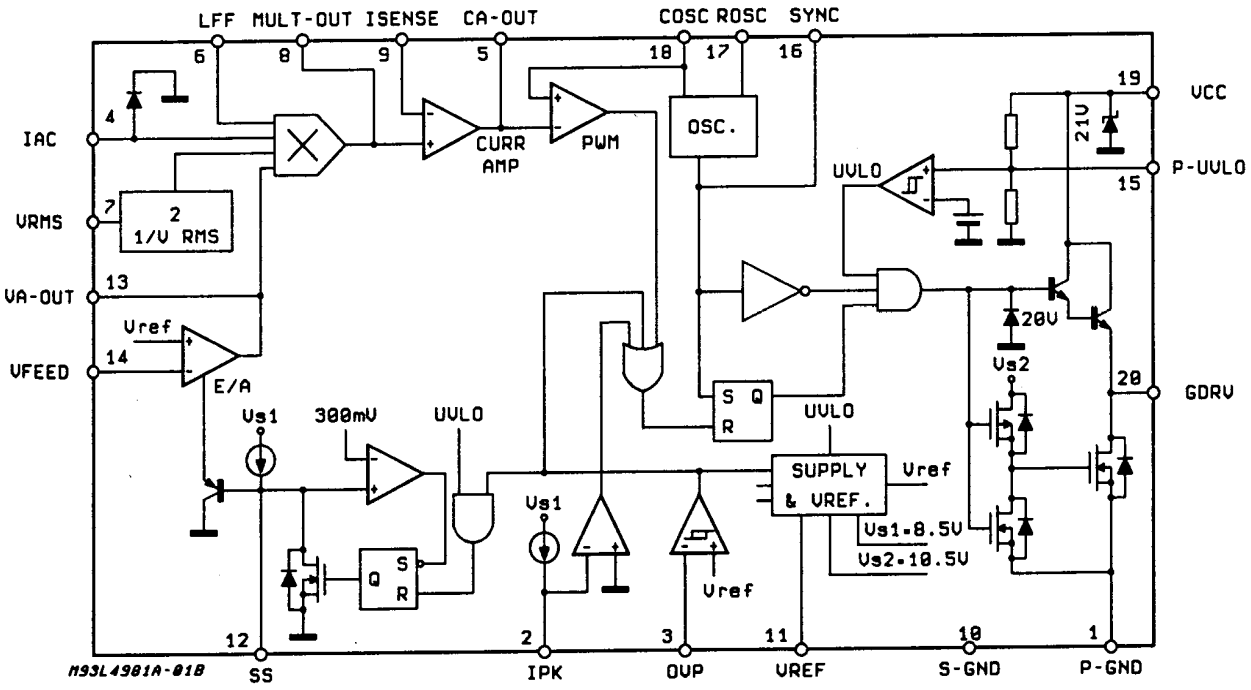
IC: SGS-THOMSON L4981A

COMPONENT VALUES

V_{cc} = 18V	R_7 = 3.3 kΩ	R_{13} = 18 kΩ	C_4 = 100 nF
R_2 = 150 kΩ	R_8 = 3.3 kΩ	R_{14} = 5.6kΩ	C_5 = 1 nF
R_3 = 1 MΩ	R_9 = 47 kΩ		C_6 = 68 pF
R_4 = 560 kΩ	R_{10} = 33 Ω	C_1 = 15 nF	C_7 = 10 µF
R_5 = 33 kΩ	R_{11} = 33 kΩ	C_2 = 220 nF	C_8 = 1 nF
R_6 = 1.2 MΩ	R_{12} = 1.5 MΩ	C_3 = 220 nF	C_9 = 10 µF

CONTROL STAGE DESIGN

IC: SGS-THOMSON L4981A



CONTROL STAGE DESIGN

1) Shunt resistance R_S*:*

Choosing R_S = 0.054Ω the power loss is:

$$P_{R_S} = R_S \cdot \frac{\hat{I}_L^2}{2} = 2.65W \tag{8}$$

2) Switching frequency:

C_8 and R_{11} determine the switching frequency:

$$f_s = \frac{2.4}{C_8 \cdot R_{11}}, \quad \text{hertz} \tag{9}$$

Choosing C_8=1nF gives R_{11}=33kΩ

3 Reference current I_{AC}*:*

$$I_{AC} = \frac{\hat{V}_g}{R_6} \tag{10}$$

The suggested value for R_6 is 1.2MΩ. Correspondingly, I_{AC} is between 106μA at minimum line voltage and 306μA at maximum line voltage.

CONTROL STAGE DESIGN

4) Feedforward voltage V_{RMS}:

R_3, C_3, R_4, R_5, C_4 form a low pass filter which must give at pin 7 a DC voltage between 1.5V and 6.5V. Suggested values are: R_3=1MΩ, R_4=560kΩ, R_5=33kΩ, C_3=220nF, C_4=100nF:

$$V_{RMS} = \frac{R_5}{R_3 + R_4 + R_5} \cdot \frac{2}{\pi} \cdot \hat{V}_g = \alpha \cdot \hat{V}_g = 1.68 \div 4.85 V \qquad (11)$$

This low-pass filter must give a good attenuation at twice the line frequency.

5) Peak current limiter:

We choose $I_{pk,lim}$=11A:

$$I_{pk,lim} = 100\mu A \cdot \frac{R_{14}}{R_S} \qquad (12)$$

from which R_{14}=5.6kΩ.

CONTROL STAGE DESIGN

6) R_7 *and* R_8 *values:*

If the current error amplifier has enough gain at line frequency we have:

$$R_S \cdot I_L = R_7 \cdot I_{MULT-OUT} \tag{13}$$

where $I_{MULT-OUT}$ is the multiplier output current, which is related to the output voltage of the voltage error amplifier V_{A-OUT} by:

$$I_{MULT-OUT} = I_{AC} \cdot \frac{V_{A-OUT} - 1.28}{V_{RMS}^2} \tag{14}$$

which is valid if pin 6 (V_{LFF}) is connected to pin 11 (V_{REF}).

Imposing that the maximum input current occurs with a voltage V_{A-OUT}=5V, we obtain R_7=R_8=3.3kΩ.

CONTROL STAGE DESIGN

7) Over voltage protection:

$$V_{o,max} = V_{REF} \cdot \left(1 + \frac{R_{12}}{R_{13}}\right) \quad (15)$$

Choosing R_{12}=1.5MΩ and R_{13}=18kΩ gives $V_{o,max}$=425V.

8) Soft-start:

Connecting a capacitor between pin 12 and ground a ramp voltage is generated which causes the duty-cycle to vary from minimum to nominal value.

Suggested value: C_9 = 10μF.

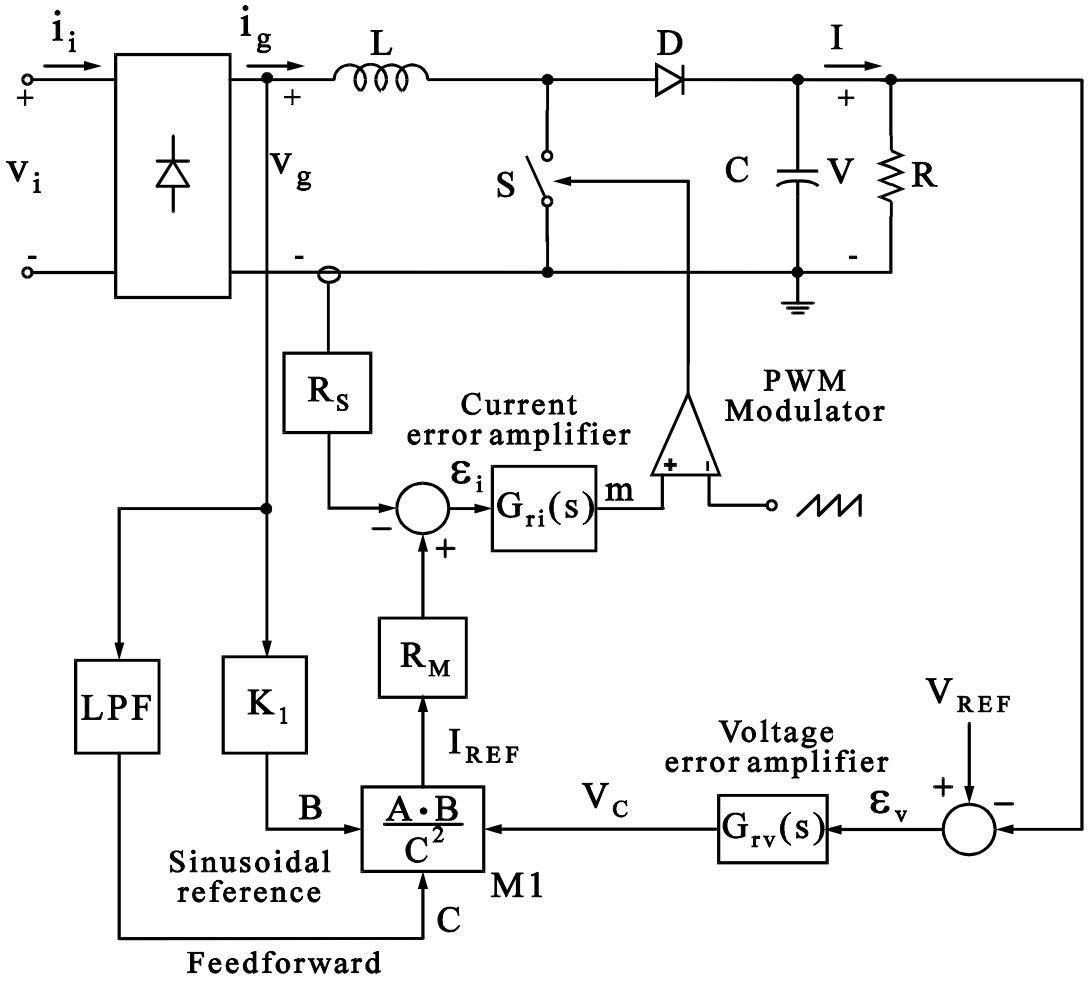
9) Feedback signal divider:

$$V_{REF} = V_o \cdot \frac{R_{p2}}{R_{p1} + R_{p2}} \quad (16)$$

R_{p1}=1MΩ e R_{p2}=12kΩ + 4.7kΩ trimmer.

As suggested a filter capacitor C_7 = 10μF is connected between pin 11 (V_{REF}) and ground.

CURRENT REGULATOR DESIGN



Approximated power stage transfer function (between duty-cycle and input current) for frequency above the output filter corner frequency:

$$G_i(s) = \frac{i_g(s)}{d(s)} = \frac{V_o}{sL} \qquad (17)$$

CURRENT REGULATOR DESIGN

The current loop transfer function is:

$$T_i(s) = \frac{V_o}{sL} \cdot \frac{1}{V_{osc}} \cdot R_s \cdot G_{ri}(s) \tag{18}$$

where, V_{osc} = 5V is the amplitude of the internal ramp of the PWM generator.

Current error amplifier: $$G_{ri}(s) = \frac{m(s)}{\varepsilon_i(s)} = \frac{\omega_{ri}}{s} \cdot \frac{(1 + s\tau_{zi})}{(1 + s\tau_{pi})} \tag{19}$$

where

$$\omega_{ri} = \frac{1}{R_8(C_5 + C_6)} \approx \frac{1}{R_8 C_5} \text{ if } C_5 >> C_6 \tag{20}$$

$$\tau_{zi} = R_9 \cdot C_5 \tag{21}$$

$$\tau_{pi} = R_9 \cdot \frac{C_5 \cdot C_6}{C_5 + C_6} \approx R_9 \cdot C_6 \quad \text{if } C_5 >> C_6 \tag{22}$$

CURRENT REGULATOR DESIGN

If $f_{zi} < f_c < f_{pi}$ where f_c is the crossover frequency, then:

$$\left|G_{ri}(j\omega_c)\right| \approx \frac{R_9}{R_8} \tag{23}$$

$$T_i(j\omega_c) = 1 \Rightarrow \frac{R_9}{R_8} = \frac{2\pi f_c \cdot L \cdot V_{osc}}{R_s \cdot V_o} \tag{24}$$

As far as the phase is concerned:

$$\angle T_i(j\omega_c) = -90^\circ - 90^\circ + \text{arctg}\left(\frac{f_c}{f_{zi}}\right) - \text{arctg}\left(\frac{f_c}{f_{pi}}\right) = m_\varphi - 180^\circ \tag{25}$$

where m_φ is the desired phase margin.

Given f_c , the phase margin and choosing $f_S/2<f_{pi}<f_S$ so as to attenuate the high-frequency ripple R_9, C_5 and C_6 values are obtained.

Example: f_c = 15 kHz, f_{pi} = 50 kHz and m_φ = 60° $\Rightarrow$ f_{zi} = 3.5kHz, R_9=47kΩ, C_5=1nF, C_6=68pF.

VOLTAGE REGULATOR DESIGN

Transfer function between control voltage and output voltage:

$$G_v(s) = \frac{V_0(s)}{V_c(s)} = g_c \cdot \frac{r_p}{1 + sCr_p} \tag{26}$$

where,

$$r_p = \frac{r_o \cdot Z_L}{r_o + Z_L}, \quad g_c = \frac{V_{g,rms}}{k \cdot M}, \quad r_o = \frac{V_o}{I_o}, \quad M = \frac{V_o}{V_{g,rms}} \tag{27}$$

$Z_L = R_L = r_o$ resistive load
$Z_L = ¥$ constant current load
$Z_L = - R_L$ constant power load

and k is defined by the relation:

$$I_{g,rms} = \frac{V_{g,rms}}{k} \cdot v_c \tag{28}$$

In the L4981A controller, feedforward term V_{RMS} eliminates the dependence of gain g_c from input voltage.

VOLTAGE REGULATOR DESIGN

From eqs. (13-14) we can write (R_M=R_7):

$$I_{g,RMS} = \frac{R_7}{R_S} \cdot I_{MULT-OUT} = \frac{R_7}{R_S} \cdot \frac{V_{g,RMS}}{R_6} \cdot \frac{V_{A-OUT} - 1.28}{V_{RMS}^2} = \frac{R_7}{R_S} \cdot \frac{V_{g,RMS}}{R_6} \cdot \frac{V_{A-OUT} - 1.28}{2\alpha^2 V_{g,RMS}^2} \quad (29)$$

which corresponds to (28) if:

$$k = 2R_6 \cdot \frac{R_S}{R_7} \cdot \left(\frac{2}{\pi} \cdot \frac{R_5}{R_3 + R_4 + R_5} \right)^2 \cdot V_{g,RMS}^2 \quad (30)$$

VOLTAGE REGULATOR DESIGN

The voltage regulator transfer function is:

$$G_{rv}(s)=\frac{V_C(s)}{\varepsilon_v(s)}=\frac{\omega_{rv}}{s}\cdot\frac{(1+\tau_{zv})}{(1+s\tau_{pv})} \qquad (31)$$

where

$$\omega_{rv}=\frac{R_{p2}}{R_{p1}+R_{p2}}\cdot\frac{1}{C_1+C_2}\cdot\frac{1}{R_1}\approx\frac{V_{REF}}{V_o}\cdot\frac{1}{C_2}\cdot\frac{1}{R_1} \quad (C_2>>C_1) \qquad (32)$$

with $R_1=R_{p1}||R_{p2}$

$$\tau_{zv}=R_2\cdot C_2 \qquad (33)$$

$$\tau_{pv}=R_2\cdot(C_1//C_2)\approx R_2\cdot C_1 \text{ se} C_2>>C_1 \qquad (34)$$

Considering a crossover frequency higher than the power stage pole we have:

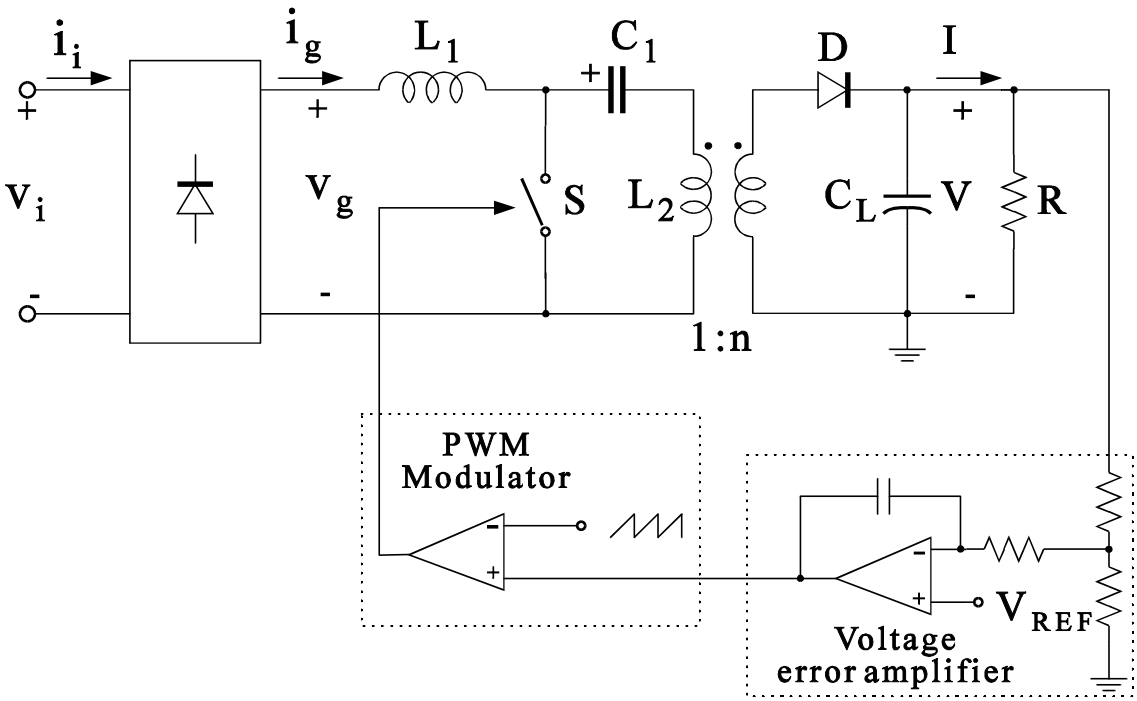
$$\left|\frac{g_c}{j\omega_c C}\cdot\omega_{rv}\tau_{zv}\right|=1 \qquad (35)$$

Choosing f_c = 10÷20 Hz, $f_i<f_{pv}<2f_i$ and a suitable phase margin, the regulator parameters can be calculated.

Example: f_c = 20Hz, f_{pv} = 70Hz and m_φ = 60° $\Rightarrow$ f_{zv} = 5Hz, R_2=150kΩ,C_1=15nF, C_2=220nF.

DESIGN OF A SEPIC PFC OPERATING IN DCM

POWER STAGE SCHEME



PROTOTYPE PARAMETERS

V_g = 220 V_{rms} ± 20%	V = 36 V	P = 100W	f_S = 100 kHz
L_2 = 74 µH	C_1 = 0.68 µF	C_2 = 10 µF	n = 0.5

SEPIC MAIN EQUATIONS

1) *Operation as dc/dc converter.*

The voltage conversion ratio is:

$$M = \frac{V}{V_g} = \frac{I_g}{I} = n \cdot \frac{D}{1-D} \qquad \text{(CCM)}$$

$$M = \frac{V}{V_g} = \frac{I_g}{I} = \frac{D}{\sqrt{K}} \quad \text{(DCM)}$$

where $n=N_2/N_1$ is transformer turns ratio, D is duty-cycle and parameter K is given by:

$$K = \frac{2L_e}{RT_s}, \text{ with} \qquad L_e = \frac{L_1 L_2}{L_1 + L_2}$$

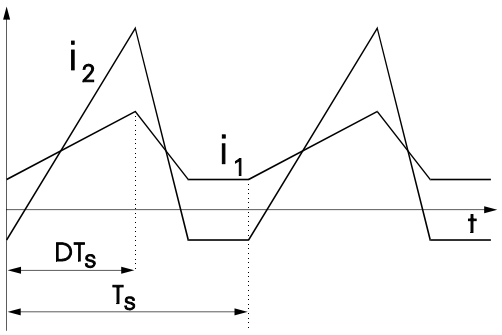
In the above equations T_s is the switching period and L_2 is the transformer magnetizing inductance.

Critical parameter:

$$K_{crit} = \frac{(1-D)^2}{n^2} = \frac{1}{(n+M)^2} \begin{cases} K > K_{crit} \Rightarrow \text{CCM} \\ K < K_{crit} \Rightarrow \text{DCM} \end{cases}$$

SEPIC MAIN EQUATIONS

Average inductor current I_2 : $I_2 = n \cdot i_D = n \cdot I$



Inductor current waveforms in DICM

2) Operation as a rectifier.

When operating as a rectifier, the dc input voltage V_g is substituted by the rectified line voltage:

$$v_g(\theta) = V_g \cdot |\sin(\theta)|$$

where $\theta = \omega_i t$. Consequently, the voltage conversion ratio becomes:

$$m(\theta) = \frac{V}{v_g(\theta)} = \frac{M}{|\sin(\theta)|}$$

where $M=V/V_g$.

SEPIC MAIN EQUATIONS

Under power factor correction conditions:

$$i_2(\theta) = n \cdot i_D(\theta) = n \cdot 2I\sin^2(\theta)$$

The apparent load r(q) seen at the secondary side of the transformer is given by:

$$r(\theta) = \frac{V}{i_D(\theta)} = \frac{R}{2\sin^2(\theta)}$$

Thus the parameter k becomes function of angle q

$$k(\theta) = \frac{2L_e}{r(\theta)T_s} = 2K_a\sin^2(\theta), K_a = \frac{2L_e}{RT_s}$$

$$k_{crit}(\theta) = \frac{\sin^2(\theta)}{\left(M + n \cdot \left|\sin(\theta)\right|\right)^2}$$

For the converter to operate in DCM the following condition must be satisfied:

$$K_a < \frac{1}{2\left(M + n \cdot \left|\sin(\theta)\right|\right)^2}$$

SEPIC MAIN EQUATIONS

The average current drawn by the converter, at constant duty-cycle and switching frequency, is sinusoidal and in phase with the line voltage and is given by

$$i_g(\theta) = \frac{D^2 T_s}{2L_e} \cdot v_g(\theta) = \frac{v_g(\theta)}{R_{em}}$$

where,

$R_{em} = \frac{2L_e}{D^2 T_s}$ is the emulated resistance.

The converter duty-cycle results:

$$D = M \cdot \sqrt{2K_a}$$

POWER STAGE DESIGN

INPUT DATA:

- minimum and maximum input voltage peak value V_{gmin}, V_{gmax};
- output voltage V;
- output power P;
- switching frequency f_s;
- initial value for transformer turns ratio n.

POWER STAGE DESIGN

DESIGN PROCEDURE:

- calculate minimum and maximum voltage conversion ratio M_{min}, M_{max}
- evaluate K_a for $\pi = \pi/2$ and M_{max} (minimum line voltage)

$$K_a = \alpha \cdot \frac{1}{2(M_{max} + n)^2}, \alpha = 0.9 \div 0.95$$

- find the value of inductance L_e from K_a definition
- find the value of duty-cycle D;
- calculate the value of inductances L_1 and L_2 from L_e and the desired input current ripple
- calculate device current and voltage stresses as well as peak inductor currents;
- repeat the procedure for different values of transformer turns ratio;
- choose the solution which best meets device ratings.

POWER STAGE DESIGN

NOTE:

particular attention must be given to the selection of capacitor C_1. Three constrains must be taken into account:

- voltage u_1 must follow the input voltage shape without distorsion
- its voltage ripple must be as low as possible
- C_1 should not cause low-frequency oscillations with inductors L_1 and L_2.