Power Factor Correction Using *TOPSwitch*®

Design Note DN-7

The *TOPSwitch* family of Three-Terminal PWM Switch Integrated Circuits implements a new, fixed frequency Power Factor Correction circuit using as few as 17 components. Output power levels up to 150 Watts are possible with a simple configuration that operates at constant frequency and eliminates current sensing.

Efficiencies up to 93% have been achieved using *TOPSwitch*. Integrating start-up bias and peak current limiting functions improve efficiency by eliminating the power dissipation (as well as cost) of external power resistors. Efficiency is further improved because of low bias currents due to standard CMOS processing and the reduced charging current requirements of the internal high voltage MOSFET which has a logic level threshold, low input capacitance, and essentially no Miller capacitance when compared to similar discrete devices.

Design techniques are presented to select the optimum boost inductance and duty cycle precompensation as a function of input voltage, output voltage, and output power.

The *TOPSwitch* Three-Terminal Off-line PWM Switch was originally designed for use in flyback power supplies but is also applicable for boost power factor correction circuits. *TOPSwitch* converts a control current signal to a duty cycle which modulates an integrated high voltage MOSFET switch. For general *TOPSwitch* information, refer to the *TOPSwitch* data sheets and *TOPSwitch* Tips (AN-14).

Figure 1 shows a simplified *TOPSwitch* boost PFC circuit which produces a DC voltage higher than the peak of full wave rectified AC input voltage. Proper control of *TOPSwitch* duty cycle over the line frequency period generates a filtered sinusoidal input current waveform that is in phase with the input voltage waveform.

To illustrate the technique, first consider a boost circuit operating with constant duty cycle over the line frequency period. *TOPSwitch* operates at 100 kHz which is quite high compared to line frequency. On a switching cycle by cycle basis, the input voltage can be considered constant. The control circuit turns on *TOPSwitch* for time Ton which causes *TOPSwitch* current to ramp up linearly as shown in Figure 2. When *TOPSwitch* turns off, the inductor induces a voltage reversal which forward biases the diode. Diode current is shown ramping down to zero. For the simple control scheme where the *TOPSwitch* duty cycle is kept constant over the entire line frequency cycle, the average (filtered value) of *TOPSwitch* current I_T(avg) will be sinusoidal as simulated in Figure 3 and measured in Figure 4. The average value of diode current I_D(avg) is also shown and does not have a sinusoidal waveshape. The inductor current I_L(avg), which is the rectified input current, is the simple sum of the diode and *TOPSwitch* currents and will not have the target sinusoidal average shape if the duty cycle is kept fixed. The measured input current shown in Figure 5 has total harmonic distortion of approximately 18% and a power factor of 0.978.

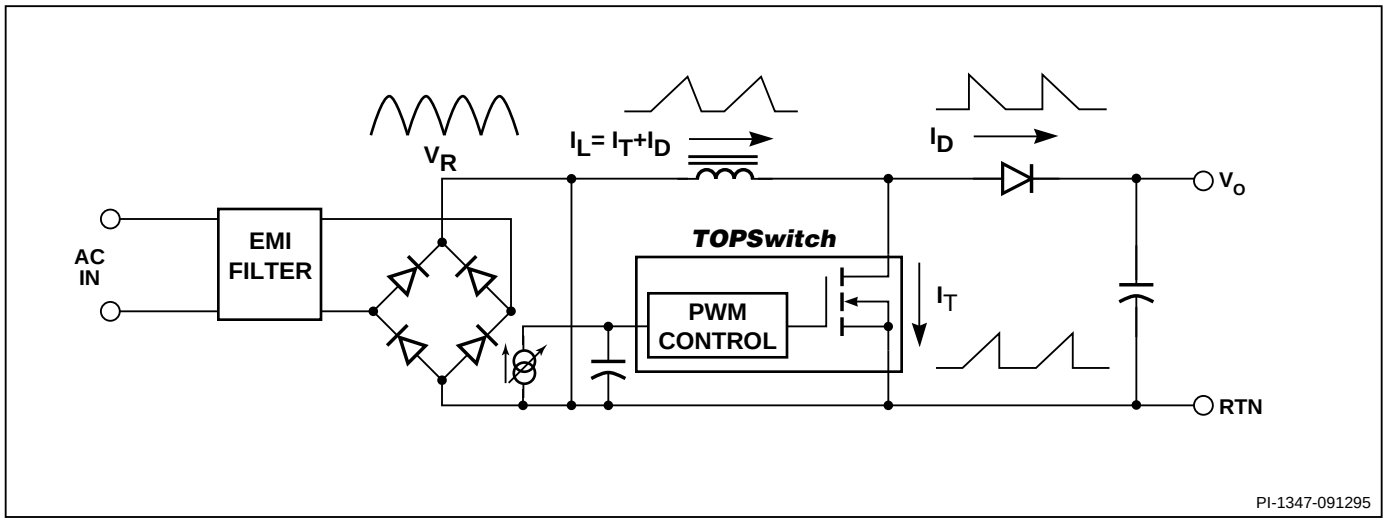

Figure 1. Simplified TOPSwitch Boost PFC Circuit.

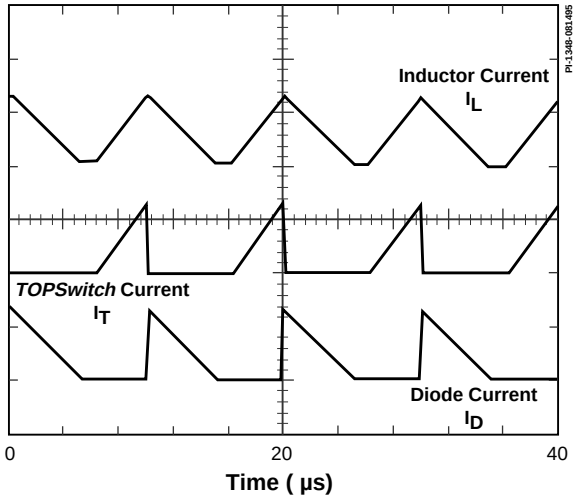

Figure 2. TOPSwitch, Inductor, and Diode Switching Current Waveforms.

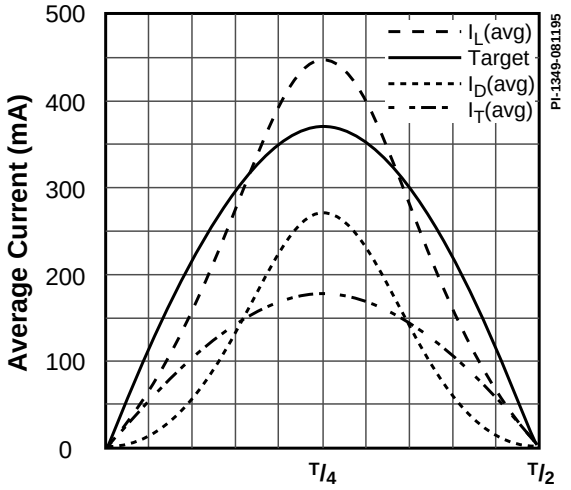

Figure 3. Simulated Average Current Waveforms with Fixed Duty Cycle. (T = Line Frequency Period).

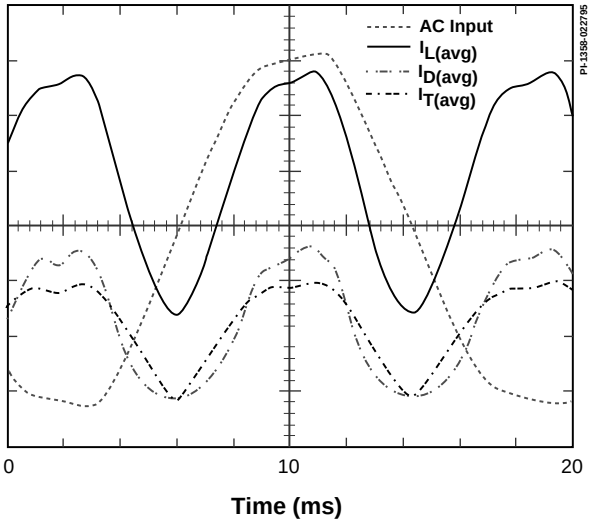

Figure 4. Measured Average Current Waveforms with Fixed Duty Cycle.

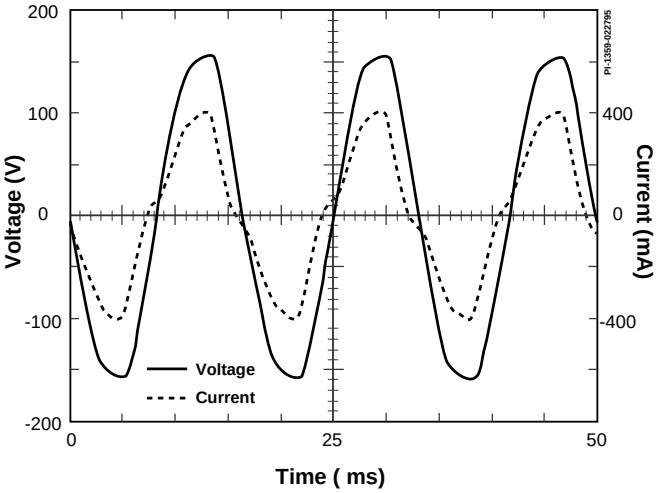

Figure 5. Measured Input Current Average Waveform with Uncorrected Duty Cycle.

To reduce THD and Improve PF, the duty cycle must be properly varied over the line frequency period. The target duty cycle for each high frequency switching cycle as a function of the instantaneous value of the rectified AC input voltage must be determined. The average value of the Nth switching cycle *TOPSwitch* current I_T(avg) can be found from Equations [1] and [2] where D is a the duty cycle, I_{PK} is the peak *TOPSwitch* current, V_{IN} is the instantaneous value of the rectified AC input voltage for the Nth switching cycle, F_S is the switching frequency, and L_p is the inductance.

$$I_{T(avg)} = I_{PK} \times \frac{D}{2} \qquad (1)$$

where peak current I_{PK} can be found from:

$$I_{PK} = \frac{V_{IN} \times D}{f_S \times L_P} \qquad (2)$$

The average value of the Nth switching cycle diode current I_D(avg) can be found from Equation [3] where V_O is the DC output voltage

$$I_{D(avg)} = \frac{I_{PK}^2 \times L_P \times f_S}{2 \times (V_O - V_{IN})} \qquad (3)$$

These two average currents sum in the inductor to become the average inductor current I_L(avg). For a given power level, the

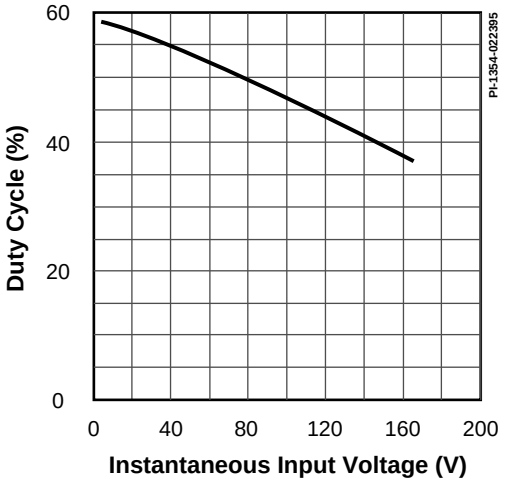

Figure 6. Duty Cycle Correction Curve.

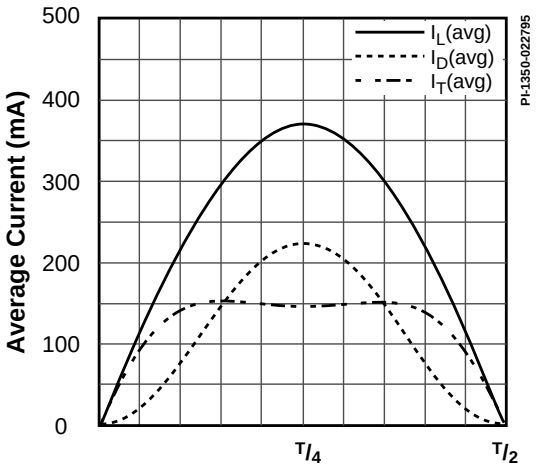

Figure 7. Simulated Average Current Waveforms with Corrected Duty Cycle. (T = Line Frequency Period)

Nth interval instantaneous AC input voltage demands a target average current value (note: average current value is defined here as the average of the 100 kHz switching current waveform which is equal to the Nth interval instantaneous line frequency input current). The equations are rearranged and solved for the duty cycle D as a function of completely independent variables as shown in Equation [5]:

$$I_{L(avg)} = I_{T(avg)} + I_{D(avg)} \qquad (4)$$

$$D = \sqrt{\frac{2 \times f_S \times L_P \times I_{L(avg)} \times (V_O - V_{IN})}{V_O \times V_{IN}}} \qquad (5)$$

This curve is plotted in Figure 6 for 30 Watt input power, 750 µH inductor, 268 volt DC output, 115 VAC input, and 100 kHz switching frequency. Note that the curve is quite linear. Because the target input current is linearly related to the instantaneous input voltage in a fixed frequency, discontinuous boost PFC/THD circuit, the desired duty cycle variation can be easily implemented with an appropriately sized resistor connected from the rectified AC input voltage to the *TOPSwitch* Control pin. The *TOPSwitch* control function is ideal because duty cycle varies inversely with Control pin current.

Figure 7 shows the simulated average waveforms for *TOPSwitch* current, diode current, and inductor current while Figure 8 gives the measured waveforms. Note that neither *TOPSwitch* or diode average currents are sinusoidal but the summation of the two has the desired sinusoidal shape.

Figure 9 is an oscilloscope plot of typical input voltage and corrected current waveforms. The corrected circuit now has THD less than 5% and PF greater than 0.99.

Attached are five example circuits using this technique to improve power factor and reduce total harmonic distortion. In the first three examples, the output voltage is the parameter to be controlled. The last two circuits show other systems where the control parameter is not the DC output voltage. The fourth circuit shows an example of controlling a system voltage while the fifth circuit shows control of a system current. Some circuitry is common to all five circuits as described below:

EMI Line Filter: Consisting in these examples of L2, C1, and C9 as shown in Figure 10. This filter averages the high frequency inductor current waveform to produce the smooth sinusoidal average input current waveform.

Bridge Rectifier: BR1 full wave rectifies the AC input voltage

Boost Power Stage: Consists of inductor L1, rectifier D1, and filter capacitor C4. The boost stage draws energy from the full wave rectified input voltage and stores the energy at high voltage in capacitor C4. Typical DC output voltages are 225 to 275 VDC for 110 VAC input and 400 to 600 VDC for 240 to 277 VAC input.

TOPSwitch Power Supply IC: This device contains an oscillator, pulse width modulator, high voltage power MOSFET switch, and protection circuitry. *TOPSwitch* duty cycle is a function of the current driven into the control pin. Increasing current into the control pin causes the duty cycle to decrease.

Blocking Diode: D2 prevents reverse current through the body diode of the power transistor due to ringing caused by the reverse recovery current spike of boost rectifier D1.

Precompensation Circuit: The key to this PFC/THD technique is to vary the duty cycle inversely with the rectified AC input voltage. Resistor R1 generates a precompensation current proportional to the instantaneous rectified AC input voltage which inversely varies the duty cycle. Capacitor C2 is selected to filter high frequency currents while having insignificant filtering effect on the line frequency precompensation current. Resistor R2 decouples the precompensation current from the auto-restart/compensation capacitor C3 to prevent an averaging effect which would increase total harmonic distortion. Capacitor C1 filters high frequency noise currents which could cause errors in the precompensation current.

Bias Circuit: A second winding on the appropriate system inductor or transformer is used in some circuits for biasing. This winding is rectified and filtered. Rectification can be either dot positive or dot negative depending on the circuit implementation required. This voltage can be used for feedback as well as bias.

Auto-restart/Compensation: *TOPSwitch* is in a quiescent state until C3 charges up to 5.7V. *TOPSwitch* then begins switching and the output voltage begins to rise. C3 holds enough energy to supply *TOPSwitch* bias power until the output becomes regulated. C3 can also be chosen to provide a delay on turn on if necessary. R10 provides a DC path for precompensation current during auto-restart.

Simple Direct Control of Output Voltage

This simple, low cost approach directly senses the output voltage with two series connected Zener diodes as shown in Figure 10. When the output voltage becomes regulated, VR1 and VR2 begin to conduct, drive current into the *TOPSwitch* control pin, and directly control the duty cycle. This 17 component circuit operates from 230 VAC input with typically 0.98 power factor and 7% THD while providing 65 Watts of output power at 420 VDC.

Feedback Winding Control of Output Voltage

This approach, shown in Figure 11, uses a bias winding with two capacitors (C5, C6) and two diodes (D3, D4) on the bias winding (similar to a doubler connection) to produce a bias voltage directly proportional to the output voltage. Small capacitors can be used with the doubler approach because each capacitor must only hold the voltage over a short switching cycle rather than a long line frequency cycle. When the output voltage becomes high enough, Zener diode VR1 begins to conduct current, drives current into the *TOPSwitch* control pin, and reduces the duty cycle. Resistor R3 and capacitor C3 are chosen to filter the line frequency components of the control current as well as compensate the feedback loop.

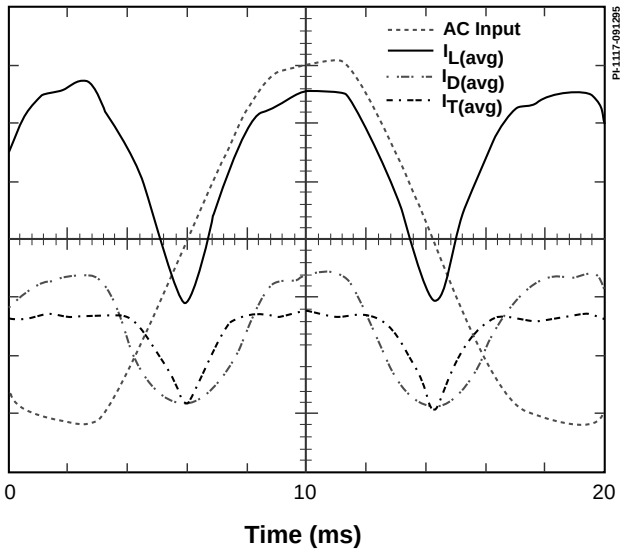

Figure 8. Measured Average Current Waveforms with Corrected Duty Cycle.

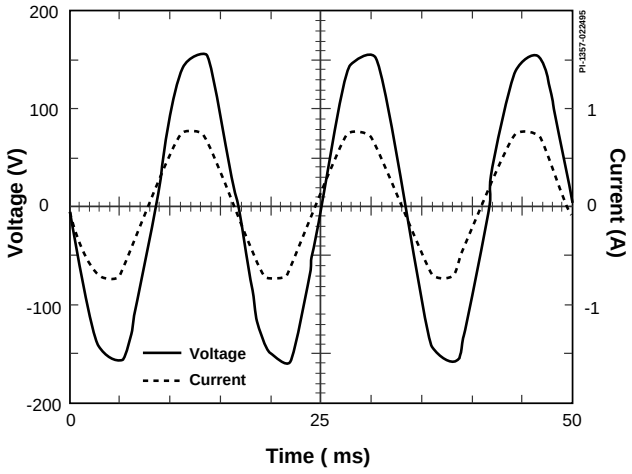

Figure 9. Measured Average Input Current Waveforms with Corrected Duty Cycle.

Direct Sensing with Error Amplifier and Reference

This circuit, shown in Figure 12, uses a TL431 shunt regulator for improved DC accuracy. The TL431 is a 3 terminal device consisting of a temperature compensated 2.5 Volt bandgap reference voltage, op amp, and driver. The TL431 (U2) senses the output voltage directly by divider R3 and R5. The TL431 acts as a current source directly controlling duty cycle. The TL431 holds 2.5 volts across R5 which sets the output voltage through R3. C2 and R5 provide filtering and compensation. R6 limits the current as well as providing additional averaging with C3. Bias power is supplied by D3 and C5.

Sensing and Controlling Load Voltage

Figure 13 shows a circuit using a push pull inverter to generate an isolated output voltage to drive the load. The output voltage is determined by the turns ratio of transformer T1. A winding on transformer T1 returns a voltage proportional to the output voltage. This return voltage is rectified and filtered to be used for closed loop duty cycle control as well as bias.

Sensing and Controlling Load Current

Figure 14 shows a circuit using a half bridge inverter to drive the transformer (T1) primary. Secondary series inductor L2 acts like a current source and is used for loads requiring control of current. A return winding on L2 produces a current proportional to the load current. R4 converts the return current to a voltage which is then rectified and filtered. The filtered voltage, proportional to load current, is used for closed loop duty cycle control as well as bias.

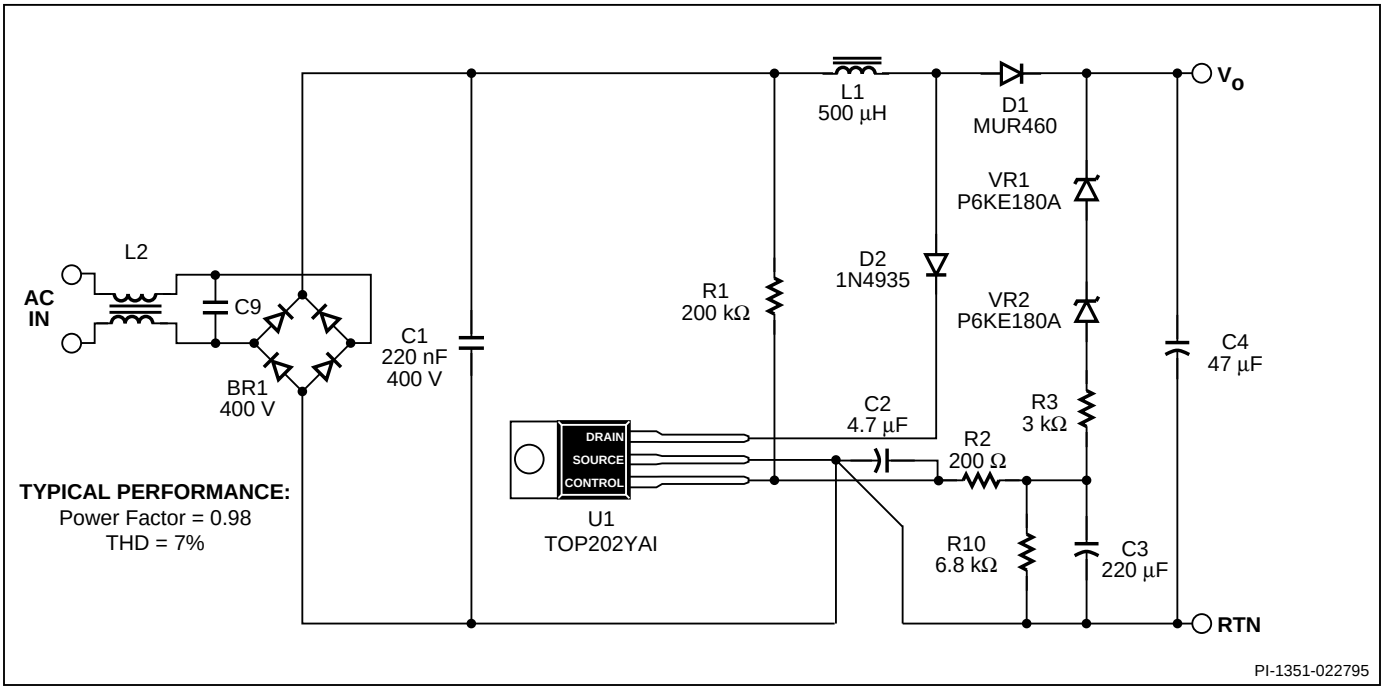

Figure 10. Simple, Direct Sensing of Output Voltage Using only 17 Components.

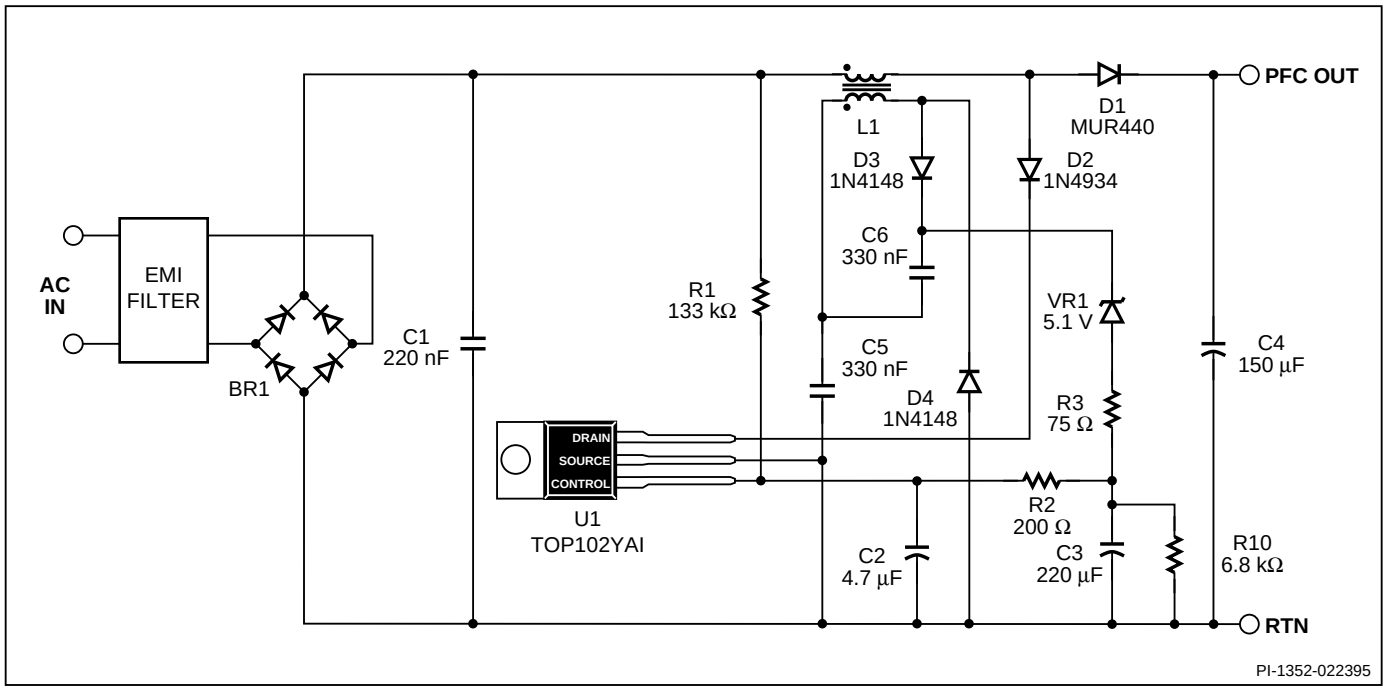

Figure 11. Simple Feedback Winding Control of Output Voltage.

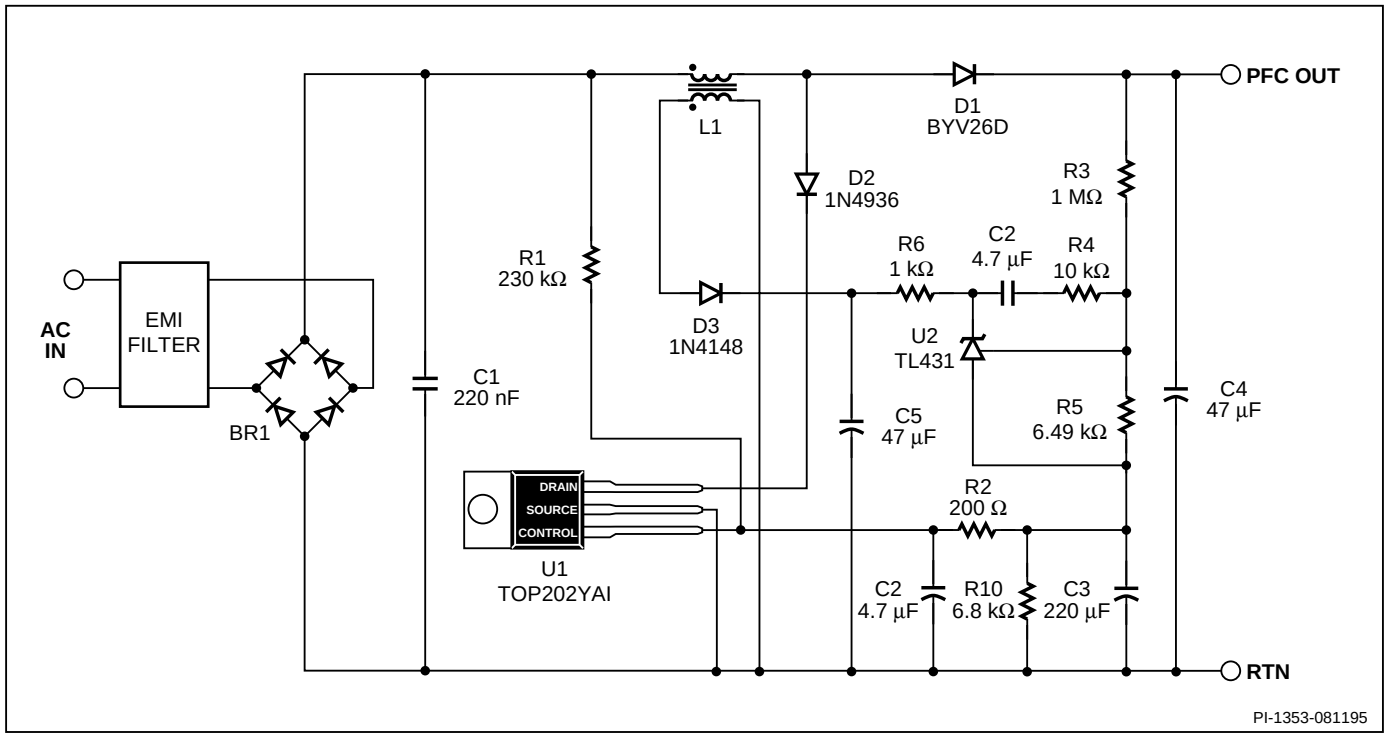

Figure 12. Direct Sensing of Output Voltage with Error Amplifier and Reference.

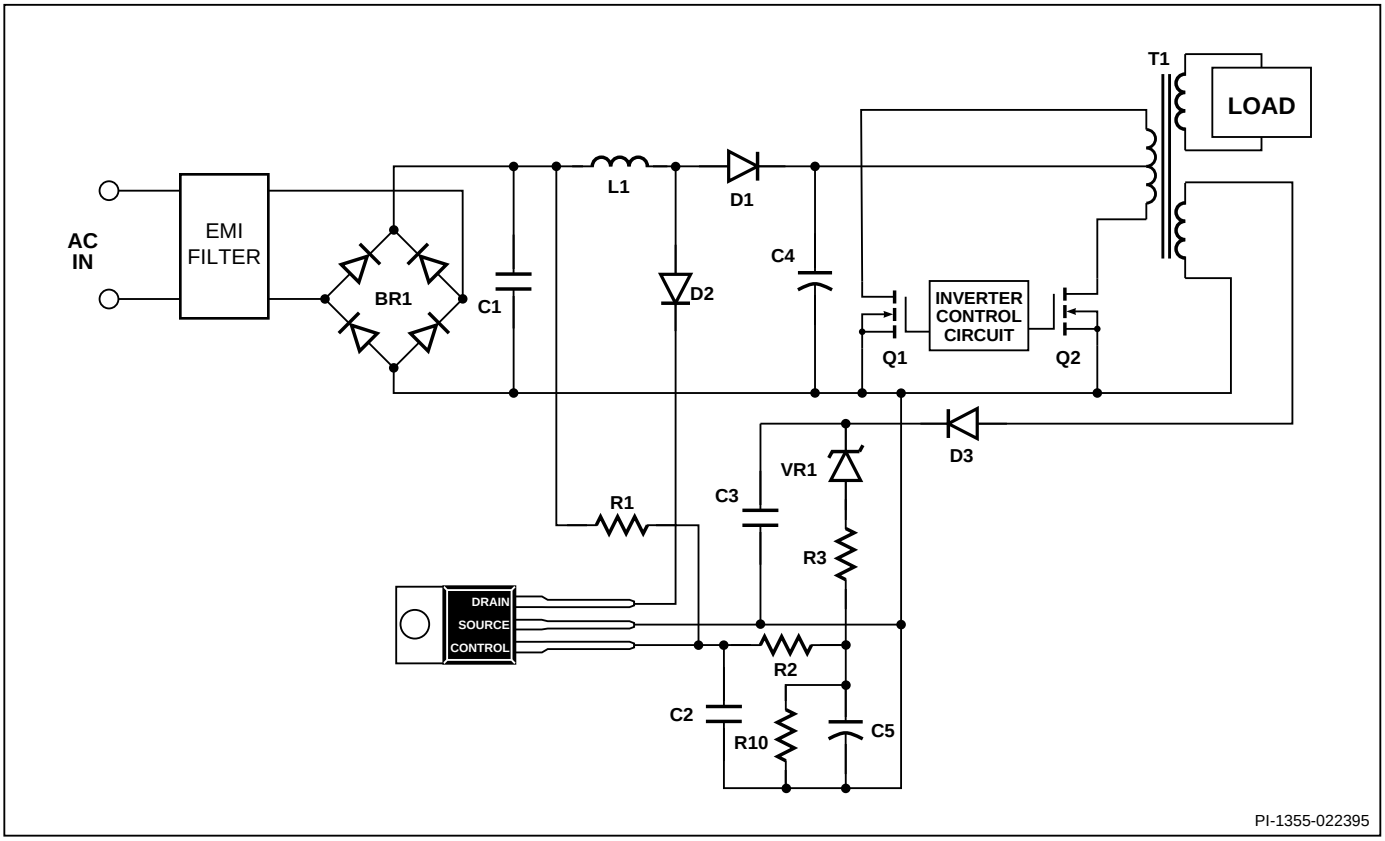

Figure 13. Indirect Sensing and Control of Load Voltage.

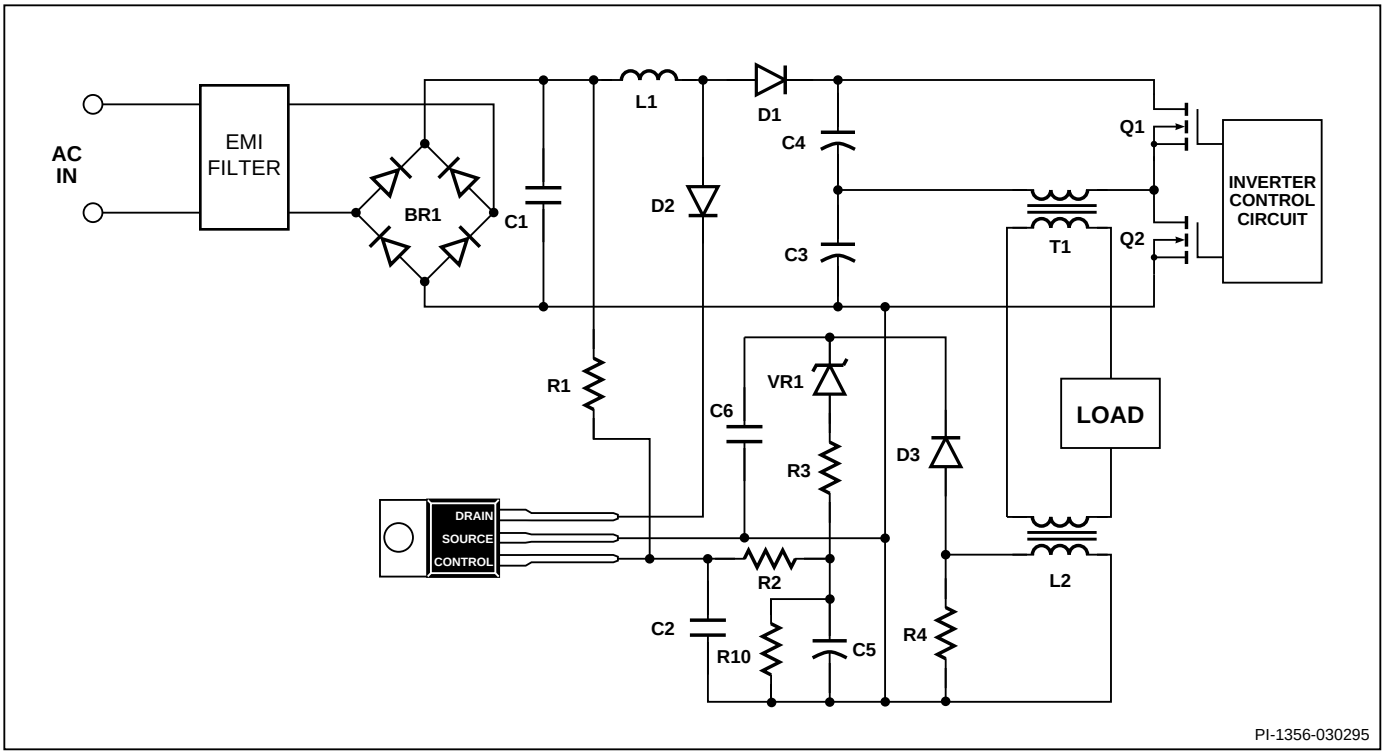

Figure 14. Indirect Sensing and Control of Load Current.

Appendix A: Selecting *TOPSwitch*, Inductor L1, and Precompensation Resistor R1

Table 1 gives the approximate output power range for each *TOPSwitch* when used in PFC circuits. The TOP100 through TOP104 should be used for 110 VAC input while the T0P200 through TOP204 (including the TOP214) should be used for 230 VAC and 277 VAC inputs.

The inductor is selected to operate in the discontinuous mode over the entire line and load range of operation. The optimum inductance value is selected for borderline discontinuous/ continuous operation at the worst case of heavy load and peak of the maximum sinusoidal AC input voltage. This optimum inductance has the lowest peak current, highest efficiency, and lowest EMI. The following iterative approach is used to select the value of the inductor:

Solve for the peak value of the sinusoidal input current with maximum AC input voltage.

Select an initial value for inductance L and solve for the target duty cycle.

Solve for *TOPSwitch* peak drain current.

Test for borderline discontinuous/continuous operation.

Iterate with new inductance value if necessary to maintain borderline discontinuous/continuous operation.

The peak value ($I_{IN(pk)}$) of the sinusoidal input current is found from an estimate of boost preregulator efficiency maximum output power P_O, and maximum RMS AC input voltage V_{MAX}:

$$I_{IN(pk)} = \frac{P_O \times \sqrt{2}}{V_{MAX} \times \eta}$$

The peak value ($V_{in(pk)}$) of the sinusoidal input voltage is found from:

$$V_{IN(pk)} = V_{MAX} \times \sqrt{2}$$

Given switching frequency F_S, DC output voltage V_O, and an initial value for inductance L_P, the target duty cycle can be found:

$$D = \sqrt{\frac{2 \times f_S \times L_P \times I_{IN(pk)} \times \left(V_O - V_{IN(pk)}\right)}{V_O \times V_{IN(pk)}}}$$

PART #	PFC OUTPUT POWER 230/277 VAC INPUT
TOP200	0 - 25 W
TOP201	20 - 50 W
TOP202	30 - 75 W
TOP203	45 - 100 W
TOP214	60 - 125 W
TOP204	75 - 150 W
PART #	**PFC OUTPUT POWER 110 VAC INPUT**
TOP100	0 - 30 W
TOP101	25 - 50 W
TOP102	35 - 70 W
TOP103	45 - 90 W
TOP104	55 - 110 W

Table 1. Recommended PFC Output Power Ranges.

Peak *TOPSwitch* current $I_{T(pk)}$ can now be found from:

$$I_{T(pk)} = \frac{V_{IN(pk)} \times D}{L_P \times f_S}$$

The inductance can now be tested for discontinuity. Results less than 1 are discontinuous while results greater than 1 are continuous:

$$\left(\frac{f_S \times L_P}{V_O - V_{IN(pk)}} \times I_{T(pk)}\right) + D \le 1$$

For a continuous result greater than 1, a smaller inductance must be selected and the calculations repeated. For a discontinuous result significantly less than 1, a larger value of inductance can be used to operate closer to the discontinuous/ continuous border for improved efficiency and EMI performance.

The final inductance value should be reduced by typically 10% for manufacturing tolerances. Measurements taken in the actual circuit should be used to calculate the effective inductance for verification and correlation with measurements taken from RLC bridges, impedance analyzers, or other bench test equipment.

Example: for the following requirements:

65 Watts output power

420 Volts DC Volts output voltage

265 Vrms maximum AC input voltage

100 kHz Frequency

0.93 Efficiency

Iteration proceeds as follows:

Iteration#	0	1	2
L(uH)	350	650	541
D	0.087	0.118	0.108
$I_{T(pk)}$ (mA)	928	681	746
DC/C Inequality (<=1)	0.80	1.10	1.00

The 550 µH value selected for inductor Lp provides borderline discontinuous/continuous operation. For an assumed manufacturing tolerance TOL of 10%, the nominal value L_{NOM} must be reduced as follows:

$$L_{NOM} = \frac{L_P}{1+\frac{TOL}{100}} = \frac{541\mu H}{1+\frac{10}{100}} = 492\mu H$$

Curves for inductance as a function of output power for various output voltages are shown in Figures 15, 16, and 17 for 277 VAC, 230 VAC, and 110 VAC respectively. These curves are based on the assumption of 93% efficiency and a high line voltage 15% over the nominal value (for example, 265 VAC is approximately 15% over the nominal 230 VAC mains voltage).

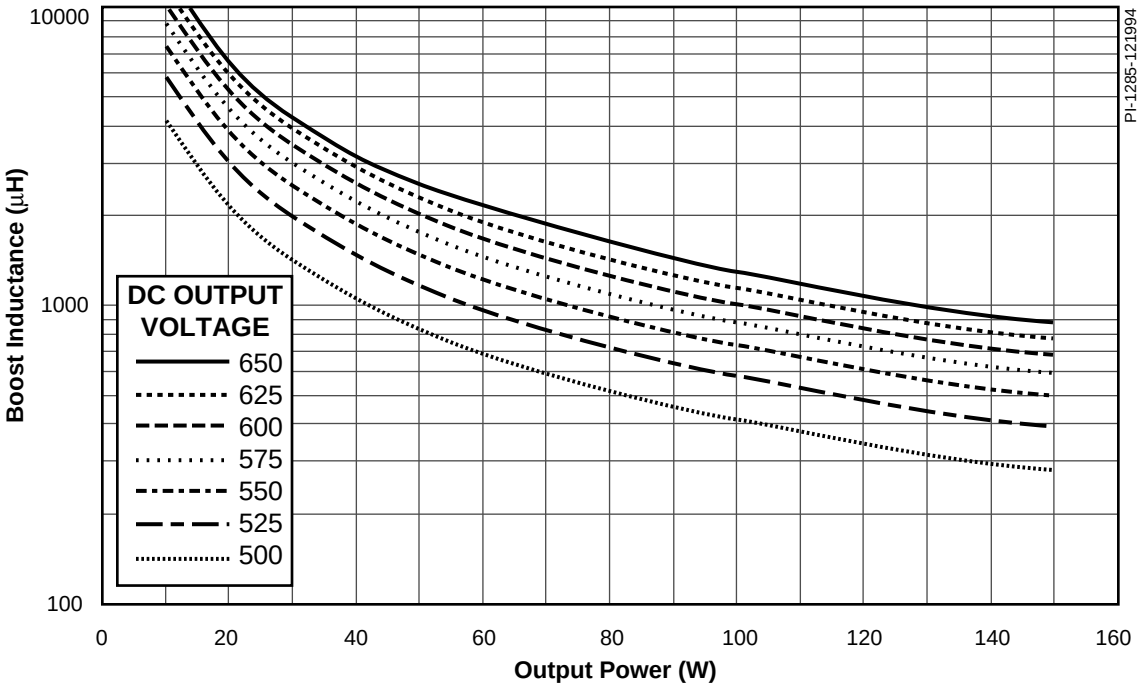

Figure 15. Boost Inductance L1 vs. Output Power (277 VAC Input).

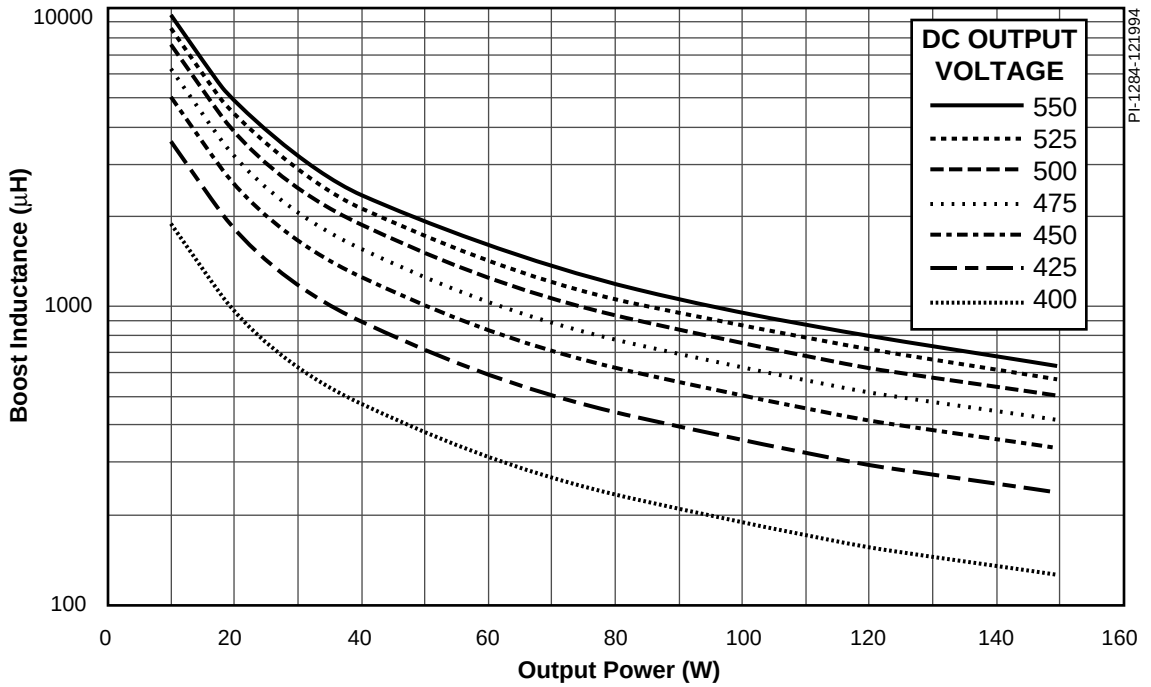

Figure 16. Boost Inductance L1 vs. Output Power (230 VAC Input).

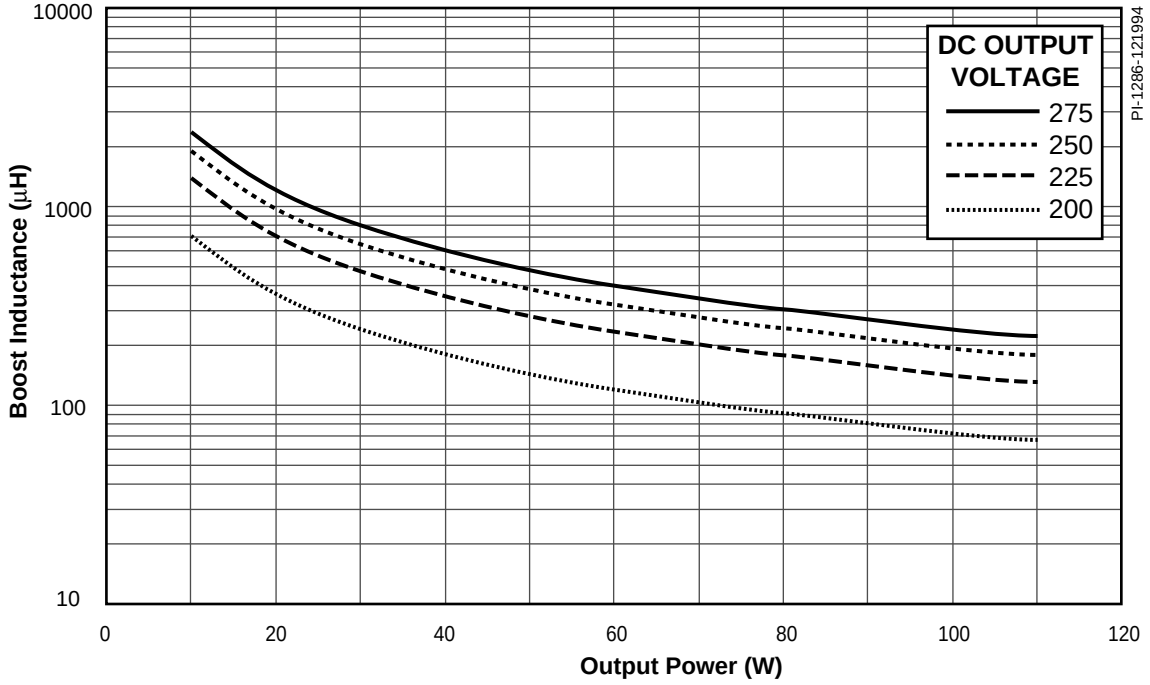

Figure 17. Boost Inductance L1 vs. Output Power (110 VAC Input).

The precompensation resistor is best selected by graphing the target duty cycle and curve fitting with a straight line as shown in Figure 18. Note that the "best fit" line should match the curve more closely at the highest voltage where most of the power is delivered. The slope S_{DV} of the best fit straight line is used to calculate precompensation resistor R1 in KΩ as follows where A_{PWM} is the *TOPSwitch* duty cycle to control current gain in %/mA (typically 16 %/mA):

$$R1 = -\frac{A_{PWM}}{S_{DV}} = \frac{16}{0.067} = 239k\Omega$$

Curves for precompensation resistor R1 as a function of output voltages for 110, 230, and 277 VAC input voltages are shown in Figure 19.

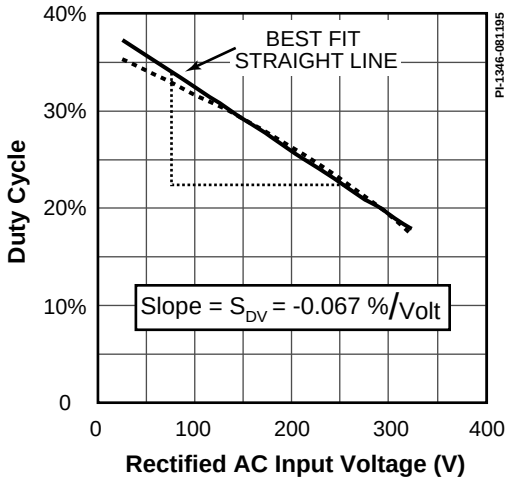

Figure 18. Curve Fitting Duty Cycle With Straight Line Approximation.

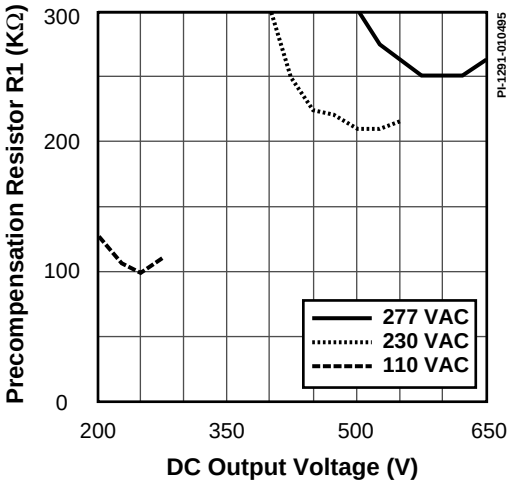

Figure 19. Precompensation Resistor R1 vs. DC Output Voltage.

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