AN1699
APPLICATION NOTE

Efficient driving network for ESBT to reduce the dynamic V_{CESAT} and enhance the switching performances

Introduction

This document deals with the ESBT driving requirements (emitter switched bipolar transistor).

First of all the classic driving network proposed in the literature has been analyzed to highlight its characteristics, its field of application and its limits as well. Among them, the dynamic V_{CESAT} is the most important. This problem becomes more evident if the conduction time is relatively low and/or not a ZCS topology. In these cases, if the base current is not well shaped, power dissipation rises, eliminating the benefits of using ESBT.

To solve this problem, a new driving network is proposed. Despite of its simplicity and cost effectiveness, it allows to drastically reduce the dynamic V_{CESAT} and to optimize the losses during both conduction and switching phases.

The benefits of the proposed solution, against the existing one, are underlined by using a forward converter with a working frequency of 110 kHz and a duty cycle of about 20 %.

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1 THE CLASSICAL DRIVING CIRCUIT

The ESBT (Emitter Switching Bipolar Transistor) configuration consists of a High Voltage Bipolar Transistor and a Low Voltage Power Mosfet in Cascode topology, as shown in *Figure 1.*

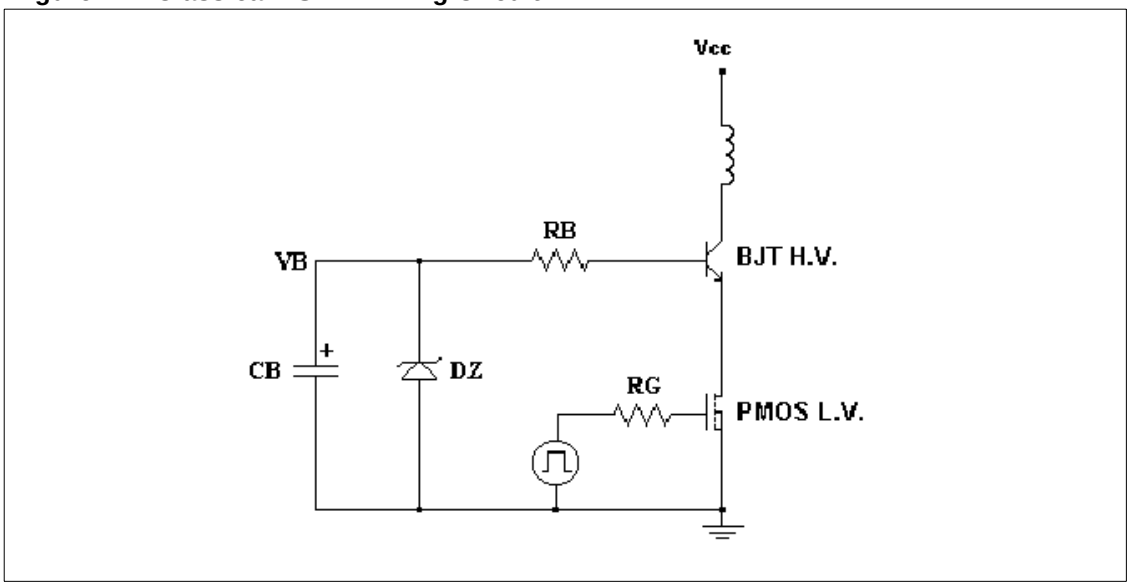
This configuration has been well known since the 80's, but what makes it very interesting nowadays, is the possibility of finding in the market better Bipolar Transistors able to reach (In Cascode Topology) squared RBSOA performance and Low voltage Power Mosfets with very low Rdson, almost similar to ideal switch in ON stage.

The main advantages of the technology are the very low ON voltage drop, typical of a Bipolar transistor and the very fast switching speed. During turn OFF the Ib, pulled from the base pin is equal to the Ic (double than the usual Iboff in any bipolar-based topology). It leads to a huge reduction of the OFF Time

(Ts+Tf), allowing working frequencies as high as 150kHz.

Usually, the driving circuit for the Bipolar Part of the ESBT devices needs just a constant voltage, an electrolytic capacitor, a zener diode and a resistor, as shown in *Figure 1.* The capacitor is needed to store energy during the Turn Off, so that it can be re-used during the next turn ON, while the zener will avoid the base voltage to overcome a fixed value.

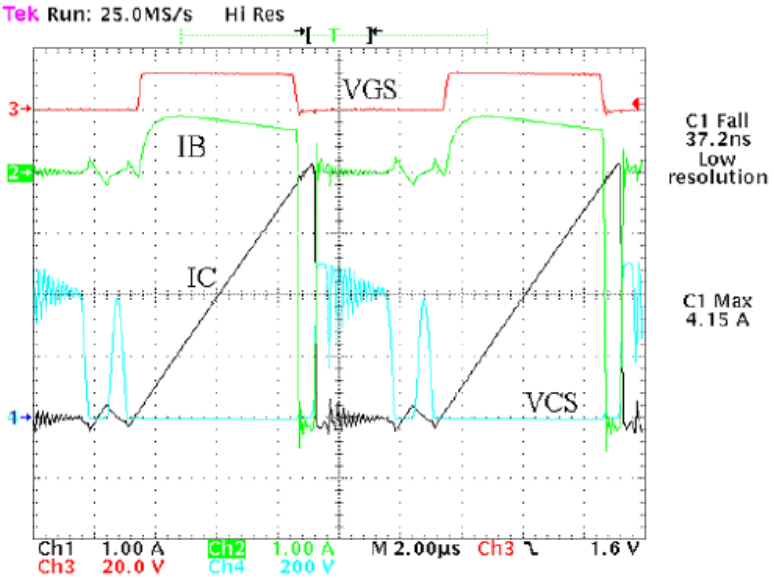
Figure 1. Classical ESBT Driving Circuit



The driving circuit shown above is very useful and efficient whenever the current on the device is almost zero or at least very small if referred to the nominal one during the turn ON. Moreover, in order to get an efficient system it is necessary to get $I_{BOFF}*t_{storage} \approx I_{BON}*t_{ON}$

In this case, the needed driving energy for the conduction is slightly higher than the one recovered during the turn OFF. It is then enough to provide to the base a very small power to recover the unavoidable losses. *Figure 2.* shows the waveforms of a discontinuous flyback converter working at 100kHz .

Figure 2. Discontinuous Flyback Converter Waveforms



2 NEED FOR OPTIMIZATION IN MORE DIFFICULT TOPOLOGIES

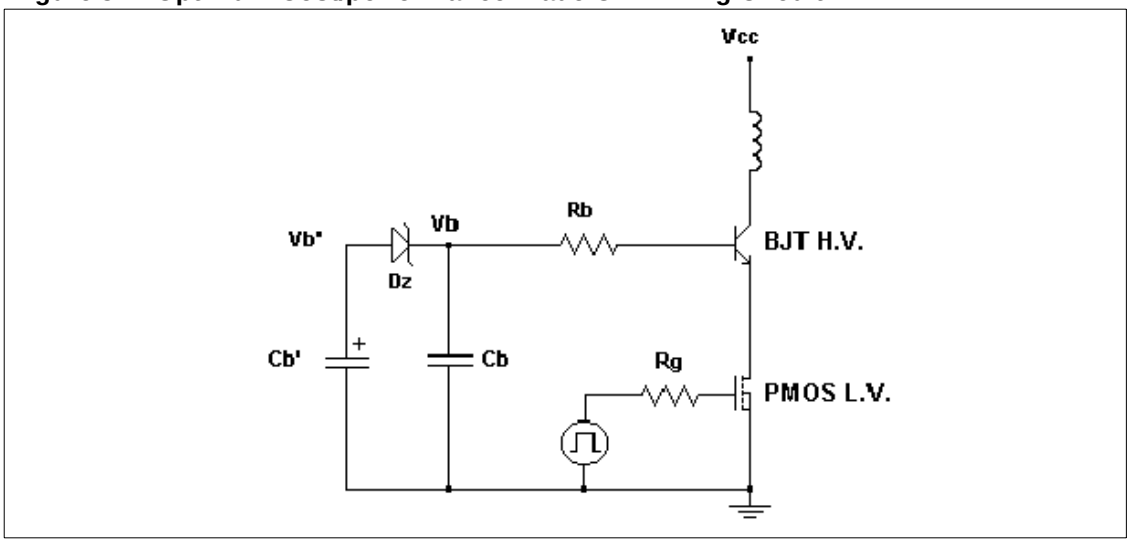
Once the Turn ON current is not equal to zero and the working frequency becomes higher than 100kHz, the dynamic V_{CEsat} problem starts to appear. This phenomenon is related with the delay of the voltage drop between Collector and Emitter to reach the static value (V_{CEsat} in any bipolar datasheet). For this reason it is needed to fill the base of minority carriers in the fastest possible way.

It is evident that the higher is the working frequency, the worse this effect will be. Moreover, the need to have a high I_{Bon} at the beginning is in contrast with the low one needed right before the turn OFF. In fact the benefits got at the turn ON could become weakness for the turn OFF performances.

For this reason a particular modulation of the base current, which allows the optimization of both switching phases, is needed.

3 MODIFIED DRIVING CIRCUIT

Figure 3. Optimum Cost/performance Trade Off Driving Circuit



In figure *Figure 3.* the optimum cost/performance trade off driving circuit is shown. Simplicity and efficacy are the points of strength of this solution. The following paragraph explains how and when to make the best of the circuit itself:

- Frequency Higher than 60kHz

- Relatively low Duty Cycle (< 30%)

- Not ZCS topologies

In all the mentioned cases the dynamic V_{CEsat} becomes a major problem. In fact, when high frequency and low duty cycle cases occurs, the total conduction time is very short and by adding a starting Ic not equal to zero, it is easily understandable why the V_{CE} is not quickly going to the saturation value.

All this can be avoided if a high base current could be got at the starting, as it happens in the proposed circuit, which allows to get a high current spike, still keeping the already shown benefits of the Emitter Switching fast turn Off.

Vb' is kept constant thanks to the electrolytic capacitor $C_{b'}$, while Vb can be chosen upon the different topology need. By using a relatively low (non electrolytic) C_b value, Vb will be higher than $V_{b'}$ during the first part of the turn ON, accomplishing to the current spike need. From this value, both the maximum current value and time of the initial spike can be adjusted: the lower is the capacitor value, the shorter will be the spike duration.

A small R_b (0.33Ω) is enough to control the base current both at the Turn ON and Conduction.

The biggest advantages of the proposed driving circuit are summarized below:

- Base current modulation

- Total energy recovery (during turn OFF)

- Simplicity

The zener diode allows a tight base current control, by setting the exact difference between V_b and $V_{b'}$, finally linked with the base current spike.

A further advantage of the proposed circuit is the possibility to set $V_{b'}$ (affecting the all ON stage) independently from the voltage needed (V_b) to get the desired current spike.

Thanks to the combination of the non-electrolytic capacitor and zener diode properly chosen, the maximum (V_b) value is set.

In the following figure an ESBT based Forward Converter is shown. The converter working parameters are here listed:

- 110kHz

- 20% duty cycle

- $I_{Cturn\text{-}ON} > I_{COFF}$

4 PERFORMANCE COMPARISON BETWEEN THE TWO NETWORKS

For a better understanding of the proposed circuit, the waveforms comparison is shown below:

Figure 4. Waveforms Related To The Proposed Driving Circuit

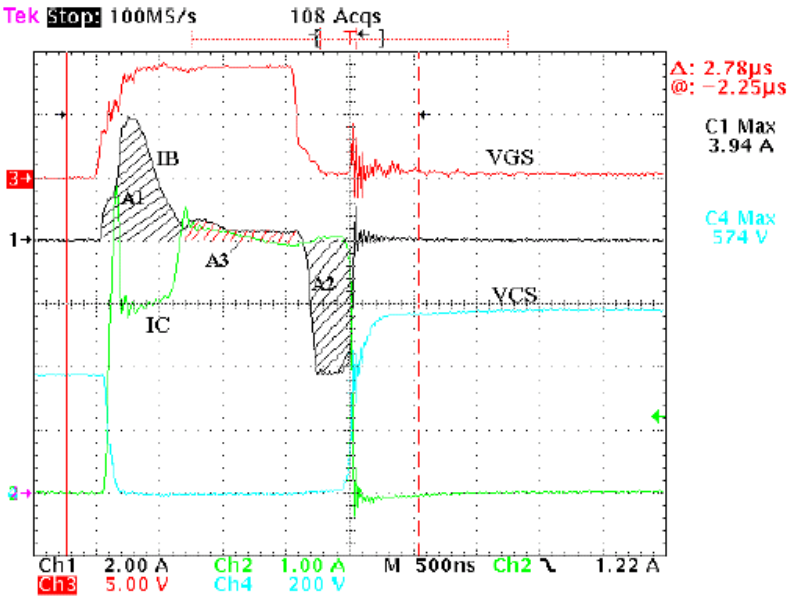
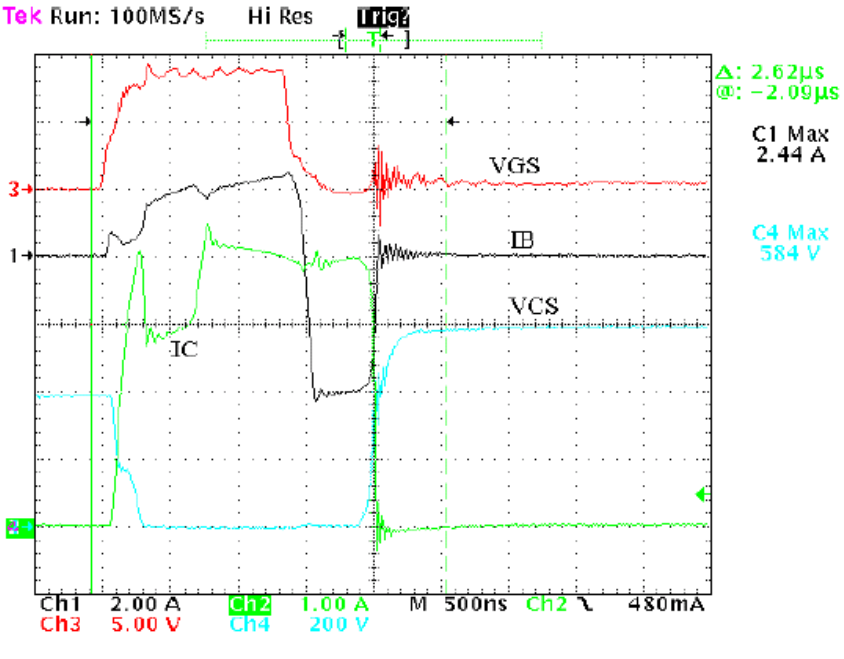


Figure 5. Waveforms Related To The Classic Driving Circuit



Due to the higher VB in the original driving circuit as compared with the proposed one, it happens to have a longer storage time, involving worse Turn Off performance both power and frequency wise. On the other hand, if this problem would be solved by reducing the voltage level, the bad performance would just shift from the Turn Off to the Turn ON& Conduction, causing a worse I_C/V_{CE} cross plus a slower dynamic

V_{CEsat}

It is important to notice that the overall power dissipated for the Base Bias network is very small, as well as in the case of the classical one, as it is evident from the almost full energy recovery from the turn OFF to the turn ON. In fact, the amount of charge needed at the turn ON, which is not recovered at the turn OFF can be easily seen in figure 4 where A1 ≈ A2, and the only one needed from the DC is A3 (Red striped zone).

In those topologies where a initial current spike is present at the collector of the device it is clear that the proposed network is giving the biggest benefit. In *Figure 6.* e *Figure 7.* is shown the turn ON condition for both the proposed circuit, where it is finally evident that by using the patented network the turn ON power consumption can be reduced to almost 1/3 of the original one.

Thanks to the proposed network, at switch ON the high V_b voltage (see *Figure 3.*) gives a base current spike which goes, after the capacitance (C_b) discharge, to the stable lower value referred to $V_{b'}$. At the same time the current value changes accordingly, keeping the ESBT in fully saturated zone (see *Figure 4.*).

Figure 6. Turn-ON With The Proposed Base Bias Network

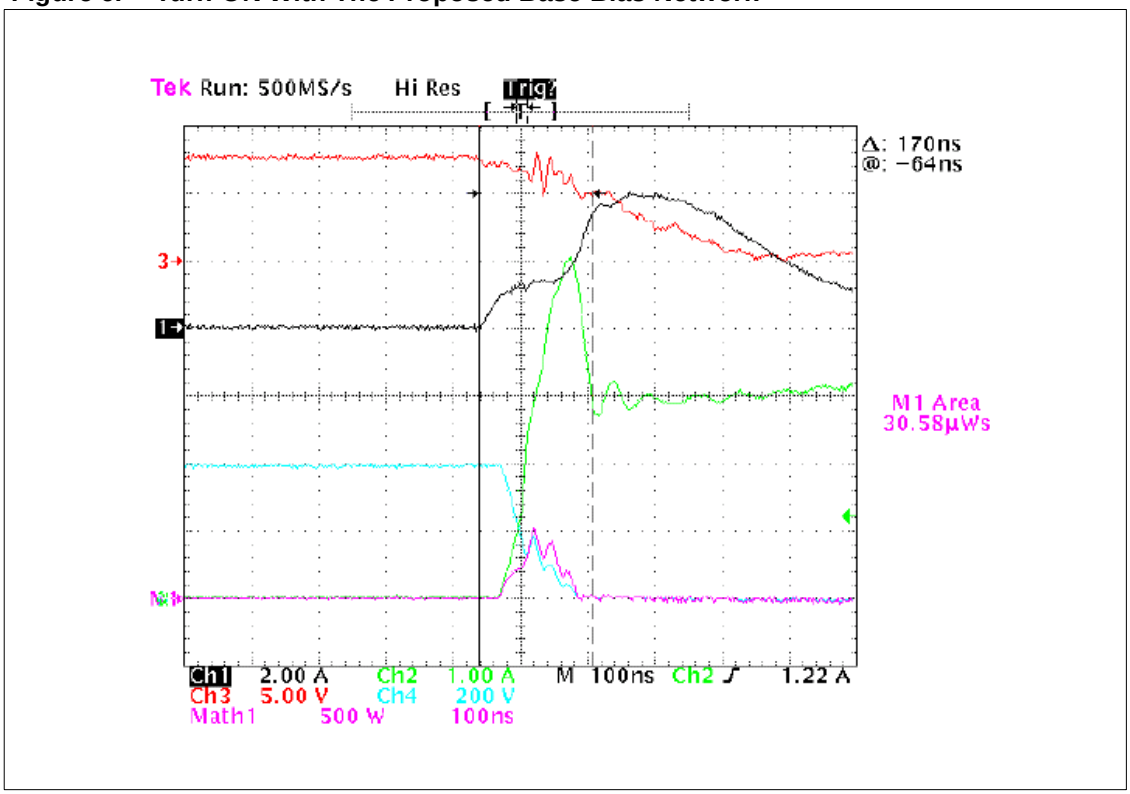
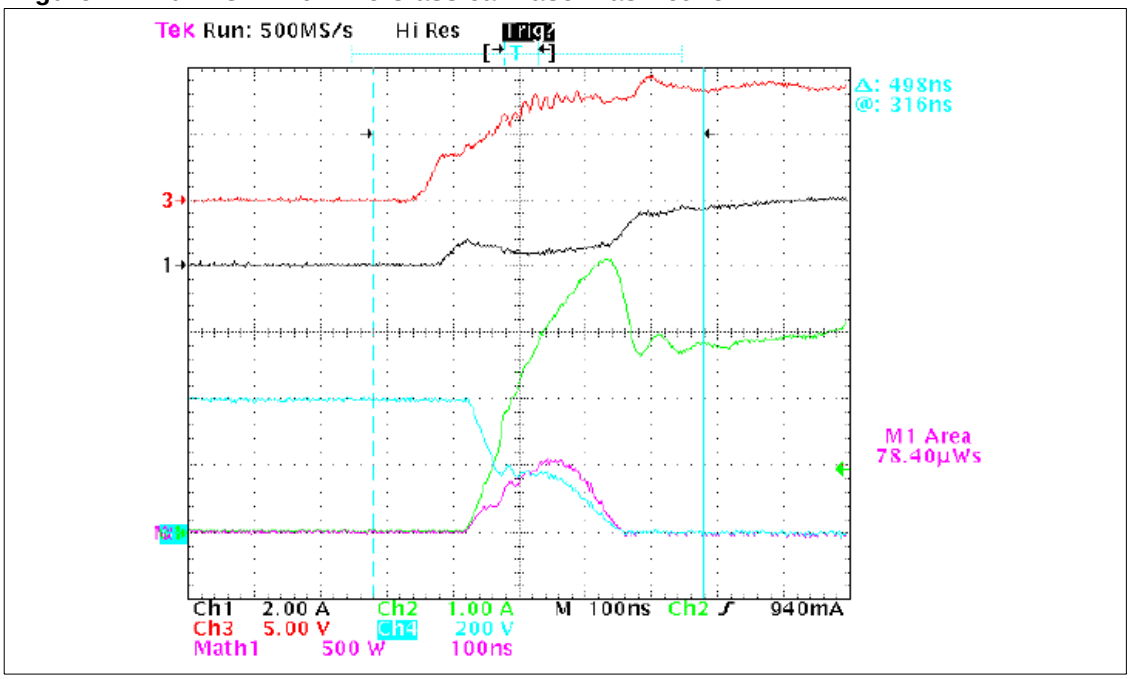


Figure 7. Turn-ON With The Classical Base Bias Network



Besides the effect of the dynamic V_{CEsat} on the turn ON performance, it has to be underlined that also the conduction losses could be badly affected by the mentioned parameter. In fact, without the initial current spike, the V_{CE} cannot get to the static low value in less than 2 ÷ 3 µs. *Figure 8.* and *Figure 9.* show a clear example of the mentioned problem. While with the proposed network the static V_{CS} value can be reached in around 200ns, by using the classical network the static value will not be reached at all. It is clear that since $V_{CS} = V_{CE} + V_{DSON}$, the overall problem is related to the V_{CE} of the bipolar core of the ESBT, being the V_{DSON} as fast as a standard low voltage Mosfet.

Figure 8. V_{CS} With The Proposed Base Bias Network

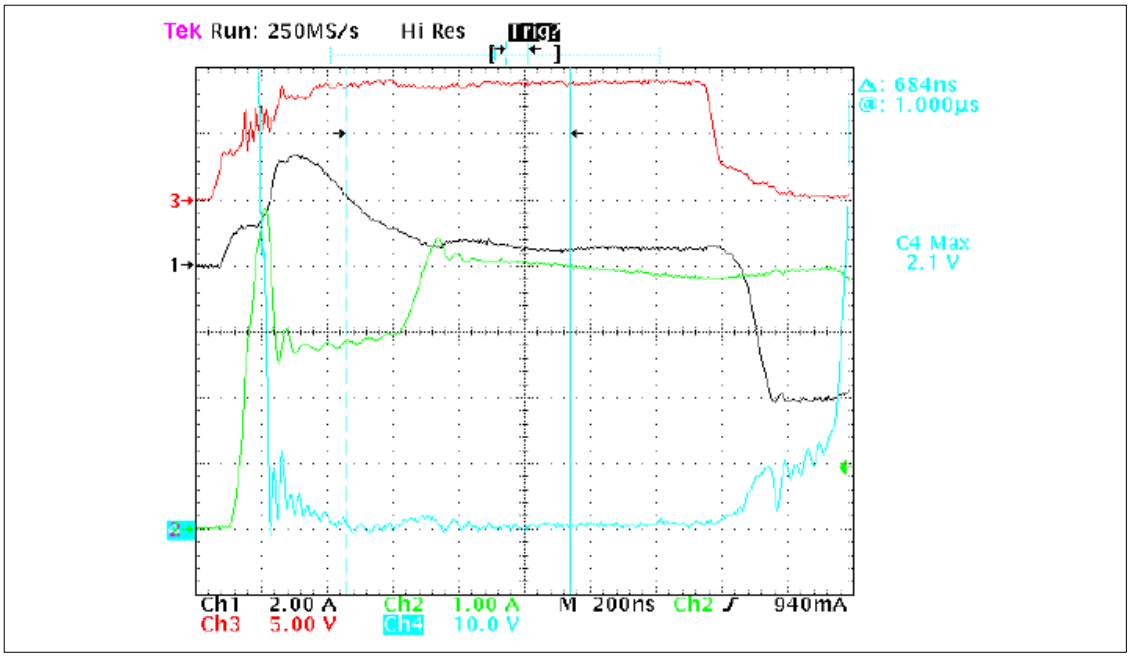
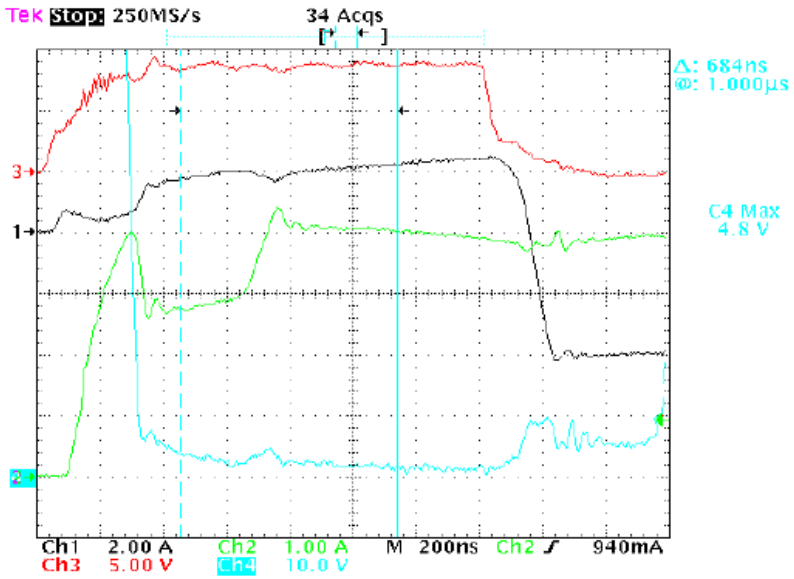


Figure 9. V_{CS} With The Classical Base Bias Network



As a further example of what explained above about the OFF performance, *Figure 10.* and *Figure 11.* show that, also in this case, the proposed network gives benefits in both power consumption and storage time as compared with the classical circuit.

Figure 10. Turn OFF With The Proposed Base Bias Network

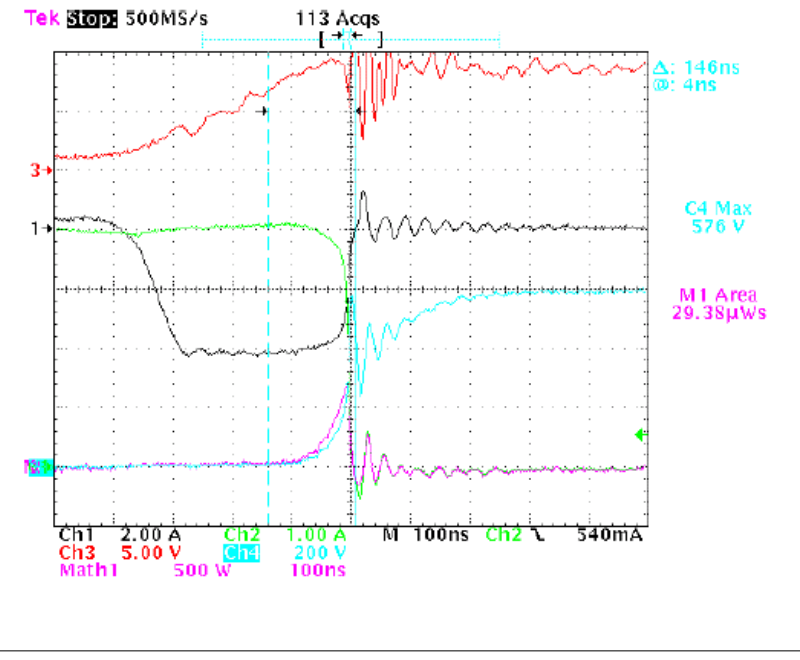
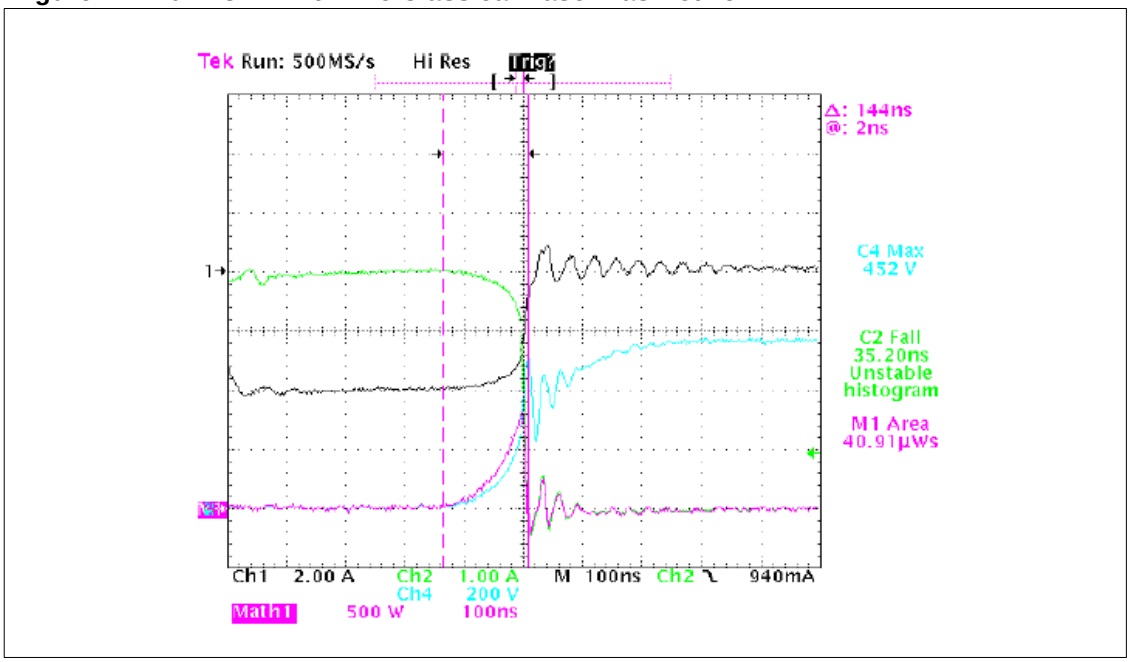


Figure 11. Turn OFF With The Classical Base Bias Network



5 PRACTICAL EXAMPLE

For a deeper and clearer understanding of the above mentioned principles, a practical example is given below, where the design equation applied to the system confirms the theory needs:

- Application: Desktop SMPS (350W)
- Configuration: Forward Single Switch
- Application Key Parameters:
  - Switching frequency = 130kHz
  - Working Drain(collector) current = 5A
- ESBT Device (STL12IE90) Key Parameters:
  - BVCSS=900V
  - h_{FE}(@5A)=10
  - V_{BSON}=1.4V

- Design Equations: (*Figure 3.*)

$$I_{BON} = \frac{V_{Cb} - 1.4 - V_{BSON}}{R_1}$$

$$V_{Cb}(t_0) = V_0 \cdot e^{\frac{-t_0}{\tau}}$$

$$V_{Cb}(t_0) = 0 \Rightarrow (R_1 + R_b) \cdot C_{Cb} = \frac{t_0}{3}$$

where R_b is the equivalent resistance of the base emitter junction.

$$V_{Cb\,TON} = \frac{1}{C_{Cb}} \int_0^{T_s} I_{BOFF}\, dt$$

$$I_C = I_B \bullet h_{FE}$$

- Example Matching:

$$I_{BON} = 5/10 = 0.5A$$

$$V_{Cb`} = 3V$$

$$V_{BSON} = 1.3$$

$$t_0 = 500n\,\mathrm{sec}$$

$$T_S = 300n\,\mathrm{sec}$$

$$R_1 = \frac{3 - 1.4 - 1.3}{0.5} \cong 0.6\Omega \Rightarrow 0.5\Omega$$

$$C_{Cb} = \frac{500 \cdot 10^{-9}}{3 \cdot 0.8} = 208nF \Rightarrow 220nF$$

$$V_{Cb\,TON} = \frac{300 \cdot 10^{-9} \cdot 5}{220 \cdot 10^{-9}} = 6.81V \Rightarrow 7V$$

6 CONCLUSIONS

In this paper a new dedicated Base Bias Network has been presented and explained in all its benefits.

The basic design equations presented in this paper have to be considered as general guidelines for a rough choice of the components values, which still need a fine tuning based on the practical PCB layout.

This "complex" network is needed only when such critical conditions occur (Ic spike and high frequency/ low duty).It is mandatory to underline that the proposed circuit is not the only solution for the topology itself. Besides the presented cases, the simple classical network is already able to provide all the benefits related to the ESBT technology, which once again, becomes a huge performance/flexibility gain whenever High Voltage "&" High Frequency are needed.

7 REVISION HISTORY

Date	Revision	Changes
May-2003	1.0	First edition
06-Sept-2005	2.0	- New template - Title of AN changed - Part 5. changed