**FAIRCHILD**

SEMICONDUCTOR®

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# FD2004 — Adaptive Digital DC-DC Controller with Current Sharing

## 1. Overview

### 1.1. Features

**Power Conversion**

- Efficient Synchronous Buck Controller

- Adaptive Performance Optimization Algorithms

- 4.5V to 14V Input Range

- 0.54V to 4V Output Range (with Margin)

- ± 1% $V_{OUT}$ Setpoint Accuracy

- Fast Load Transient Response

- Current Sharing and Phase Interleaving

- Digitally Adjustable Current Sense Range

- *Snapshot™* Parametric Capture Mechanism

- RoHS-Compliant (5 x 5mm) QFN Package

**Power Management**

- Digital Soft-Start/Stop

- Precision Delay and Ramp-up

- Power Good / Enable

- Voltage Tracking, Sequencing, and Margining

- Voltage / Current / Temperature Monitoring

- SMBus Communication (PMBus™ Compliant)

- Output Voltage and Current Protection

- Internal Non-volatile Memory (NVM)

### 1.2. Applications

- Servers / Storage Equipment

- Telecom / Datacom Equipment

- Power Supplies (Memory, DSP, ASIC, FPGA)

### 1.3. Description

The FD2004 is a digital DC-DC controller designed to work with the FD1505 MOSFET driver IC. Current sharing allows multiple devices to be connected in parallel to source loads with very high current demands. Adaptive performance optimization algorithms improve power conversion efficiency across the load range. The Digital-DC™ technology enables a blend of power conversion performance and power management features.

The FD2004 is designed to be a flexible building block for DC power and can be easily adapted to designs ranging from a single-phase power supply operating from a 4.5V input to a multi-phase supply operating from a 12V input. The FD2004 eliminates the need for complicated power supply managers as well as numerous external discrete components.

Operating features can be configured by pin-strap / resistor selection or through the SMBus serial interface. FD2004 uses the PMBus™ protocol for communication with a host controller and the inter-device DDC bus for communication with other Digital-DC devices.
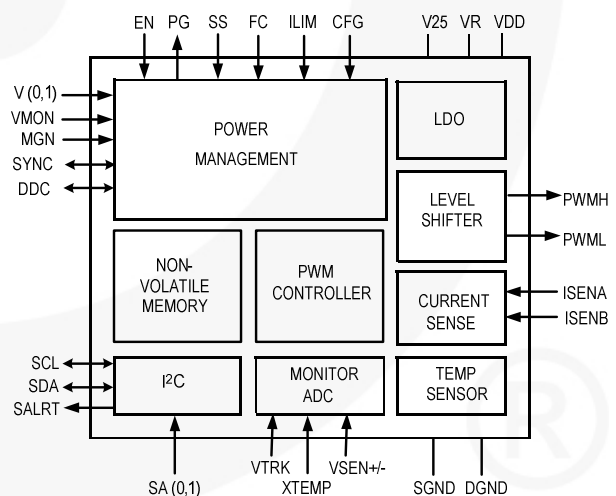


**Figure 1. Block Diagram**

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