

# **N-Channel MOSFET**

**Rev. 2.01 – April 2007**  
**SAMWIN SOUTH Semiconductors**

## 1. Content

<b>1. Content</b> .....	1
<b>2. General Information</b> .....	2
<b>3. Technology Information</b> .....	3
<b>3.1 Wafer Process Technology</b> .....	3
<b>3.2 Package Technology</b> .....	4
<b>3.2.1 Package Information</b> .....	4
<b>3.2.2 Other available packages</b> .....	5
<b>3.3 Test</b> .....	5
<b>3.4 Wafer Process Control</b> .....	6
<b>3.5 Assembly Process Control</b> .....	8
<b>3.6 OQC(Out-going Quality Control)</b> .....	11
<b>4. Qualification</b> .....	13
<b>4.1 Change Procedure</b> .....	13
<b>4.2 Qualification Flow</b> .....	14
<b>5. Package Dimensions</b> .....	15
<b>6. User Information</b> .....	18
<b>7. Environmental Information</b> .....	18
<b>8. Other Data</b> .....	19
<b>8.1 Approval Certificate</b> .....	19
<b>8.2 Datasheet Reference</b> .....	21
<b>8.3 Address Reference</b> .....	21
<b>Remarks:</b> .....	22

## 2. General Information

**Product Name:** For All Products  
**Function:** N-Channel MOSFET  
**Wafer process:** 0.8um VDMOS  
**Available plastic package types:** TO-92 TO-251(252) TO-220(F)

**Locations:**

<b>Product development</b>	Samwin South Semiconductors, ShenZhen, China	Samwin
<b>Wafer plant</b>	Silan Semiconductor, Hangzhou, China	F1
	CSMC	F2
<b>QC responsibility</b>	Samwin	
<b>Assembly</b>	Huanshan Electronics, ShanTou, China (TO-220/F, TO-92)	A1
	Mingxing Electronics, Wuxi, China (TO-251, TO-252)	A3
	Changjiang Electronics, Jiangying, China (TO-92)	A2
<b>Probe test</b>	F1,F2	
<b>Final test</b>	Huanshan Electronics, ShanTou, China (TO-220/F, TO-92)	
	Mingxing Electronics, Wuxi, China (TO-251, TO-252)	
	Changjiang Electronics, Jiangying, China (TO-92)	
<b>Quality Assurance</b>	Samwin	
<b>Reliability testing</b>	Samwin, F1	
<b>Failure analysis</b>	Samwin, F1,F2,A1,A2,A3	

Quality Assurance Management

Signed.....

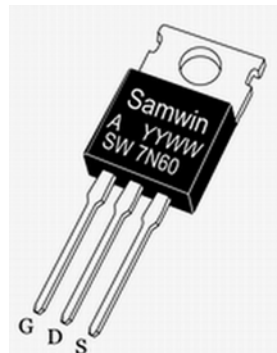
## 3.1 Wafer Process Technology

<b>Process type (Name):</b>	<b>0.8um VDMOS</b>
<b>Base material:</b>	<b>Silicon</b>
<b>Wafer Thickness (final)</b>	<b>XXXµm</b>
<b>Wafer diameter</b>	<b>XXXmm</b>
<b>Number of masks</b>	<b>XXX</b>
<b>Gate oxide</b>	
<b>Material</b>	<b>Silicon oxide</b>
<b>Thickness</b>	<b>XXXXA</b>
<b>Polysilicon</b>	
<b>Number of layers</b>	<b>1</b>
<b>Thickness</b>	<b>XXXXA</b>
<b>Metal</b>	
<b>Number of layers</b>	<b>1</b>
<b>Layer 1 material</b>	<b>AL</b>
<b>Passivation</b>	<b>NONE</b>

## 3.2 Package Technology

### 3.2.1 Package Information

	TO-92	TO-251(252)	TO-220(F)
Package weight	0.2 g		2.05g (2.2g)
Chip separation method		<b>Sawing</b>	
Lead frame			
Material		<b>Bar Cu</b>	
Type	TO-92DT(H)	KFC-30	SANSUNG TSP
Lead plating		<b>Electroplated Sn/100</b>	
Die attach	Silver paste	Soft Solder	Soft Solder
Material		<b>Pb/Sn/Ag 93.5/5/1.5</b>	
Type	DAD-87		
Wire bonding			
Material	AU wire	AL wire	AL wire
Diameter	0.8mil(G) 0.8×2mil(s)	6mil (G) 10mil(s)	6mil(G) 10mil (S)
Method		<b>Ultrasonic</b>	
Molding			
Material		<b>EPOXY</b>	
Type	SI-7200DX2 (HF) KL-G200	EK5600H (HF) EK5600G	SI-7200DX2 (HF)SG8200DS/8300DS
Flammability rating		<b>UL94 V-0</b>	
Marking			
Method		<b>Laser Print</b>	
Coding (Example: SW 7N60)			



YYWW (process code include date info.)

Dry packing		None	
Tape packed	TO-92	TO-251(252)	TO-220(F)
Primary	Box	Tube (Tape)	Tube
Material	Tape paper	Antistatic PVC	Antistatic PVC
Number per unit	2000	80 (2500)	50
Secondary	Box	---	---
Material	Cardboard	---	---
Number per unit	30000	32000 (20000)	8000

Labeling (minimum)  
Bar coding

Device type, Quantity, Date Code, Prod. code  
Code 39 to EIA-556-A

### 3.2.2 Other available packages

Other package available: TO-126, TO-263

### 3.3 Test

Probe equipment  
Probe temperature

VR/30A KE  
25±2°C

Final Test equipment

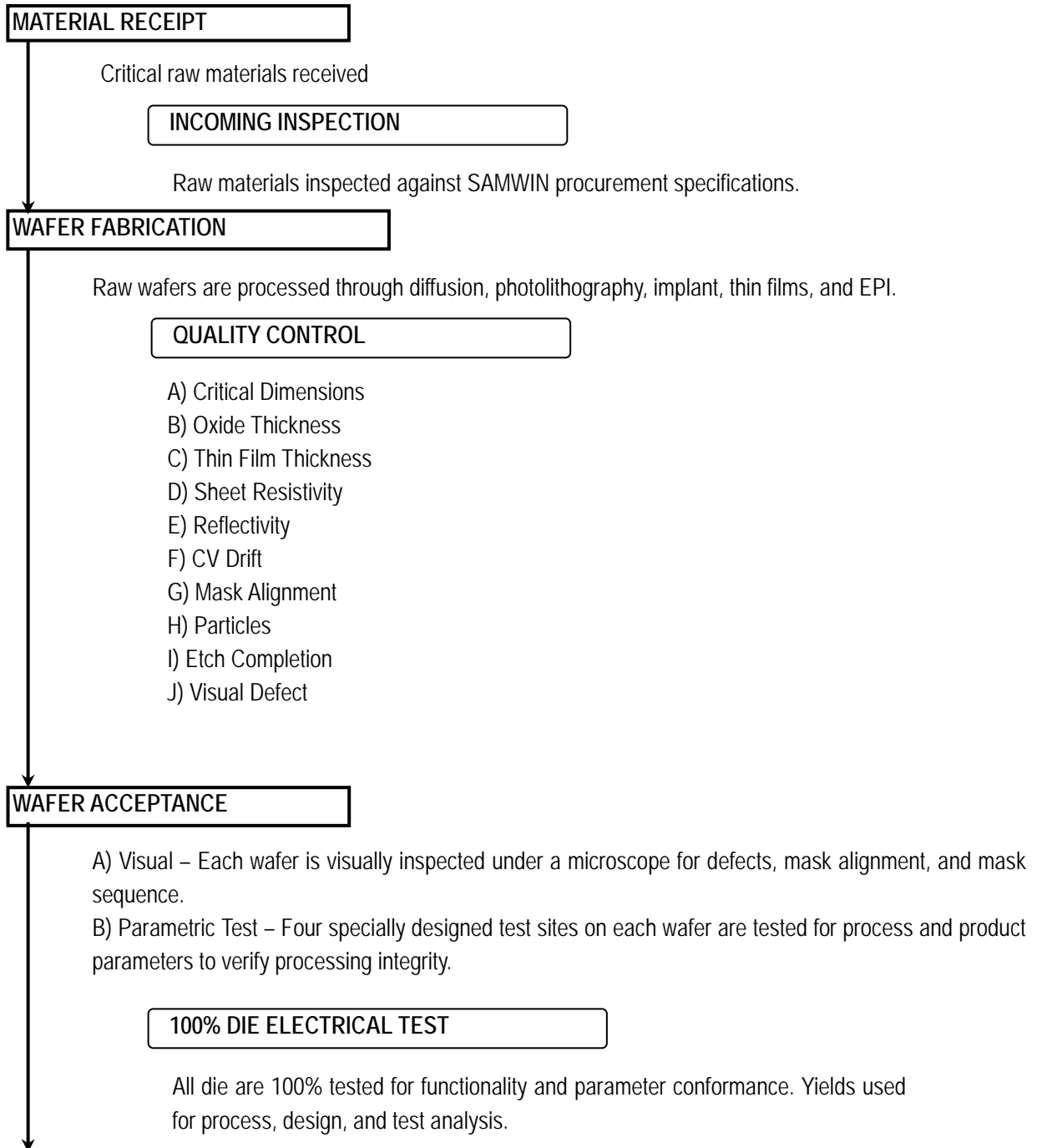
881-TT TESEC  
DTS-1000 JUNO

Final Test temperature

25±2°C

## 3.4 Wafer Process Control

All the inspections and controls are defined as a process step in the production management control system. PC system could be summarized as follows:



DIE ELECTRICAL TEST

Visual Inspection for:

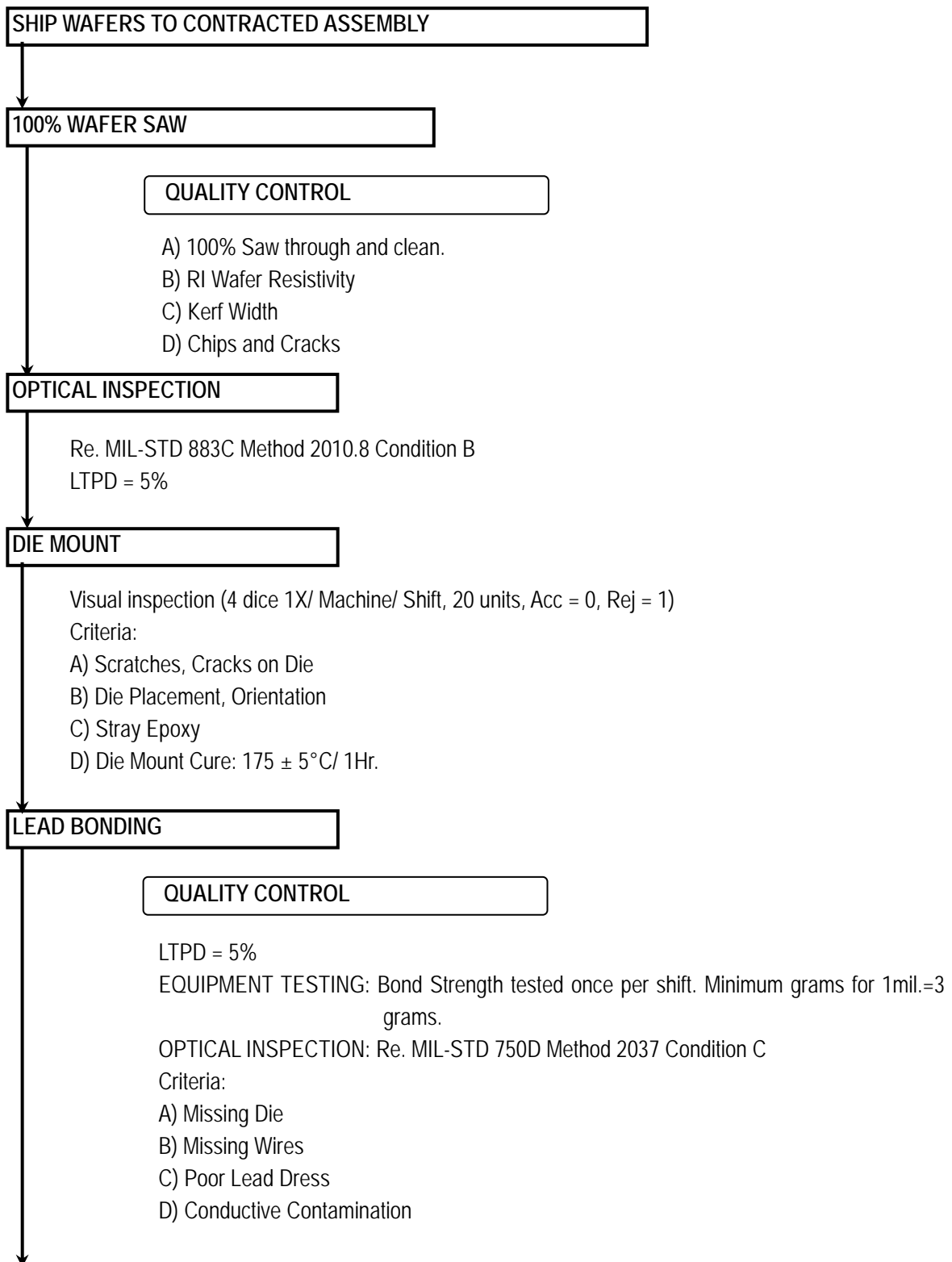
- A) Process Defects
- B) Probe Scratches or Other Damage
- C) Electrical Test Anomalies
- D) Correct Probe Marks

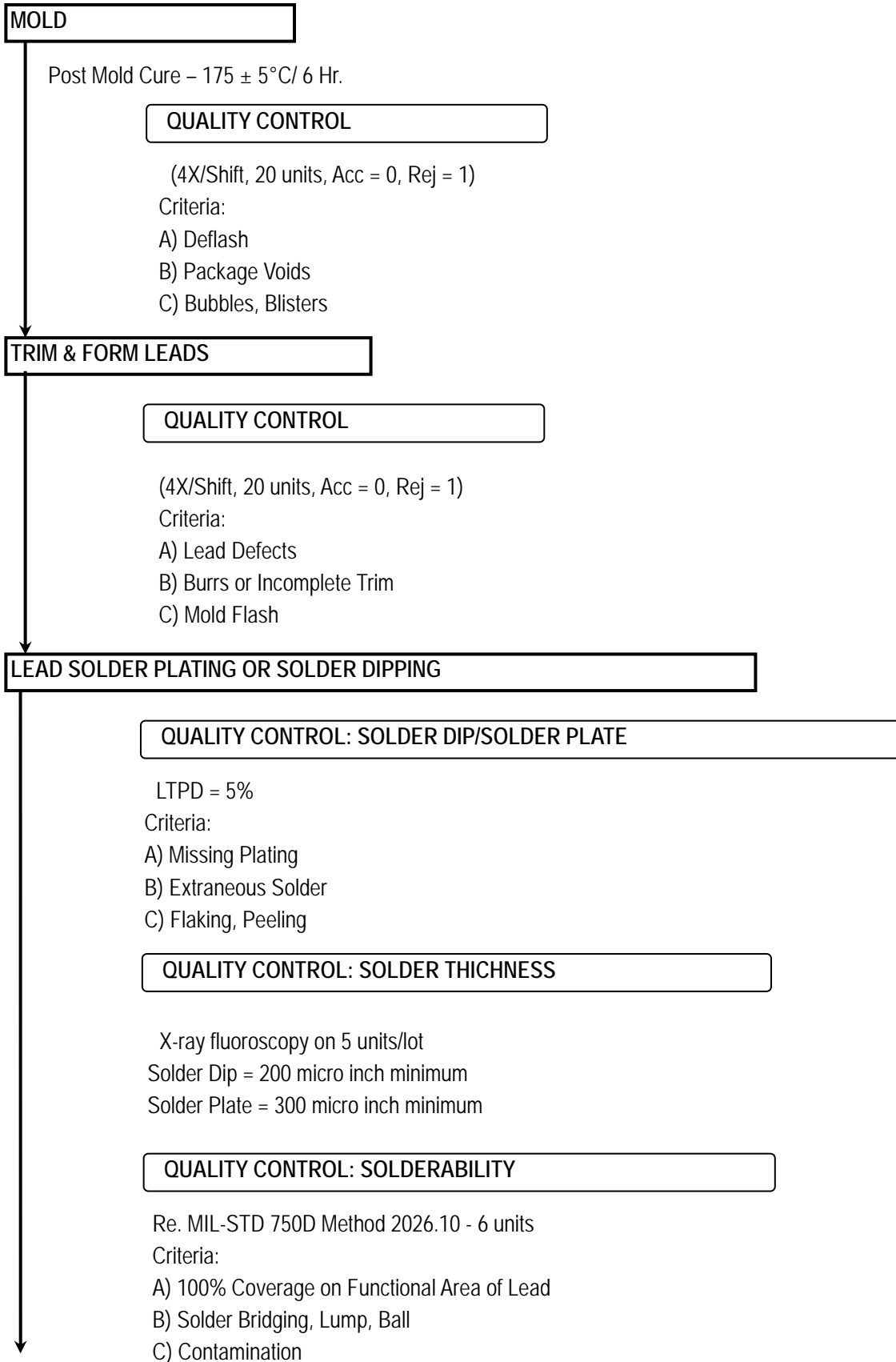
SHIP WAFERS TO CONTRACTED ASSEMBLY

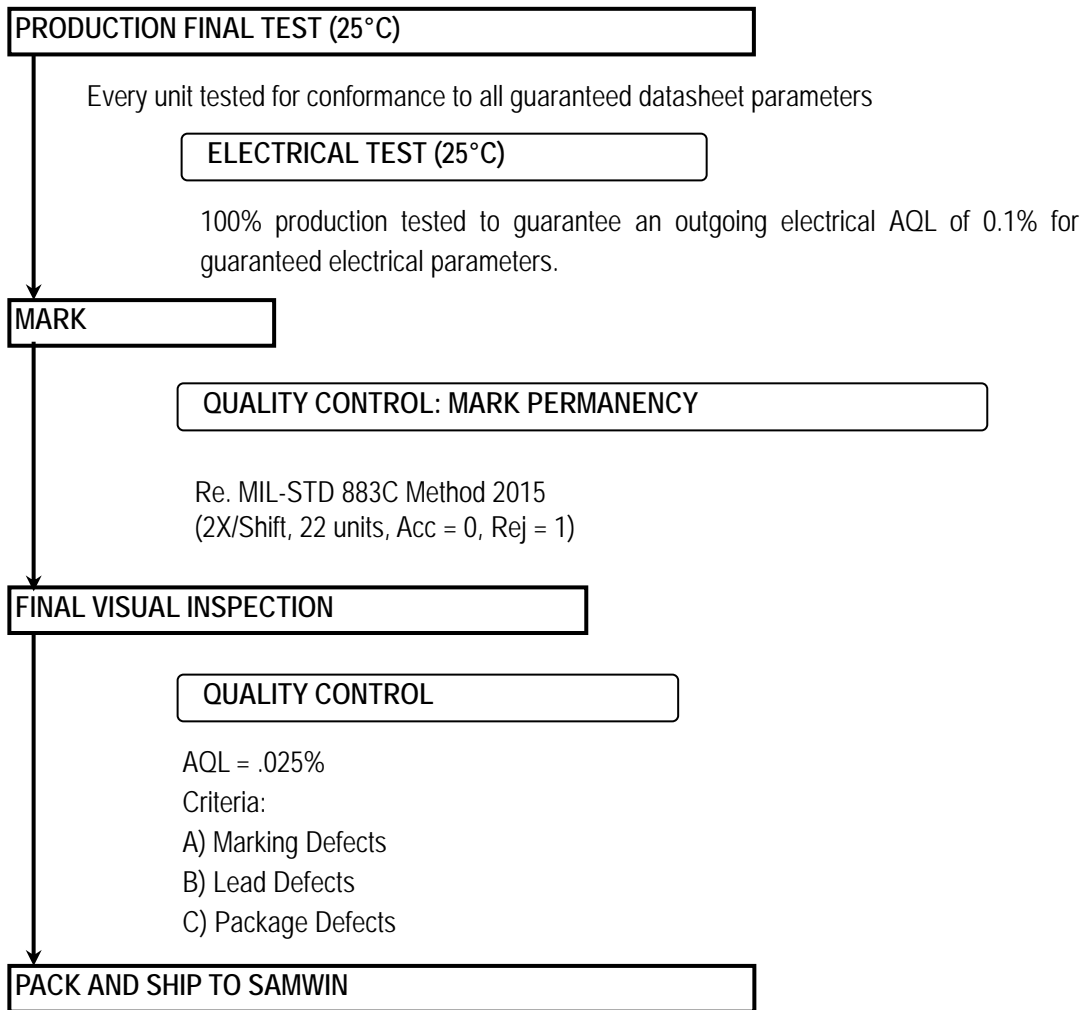
**Critical process parameters are identified by using F.M.E.A. and other advanced tools. Specific steps of wafer process quality control are defined as hereafter:**



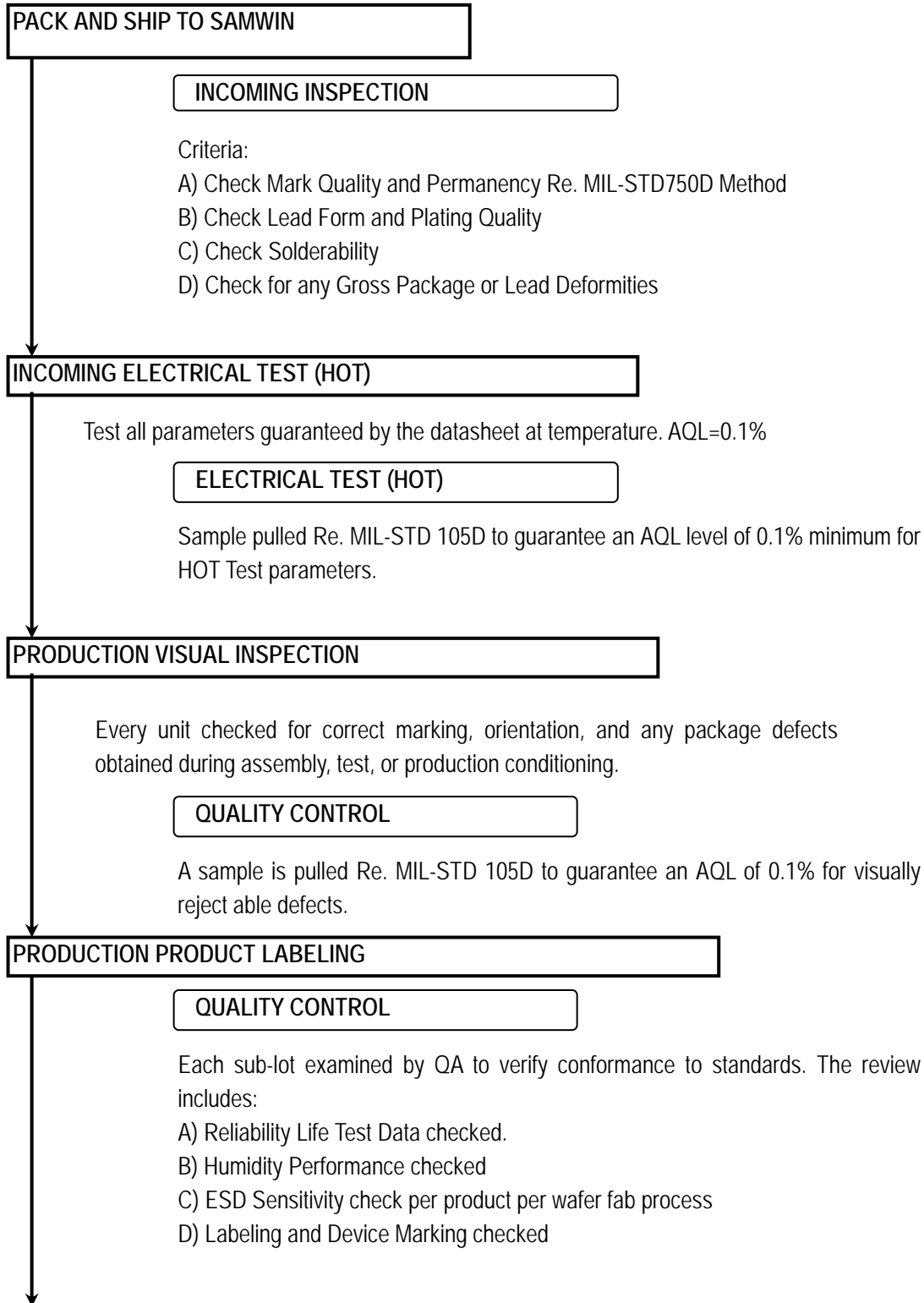
## 3.5 Assembly Process Control

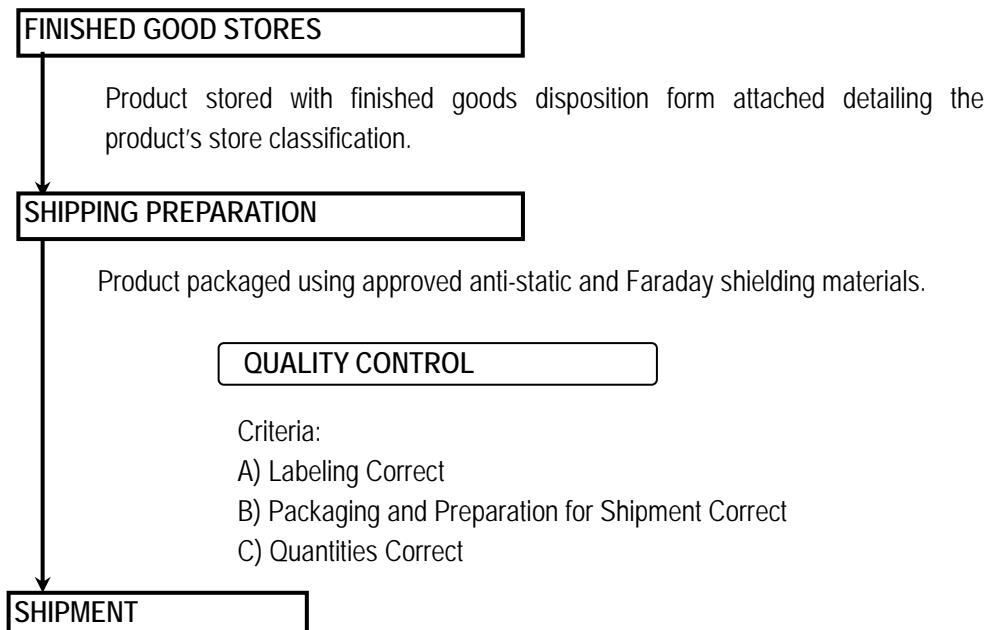






## 3.6 OQC(Out-going Quality Control)





## 4. Qualification

All product qualifications are split into three distinct steps as shown above. This same procedure is also used to qualify a change. Before a product is released for use, it must have been manufactured using a qualified wafer and package process. Before a device is released for production processing, it must also have successfully completed its required specific qualification.

The standard tests which are used for this procedure are shown in the section "Qualification Flow"

### 4.1 Change Procedure

All changes are controlled by ECN (Engineering Change Notice). All major changes are notified to those customers using products which are affected by the change.

A major change is defined as a change which affects the electrical and/or mechanical specification as defined in the datasheet or which affects the following parameters as defined hereafter:

#### 1 General Major Changes

- 1-1 Manufacturing line
- 1-2 Sequence of fabrication process cycle
- 1-3 Material
- 1-4 Electrical parameters
- 1-5 Dimensions
- 1-6 Pad location
- 1-7 Die size

#### 2 Changes specific to wafer fabrication area

- 2-1 Doping process
- 2-2 Oxide formation method
- 2-3 Equipment change
- 2-4 Layer thickness
- 2-5 Module dimensions

#### 3 Changes specific to assembly process area

- 3-1 Sawing process
- 3-2 Die attach process
- 3-3 Wire interconnect method
- 3-4 Molding process
- 3-5 Tinning process

#### 4 Changes specific to test area

- 4-1 Specification limit
- 4-2 Test coverage reduction
- 4-3 Product identification
- 4-4 Final conditioning

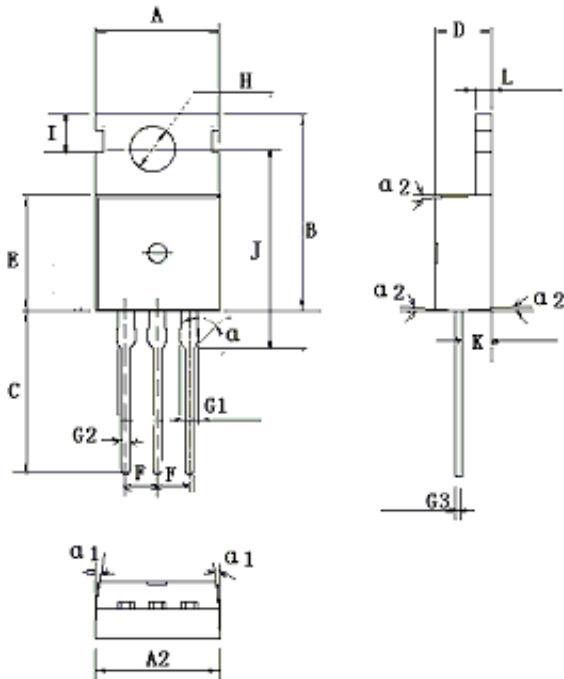
## 4.2 Qualification Flow

### General Requirements for Plastic packaged MOSFET:

	Description	Test Condition	Qualification type	Re. Standard	Acceptance
1	Temperature Cycle Test	TA = -55 °C <-> 25 °C <-> +150°C (air to air), t = 15 – 5 –15 min. / cycle, Bias = None.	1000 Cycles	Mil-Std-750D Method 1051	0/3 x 28
2	Pressure Cooker Test	TA = 121 °C +/- 2 °C, RH = 100%, P = 15PSIG, Bias = None	168 Hours	Mil-Std-202F	0/3 x 28
3	High Temperature Reverse Bias Test	TA = +150/175°C, Reverse Bias = Specification Limit X 0.8.	1000 hours	MIL-STD-750D, method 1042.3	0/3 x 28
4	High Temperature Gate Bias Test	TA = +150/175°C, Reverse Bias = Specification Limit X 0.8.	1000 hours	MIL-STD-750D, method 1042.3	0/3 x 28
5	Power Cycle Test	TA = +25 °C <-> +125 °C, Power Dissipation = ~2.5 Watts	3000 Cycles	MIL-STD-750D, method 1037.2	0/3 x 28
6	Scanning acoustic microscope			MIL-STD-750D, method 2077.3	0/3 x 50

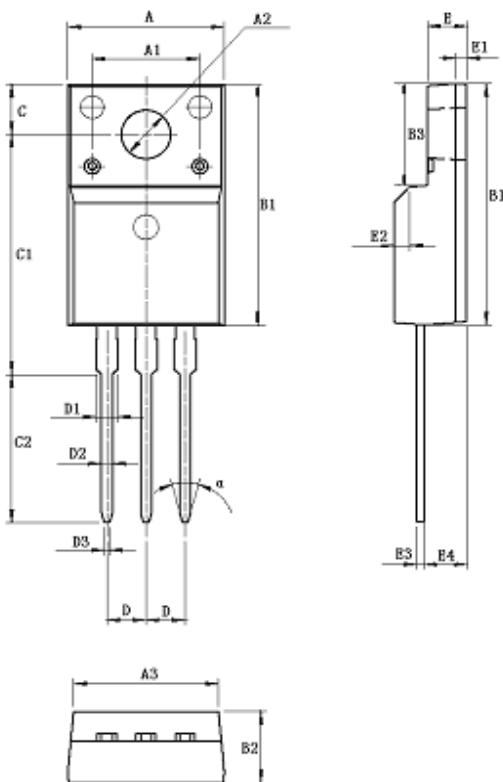
## 5. Package Dimensions

### TO-220



A(mm)	9.66~10.28
A2(mm)	9.80~10.20
B(mm)	15.6~15.8
C(mm)	12.70~14.27
D(mm)	4.30~4.70
E(mm)	8.59~9.40
F(mm)	typical 2.54
G1(mm)	1.32~1.72
G2(mm)	0.70~0.95
G3(mm)	0.4~0.60
H(mm) dia.	3.50~3.83
I(mm)	2.7~2.9
J(mm)	15.70~16.25
K(mm)	2.20~2.90
L(mm)	1.15~1.40
a(degree)	45°
a2(degree)	3°±0.5°
a3(degree)	3°±0

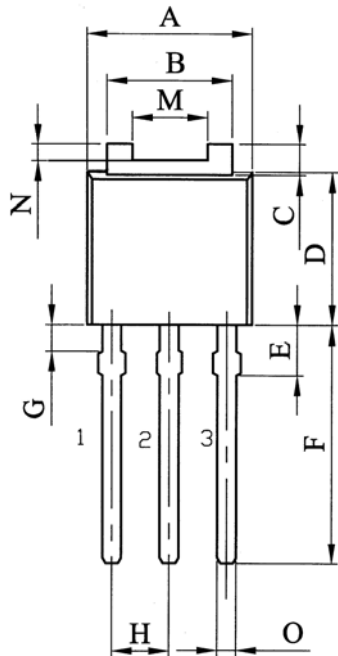
### TO-220F



A(mm)	10.16±0.20	
A1(mm)	7.00	
A2(mm)dia.	3.18±0.10	
A3(mm)	9.46±0.20	
B1(mm)	15.87±0.20	
B2(mm)	4.70±0.20	
B3(mm)	6.68±0.20	
C(mm)	3.30±0.10	
C1(mm)	15.80±0.20	
C2(mm)	9.75±0.20	
D(mm)	typical 2.54	
D1(mm)	1.47(MAX)	
D2(mm)	0.80±0.10	
D3(mm)	0.35±0.10	
E(mm)	2.54±0.20	
E1(mm)	0.70	
E2(mm)	1.0×45°	
E3(mm)	0.5	+0.10 -0.05
E4(mm)	2.76±0.20	
α(degree)	30°	

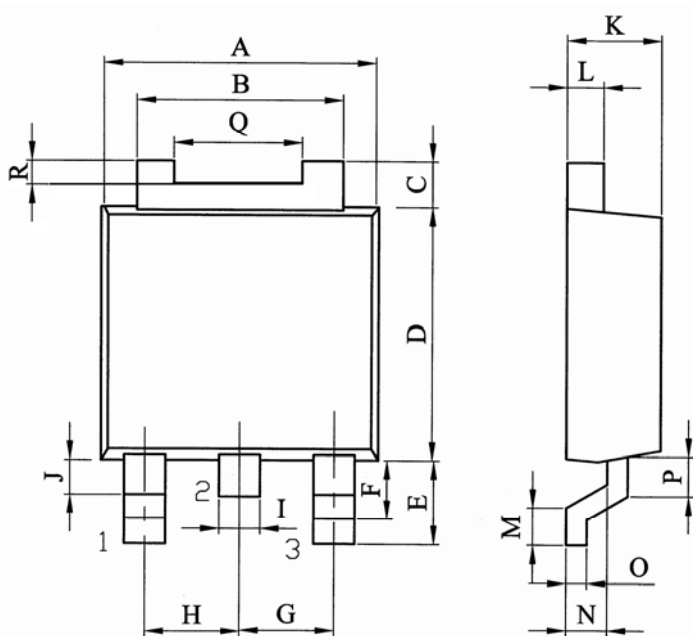


## TO-251



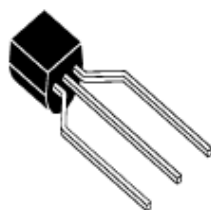
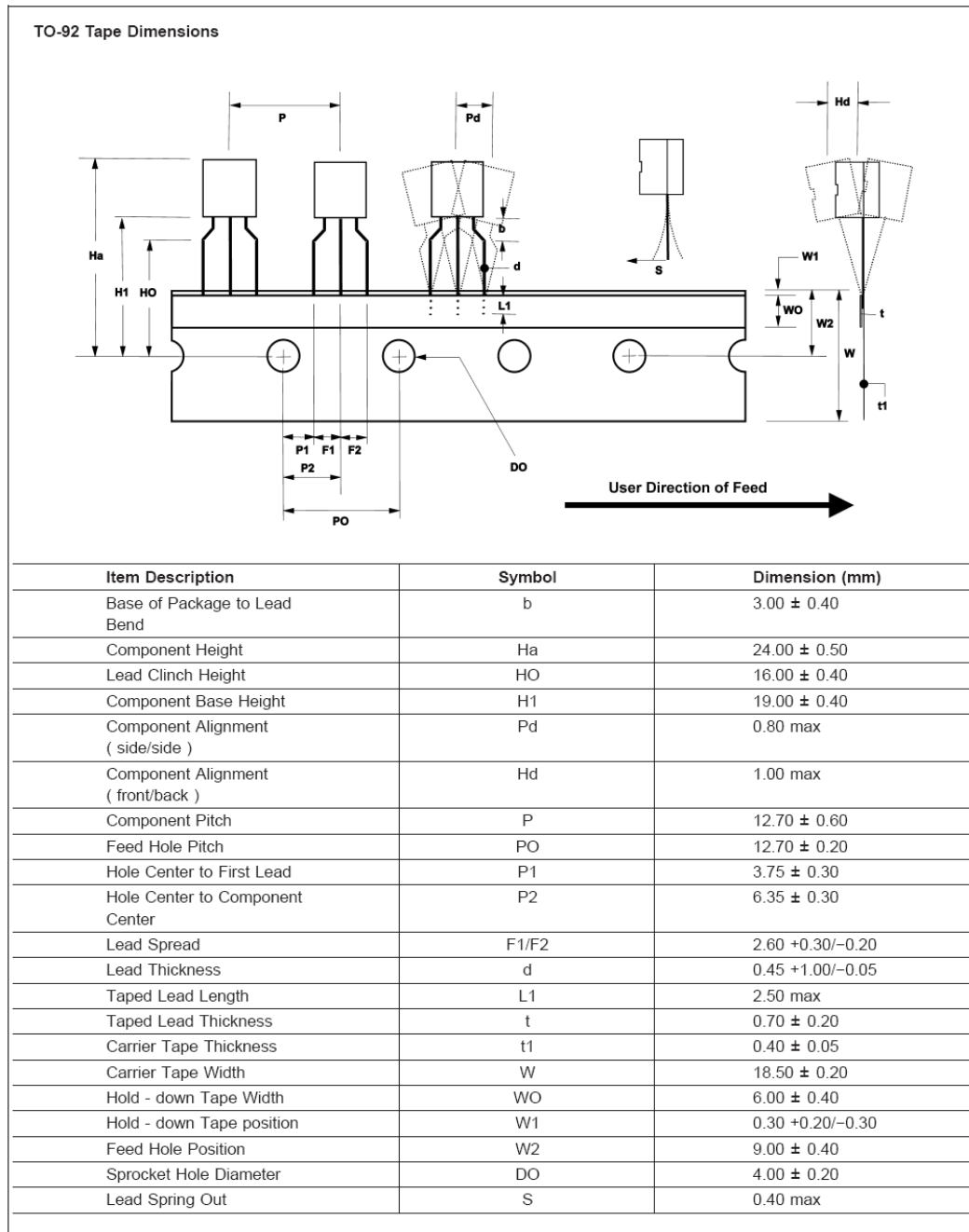
A(mm)	6.4-6.8
B(mm)	4.8-5.53
C(mm)	0.9-1.3
D(mm)	5.9-6.3
E(mm)	1.8-2.3
F(mm)	8.9-10.1
G(mm)	1.2-1.53
H(mm)	2.2-2.4
I(mm)	2.1-2.5
J(mm)	0.4-0.99
K(mm)	0.4-0.6
L(mm)	0.9-1.1
M(mm)	3.6-4.0
N(mm)	0.4-0.6
O(mm)	0.66-0.92

## TO-252



A(mm)	6.4-6.8
B(mm)	4.8-5.53
C(mm)	0.9-1.3
D(mm)	5.9-6.3
E(mm)	2.3-2.9
F(mm)	1.8-2.2
G(mm)	2.2-2.4
H(mm)	2.2-2.4
I(mm)	0.66-0.92
J(mm)	0.6-0.95
K(mm)	2.1-2.5
L(mm)	0.4-0.6
M(mm)	0.80-1.4
N(mm)	0.9-1.1
O(mm)	0.4-0.6
P(mm)	0.81-1.01
Q(mm)	3.6-4.0
R(mm)	0.4-0.6

## TO-92



TO-92 (Ammopack)



TO-92

## **6. User Information**

The user must protect components against EOS and ESD damages by grounding personal and workstations.

## **7. Environmental Information**

The SAMWIN Environmental Policy aims at:

- Reducing the use of harmful chemicals in its processes
- Reducing the content of harmful materials in its products
- Using re-cyclable materials wherever possible
- Reducing the energy content of its products

As part of that plan, Ozone Depleting Chemicals are being replaced either by SAMWIN or its subcontractor's processes.

## 8. Other Data

### 8.1 Approval Certificate



FAB ISO 9001



FAB ISO 14001



Assembly ISO 16949



Assembly ISO 14001



Assembly ISO 2000



Assembly PHILIPS Semiconductors Certificate



TO-220 SGS report 2006.Aug



TO-220F SGS report 2006.Aug

## 8.2 Datasheet Reference

Direct access on the web to datasheet at:

<http://www.samwinsemi.com>

## 8.3 Address Reference

All enquiries relating to this document should be addressed to the following:

**Samwin South Semiconductors**  
**2005, A Building,**  
**Cyber Times, Tianan Cyber Park,**  
**Futian District, Shenzhen, China**  
**Telephone (86) 755 83391818**  
**Telefax (86) 755 83476838**

**Remarks:**

The information given in this document is believed to be accurate and reliable. However, no responsibility is assumed by SAMWIN for its use. No specific guarantee or warranty is implied or given by this data unless agreed in writing elsewhere.

SAMWIN reserve the right to update or modify this information without notification, at any time, in the interest of providing the latest information.