

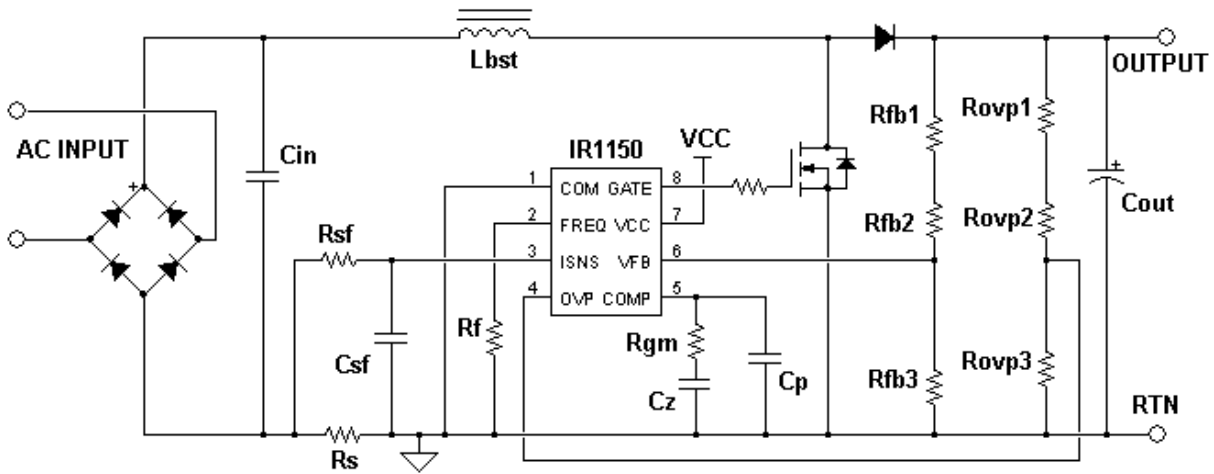
**One Cycle Control  $\mu$ PFC Circuit Featuring the IR1150S IC**

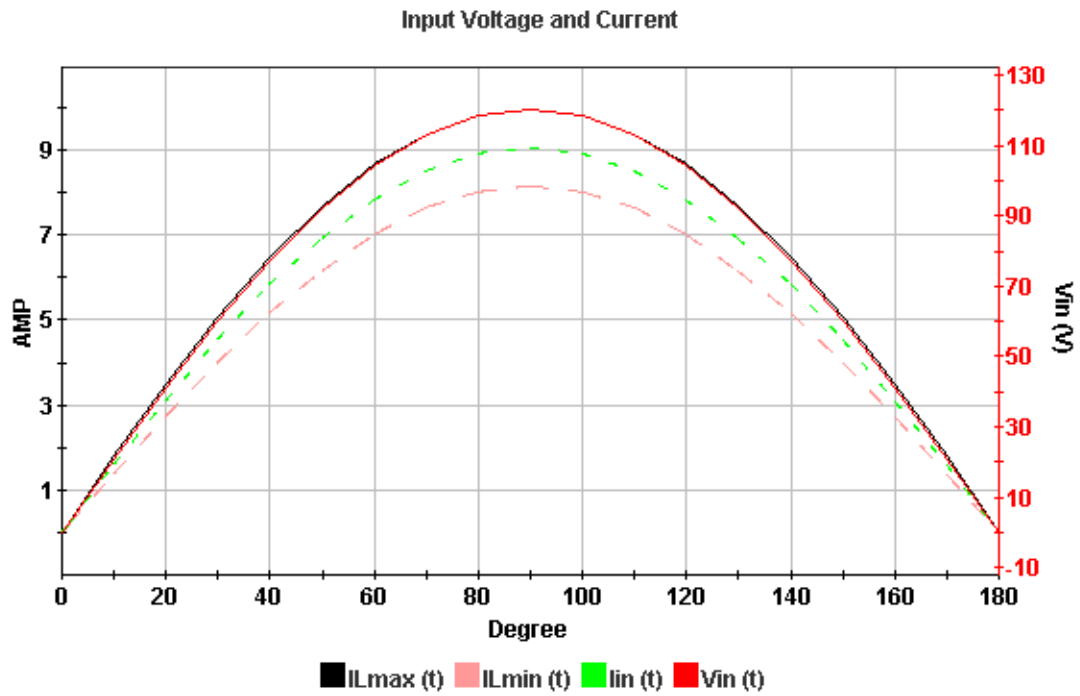
**Operating Conditions:**

Input		Output	
Min Input Voltage:	<b>85 V</b>	Switching Frequency:	<b>80 kHz</b>
Max Input Voltage:	<b>264 V</b>	Hold-up Time:	<b>20 ms</b>
Input AC Frequency:	<b>50 Hz</b>	Choke Ripple Current:	<b>20 %</b>
Start-up Time:	<b>50 ms</b>	Output Power:	<b>500 W</b>
Target Efficiency:	<b>92 %</b>	Output Voltage:	<b>385 V</b>
		Output Voltage (min):	<b>300 V</b>
		Output Cap Tolerance:	<b>10 %</b>
		OVP Threshold:	<b>425 V</b>

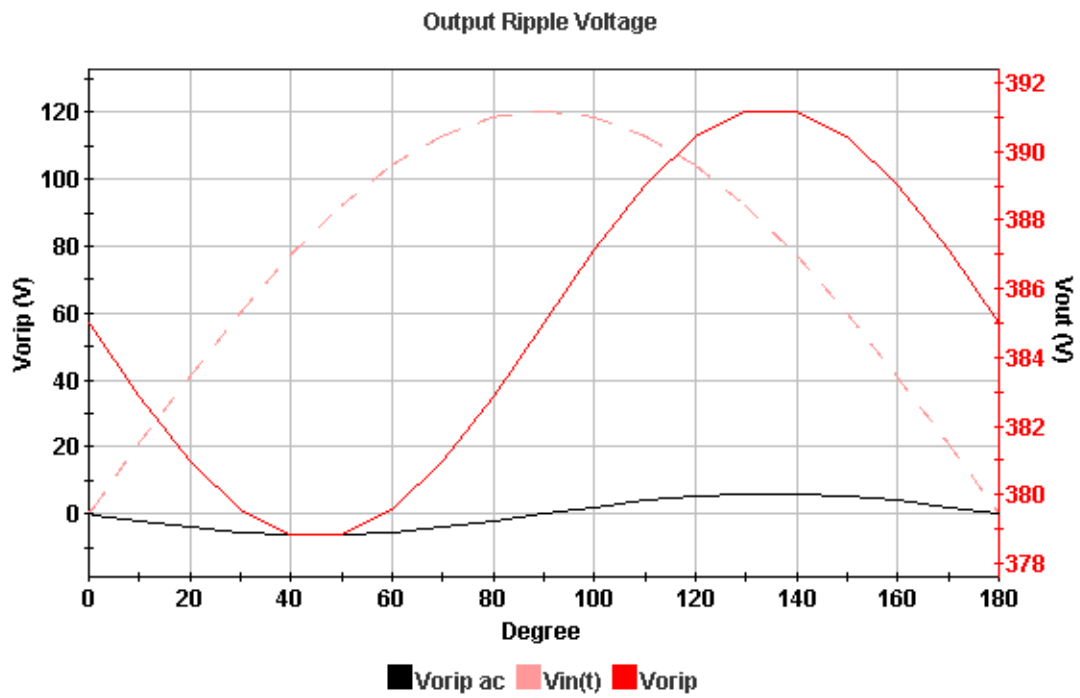
**Calculation Result:**

Output Conditions			Component Values			
Max Input Power	543	W	<b>Component</b>	<b>Ref Des</b>	<b>Std Value</b>	<b>Calc Value</b>
Input RMS Current	6.39	A	High Freq Input Cap	Cin	680 nF	0.50 $\mu$ F
Input Peak Current	9.04	A	Boost Choke Value	Lbst	620 $\mu$ H	571 $\mu$ H
Input Average Current	5.76	A	Output Capacitor	Cout	470 $\mu$ F	382 $\mu$ F
Input Pk Voltage (min)	120	V	Output Voltage Rset	Rfb3	18.7 kOhm	18.5 kOhm
Duty Cycle - low line	0.69		Output OVP Rset	Rovp3	18.2 kOhm	17.9 kOhm
Ripple Current	1.81	A	Current Sense Res	Rs		0.072 Ohm
Peak Inductor Current	9.95	A	Zero Capacitor	Cz	330 nF	331 nF
V Current Sense	0.76	V	Gain Resistor	Rgm	3.01 kOhm	2.96 kOhm
Peak Current Limit	13.82	A	Pole Capacitor	Cp	3.9 nF	4.03 nF
Input Pk Ovld Current	10.44	A	Current Sense Filter Capacitor	Csf	1 nF	1.00 nF
<b>Power Distribution</b>			Current Sense Filter Resistor	Rsf	100 Ohm	100 Ohm
Power Dissipation Rfb	71.6	mW	Timing Resistor	Rf	102 kOhm	101.1 kOhm
Power Diss Rovp	71.4	mW	Rfb1, Rfb2, Rovp1 and Rovp2 are 499 kOhms each			
Power Rs	2.96	W				

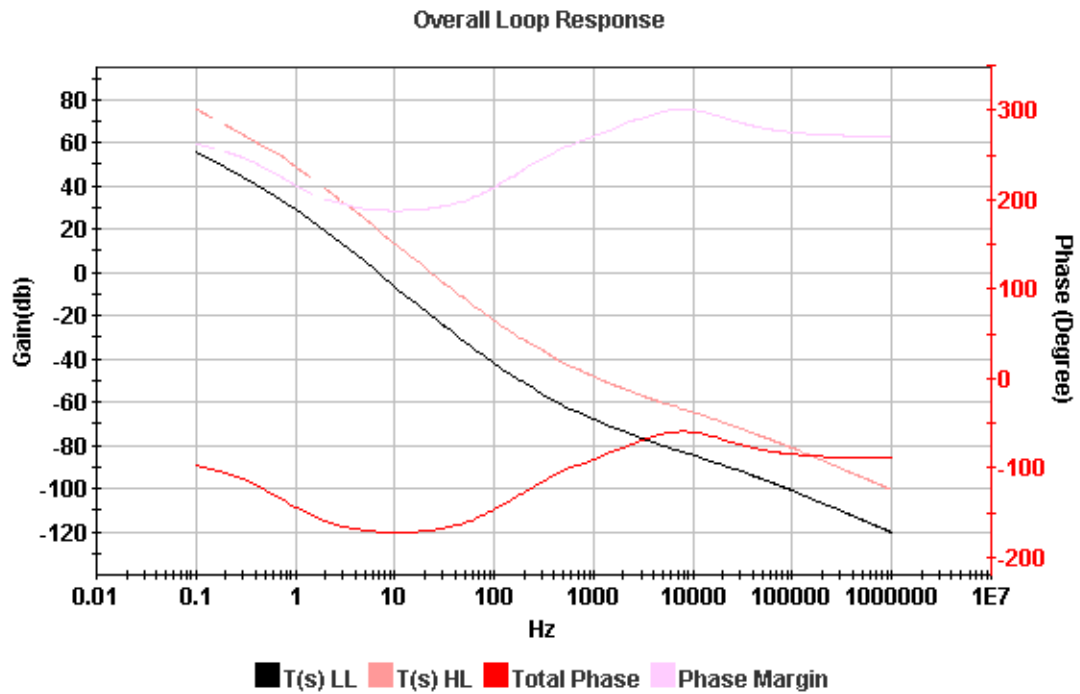




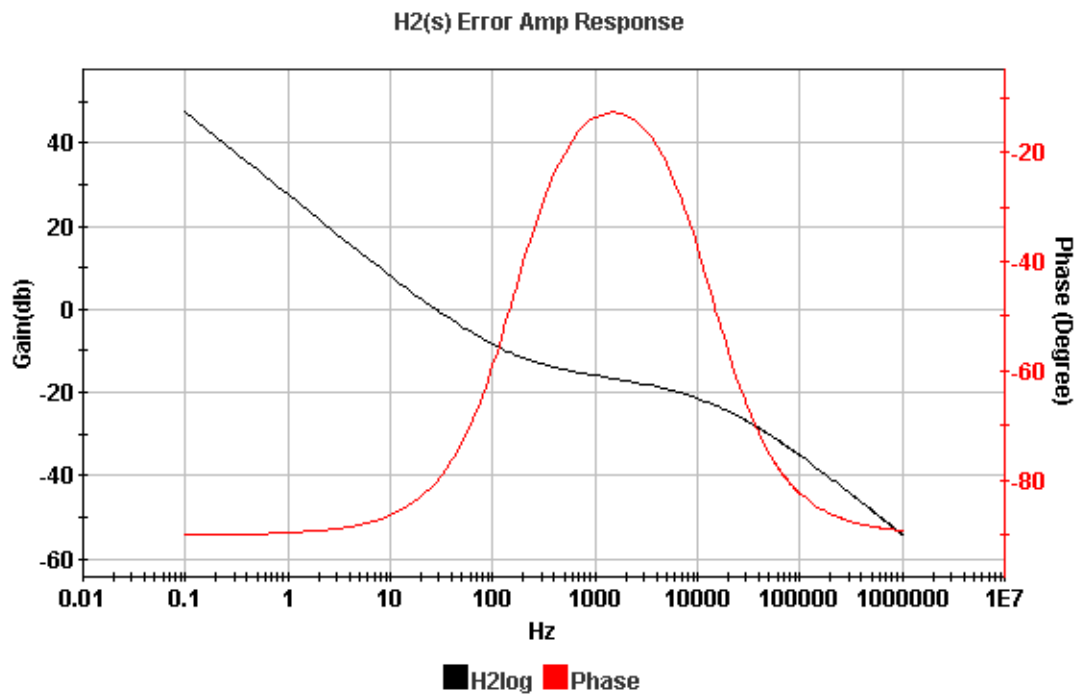
Graph 1: Input voltage and current relationship for this IR1150 power factor correction circuit.



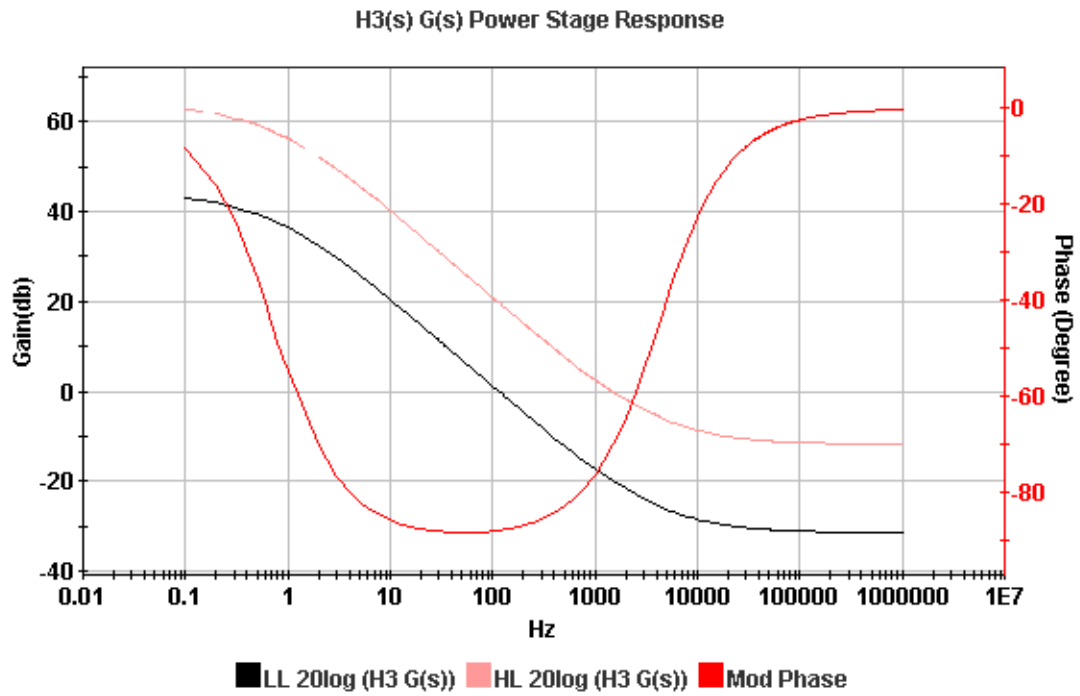
Graph 2: Output voltage ripple amplitude relative to the AC input voltage for this design.



Graph 3: This is the overall feedback loop response of the power factor correction circuit showing phase and gain.



Graph 4: This is the error amplifier response of the power factor correction circuit showing phase and gain.



Graph 5: This is the power stage response of the power factor correction circuit showing phase and gain.

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