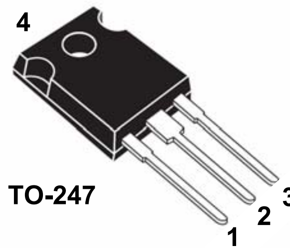
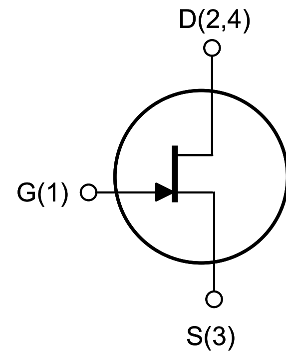
Normally-OFF Trench Silicon Carbide Power JFET

Product Summary		
BV_{DS}	1200	V
$R_{DS(ON)max}$	0.125	Ω
$Q_{g,typ}$	25	nC

Features:
- Compatible with Standard PWM ICs
- Positive Temperature Coefficient for Ease of Paralleling
- Temperature Independent Switching Behavior
- 175 °C Maximum Operating Temperature
- $R_{DS(on)max}$ of 0.125 Ω
- Voltage Controlled
- Low Gate Charge
- Low Intrinsic Capacitance





Internal Schematic

Applications:
- Solar Inverter
- SMPS
- Power Factor Correction
- Induction Heating
- UPS
- Motor Drive

MAXIMUM RATINGS, at T_j = 25 C unless otherwise stated

Parameter	Symbol	Conditions	Value	Unit
Continuous Drain Current	I_{D25}	T_C = 25 °C	15	A
	I_{D100}	T_C = 100 °C	12	
Pulsed Drain Current	I_{DM}	T_C = 25 °C	25	A
Avalanche Energy, single pulse	E_{AS}	I_D = 6 A, V_{DD} = 50V, Tj < 175 °C	TBD	mJ
Avalanche Energy, repetitive	E_{AR}		2	
Avalanche Current, repetitive	I_{AR}		6	A
Short Circuit Withstand Time	t_{SC}	V_{DD} < 1200 V, T_j < 175 °C	50	us
Power Dissipation	P_D	T_C = 25 °C	136	W
DC Gate-Source Voltage	V_{GS}		-15 to +3	V
AC Gate-Source Voltage	V_{GS}	t_P < 100ns	-15 to +15	V
Operating and Storage Temperature	T_j, $T_{j,stg}$		-55 to +175	°C

THERMAL CHARACTERISTICS

Parameter	Symbol	Conditions	Value			Unit
			Min	Typ	Max	
Thermal Resistance, junction-case	$R_{th,JC}$		-	1.1	-	°C / W
Thermal Resistance, junction-ambient	$R_{th,JA}$		-	50	-	°C / W

STATIC CHARACTERISTICS, at T_j = 25 C unless otherwise stated

Parameter	Symbol	Conditions	Value			Unit
			Min	Typ	Max	
Drain-Source Blocking Voltage	BV_{DS}	V_{GS} = 0 V, I_D = 1000 µA	1200	-	-	V
Drain-Source Leakage Current	I_{DSS}	V_{DS} = 1200 V, V_{GS} = 0 V	-	-	1000	uA
		V_{DS} = 1200 V, V_{GS} = -5 V	-	100	-	
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = 1 V, I_D = 34 mA	0.75	1.00	1.25	V
Gate-Source Leakage Current	I_{GSS}	V_{GS} = 3 V	-	100	-	mA
		V_{GS} = -15 V	-	-0.2	-	
Drain-Source On-resistance	$R_{DS(on)}$	I_D = 12 A, V_{GS} = 3.0 V, T_j = 25 °C	-	0.115	0.125	Ω
		I_D = 12 A, V_{GS} = 3.0 V, T_j = 150 °C	-	0.299	-	
Gate Resistance	R_G	f = 1 MHz, open-drain	-	TBD	-	Ω

DYNAMIC CHARACTERISTICS, at T_j = 25 C unless otherwise stated

Parameter	Symbol	Conditions	Value			Unit
			Min	Typ	Max	
Total Gate Charge	Q_g	V_{DS} = 600 V, I_D = 12 A, V_{GS} = 0 V to + 3 V	-	25	-	nC
Gate-Source Charge	Q_{gs}		-	8.3	-	
Gate-Drain Charge	Q_{gd}		-	16.7	-	
Turn-on Delay (Resistive Load)	t_{on}	V_{DS} = 600 V, I_D = 12 A, C_{BP} = 33 nF, R_{CL} = 220 Ω, *Figure 9*	-	20	-	ns
Rise Time (Resistive Load)	t_r		-	70	-	
Turn-off Delay (Resistive Load)	t_{off}		-	30	-	
Fall Time (Resistive Load)	t_f		-	70	-	
Turn-on Energy	E_{on}		-	TBD	-	mJ
Turn-off Energy	E_{off}		-	TBD	-	
Total Switching Energy	E_{ts}		-	TBD	-	
Input Capacitance	C_{iss}	V_{DS} = 100 V	-	584	-	pF
Output Capacitance	C_{oss}		-	62	-	
Reverse Transfer Capacitance	C_{rss}		-	61	-	
Effective Output Capacitance, energy related	$C_{o(er)}$	V_{DS} = 0 V to 480 V, V_{GS} = 0 V	-	40	-	

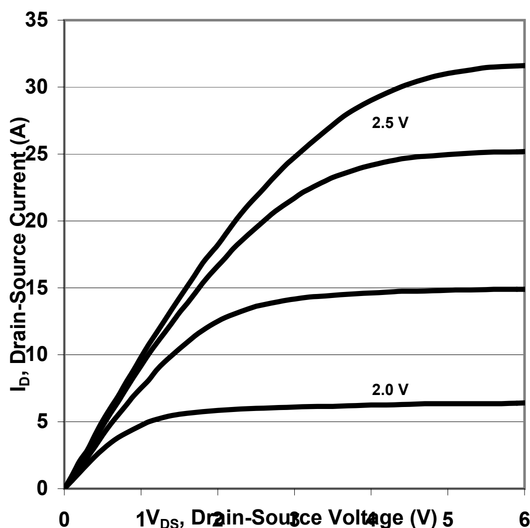


Figure 1. Typical Output Characteristics
$I_D = f(V_{DS})$; $T_j = 25$ °C; parameter: V_{GS}

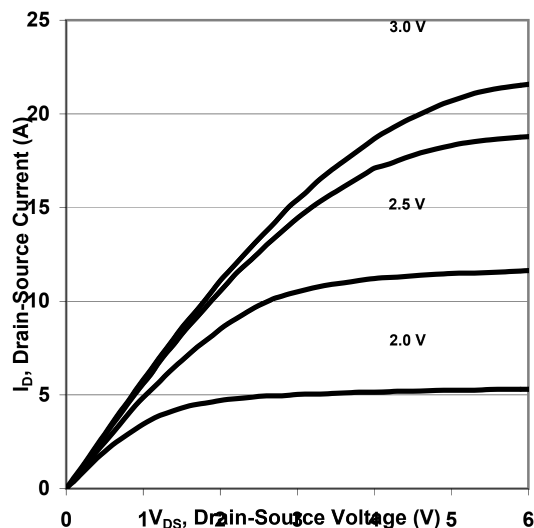


Figure 2. Typical Output Characteristics
$I_D = f(V_{DS})$; $T_j = 100$ °C; parameter: V_{GS}

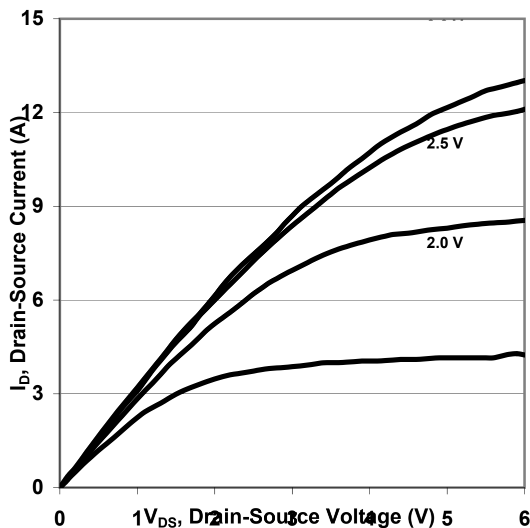


Figure 3. Typical Output Characteristics
$I_D = f(V_{DS})$; $T_j = 175$ °C; parameter: V_{GS}

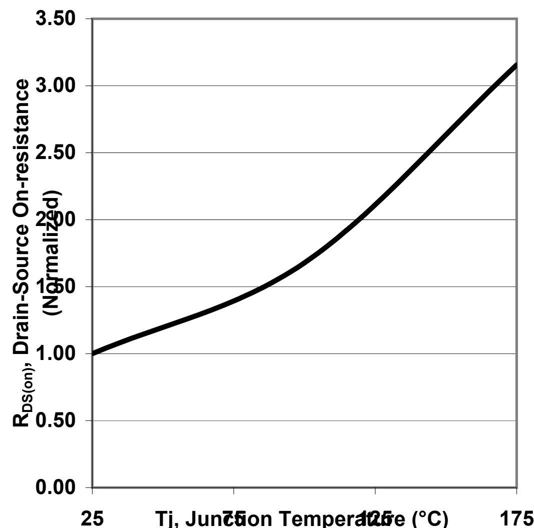


Figure 4. Drain-Source On-resistance
$R_{DS(on)} = f(T_j)$; $V_{GS} = 3.0$ V, $I_D = 0.5 * I_{D25}$

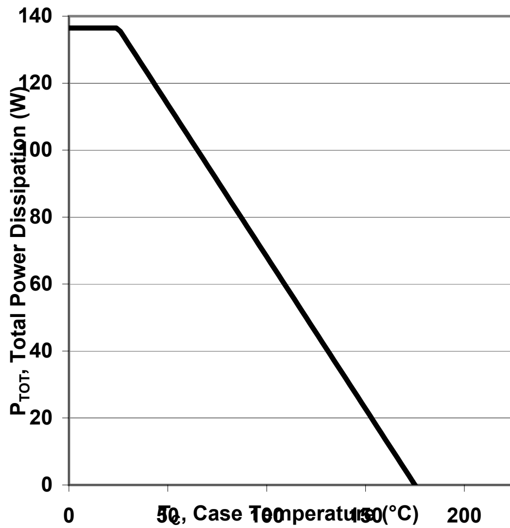


Figure 5. Power Dissipation

$P_{tot} = f(T_c)$

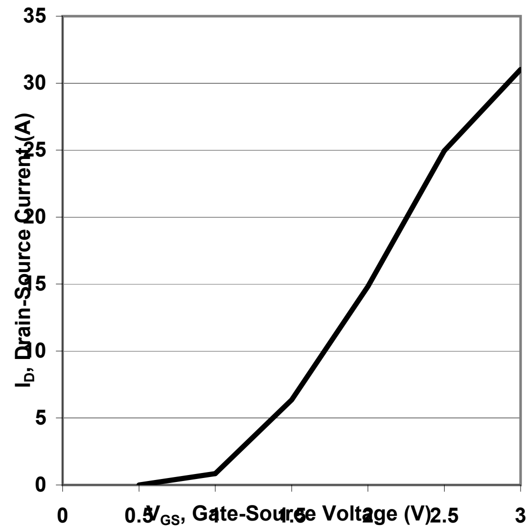


Figure 6. Typical Transfer Characteristics

$I_D = f(V_{GS}); V_{DS} = 5\ V$

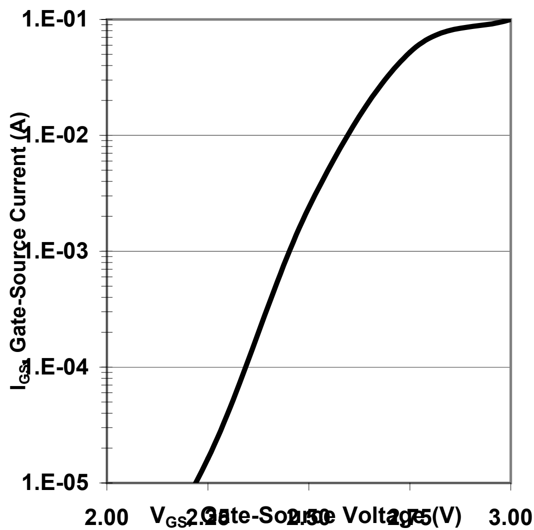


Figure 7. Gate-Source Current

$I_{GS} = f(V_{GS})$

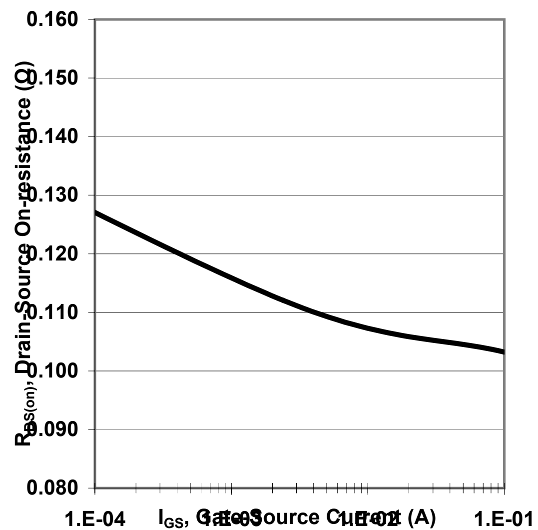


Figure 8. Drain-Source On-resistance

$R_{DS(ON)} = f(I_{GS}); I_{DS} = 12\ A$

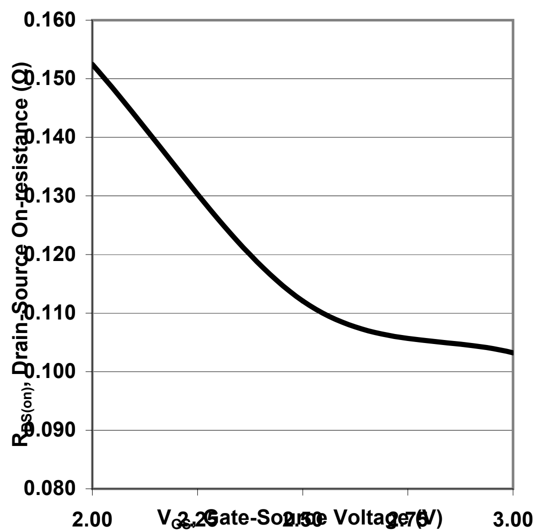


Figure 9. Drain-Source On-resistance
$R_{DS(ON)} = f(V_{GS})$; $I_{DS} = 12$ A

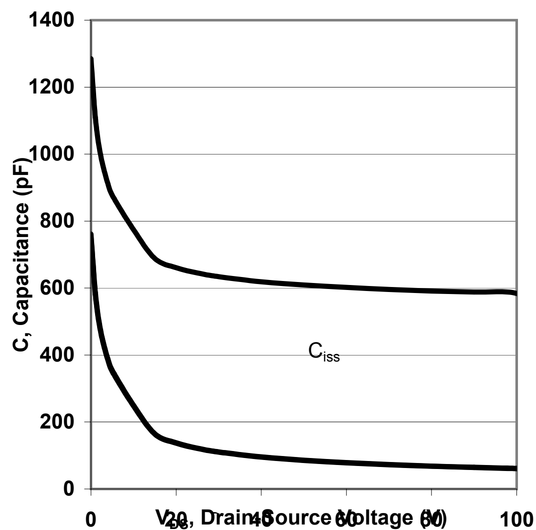


Figure 10. Typical Capacitance
$C = f(V_{DS})$; $V_{GS} = 0$ V; $f = 1$ MHz

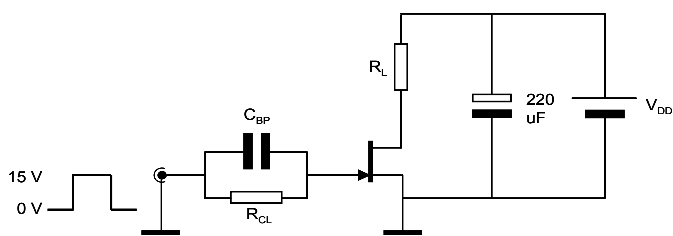


Figure 11. Resistive Load Switching Circuit

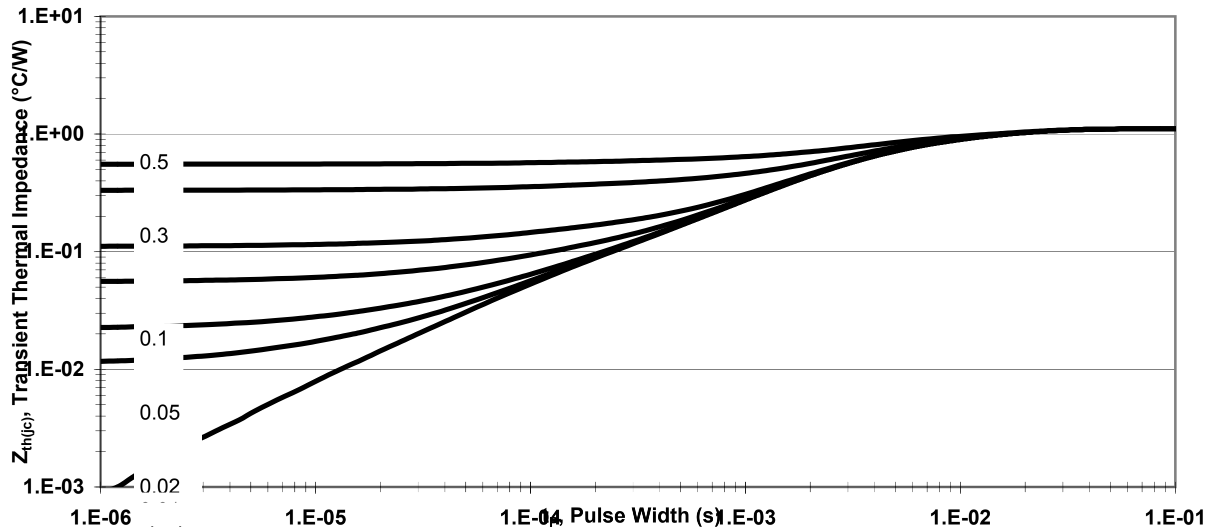


Figure 12. Transient Thermal Impedance
$Z_{th(jc)} = f(t_P)$; parameter: Duty Ratio

A. Device Overview

The SJEP120R125 is an enhancement-mode (EM) silicon carbide (SiC) Vertical Junction Field Effect Transistor (JFET) optimized for use in high-voltage, high-power, high-frequency power management applications. Due to the superior material properties of the SiC semiconductor and patented trench architecture, the SJEP120R125 delivers best-in-class performance in both hard-switching and soft-switching applications. The SJEP120R125 is designed to be a replacement for MOSFETs and IGBTs and delivers the following performance advantages:

No saturation voltage: Due to unipolar conduction in the JFET structure (i.e. no conductivity modulation) there is not a saturation voltage to overcome before output current is available enabling lower conduction losses and higher systems efficiencies.

No tail-current: No tail current is present at the turn-off transition enabling lower switching losses and higher practical switching frequencies.

Low on-resistance: Lowest specific-on-resistance of all 1200V-class semiconductor devices due to the SiC material enables reduced conduction losses and higher system efficiencies.

Low Intrinsic Capacitance: Lower device capacitances allow for reduced gate charge requirements and high-frequency switching applications.

Positive Temperature Coefficient: Allows multiple die to be paralleled easily and without concerns for unbalanced current sharing or thermal runaway.

No Body Diode: There is not an intrinsic body diode in the JFET structure. A SiC SBD can be co-packed as required by the application to enable the lowest possible switching losses.

B. Device Structure

Figure 13 illustrates the simplified schematic representation of the SJEP120R125. Much like a BJT, gate-source and gate-drain junctions are p-n diodes. Like all three-terminal semiconductor devices, the gate-source, gate-drain, and drain-source junctions act as non-linear, voltage-dependent capacitances in the circuit. The SJEP120R125 is a based on a vertical-channel, trench structure, thus no current flows laterally in the device and very high current densities are achieved. The SJEP120R125 does not have a p-n junction between drain-source and therefore has no intrinsic body diode. The control methodology is similar to that of a BJT, but the switching performance is characteristic of a unipolar device because device there is no conductivity modulation in the channel.

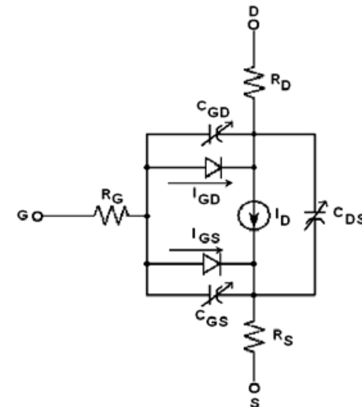


Figure 13. Equivalent Circuit of SJEP120R125

C. Gate Driver

1. Low-side Switching Applications:

The SJEP120R125 is designed to be a direct replacement for MOSFETs and IGBTs in ground-referenced, low-side switching applications with only minor modifications to the gate drive circuitry. Figure 14 shows the recommended configuration using a 0V/+15V PWM/driver signal, which includes the addition of a resistor (R_{CL}) in parallel with a capacitor (C_{BP}) between the driver/PWM IC output and the gate resistor (R_g). These components serve four primary functions:

a. Fast delivery and removal of gate charge to the SJEP120R125, thus improving the turn-on and turn-off times.
b. Level-shifting of the +15V output from the PWM/driver IC to +2.5-3.0V as selected by the user.
c. Reflection of a negative voltage on the gate-source junction at the turn-off transition to improve the turn-off time and improve EMI immunity of the gate-source signal.
d. Limit the continuous current sourced from the PWM/driver IC during the on-state.

Figure 15 is a waveform showing the PWM/driver IC output and SJEP120R125 gate-source voltage obtained using this configuration. The selections of R_{CL} and C_{BP} are discussed in section C.3.

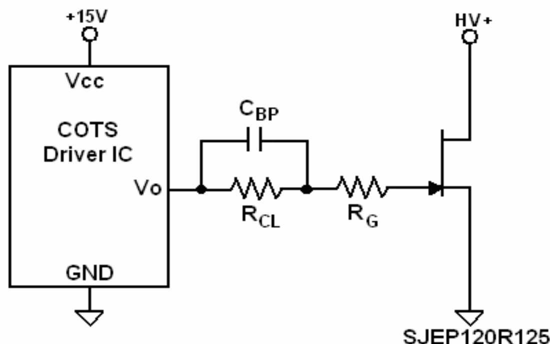


Figure 14. Recommended Driver/IC Interface

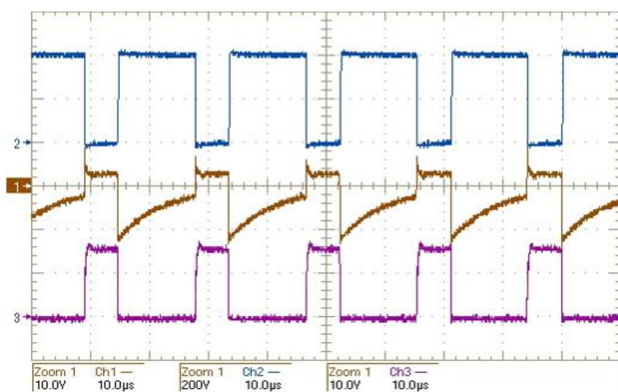


Figure 15. Switching waveforms for 0/+15V PWM/driver IC level shifted to +3V. V_{DS} (top, 200V/div), V_{GS} (middle, 10V/div), and V_O (bottom, 10V/div)

2. High-side Switching Applications

In addition to the use of RCL and CBP as described in section C.1., the use of a negative voltage rail for the PWM/driver IC is recommended when the SJEP120R125 is used in a high-side switching application. This configuration improves the EMI immunity of the gate-source voltage and prevents dV/dt induced turn-on that could result from operation in a half-bridge or full-bridge configuration. Figure 16 shows the recommended configuration using a -12V/+5V PWM/driver output. Figure 17 is a waveform showing the PWM/driver IC output and SJEP120R125 gate-source voltage obtained using this configuration. The selections of R_{CL} and C_{BP} are discussed in section C.3.

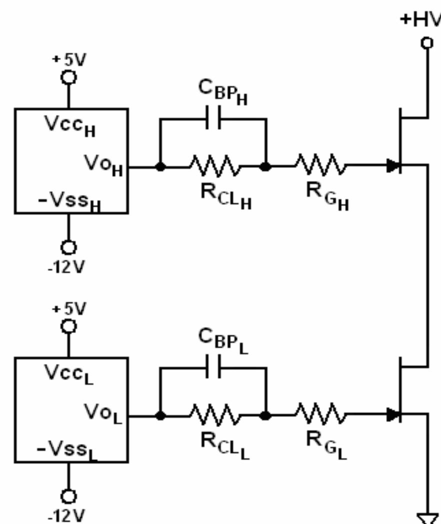


Figure 16. Recommended Driver/IC Interface for high-side switching applications.

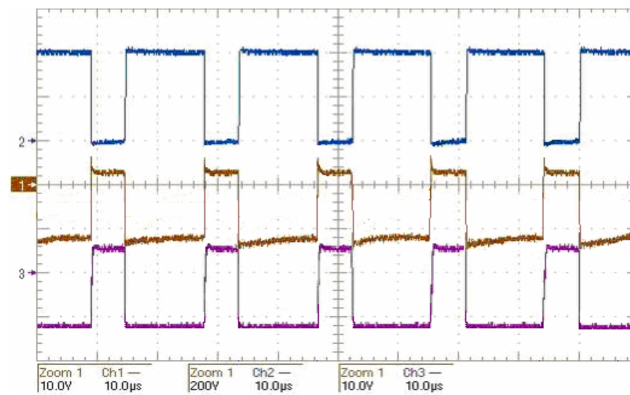


Figure 17. Switching waveforms for -12V/+5V PWM/driver IC level shifted to +3V. V_{DS} (top, 200V/div), V_{GS} (middle, 10V/div), and V_O (bottom, 10V/div)

3. R_{CL} and C_{BP} Selection

The appropriate C_{BP} value is selected based on Q_g of the SJEP120R125 and is independent PWM/driver IC supply rail voltages. Parasitic circuit effects can influence the selection of C_{BP}, so one particular value is C_{BP} is not necessarily appropriate for all applications. Rather a range of C_{BP} values to be evaluated empirically is suggested to the user as defined by Equation 1:

$$\frac{2 * Q_g}{V_{cc} - V_{gs}} \leq C_{BP} \leq \frac{4 * Q_g}{V_{cc} - V_{gs}}, \quad (1)$$

where V_{cc} is the PWM/driver IC output voltage and V_{gs} is the desired gate-source voltage of the SJEP120R125.

R_{CL} is used to limit the continuous current flowing from the PWM/driver IC through the gate-source diode (Figure 7) of the SJEP120R125, thus setting the gate-source voltage. The maximum recommended gate-source current is 50mA. It is recommended that the maximum steady-state (DC) gate voltage be not exceed +3.0 V; however a gate-source voltage pulse to +15V may be applied during the turn-on transition. The selection of R_{CL} requires the following information:

a. V_O = Positive output voltage of the PWM/driver IC
b. V_{gs} = Desired SJEP120R125 gate-source voltage
c. I_{gs} = Gate-source diode current at the desired gate-source voltage. IGS can be estimated from Figure 7.

The recommended value of R_{CL} is defined by Equation 2:

$$R_{CL} = \frac{V_O - V_{gs}}{I_{gs(@Vgs)}} \qquad (2)$$

D. Resistive Load Switching Waveforms

A simplified schematic of the resistive load switching circuit is show in Figure 18. The resulting switching waveforms are shown in Figures 19-21.

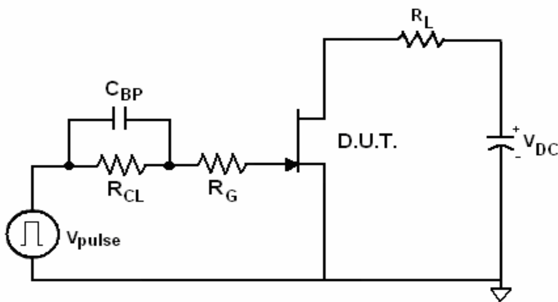


Figure 18. Resistive Load Switching Circuit

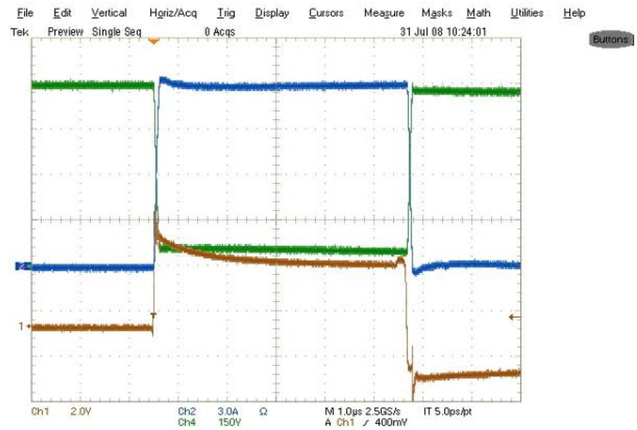


Figure 19. SJEP120R125 Switching Waveforms. V_{DS} (top, 150V/div), I_D (middle, 3A/div), and V_{GS} (bottom, 2V/div)

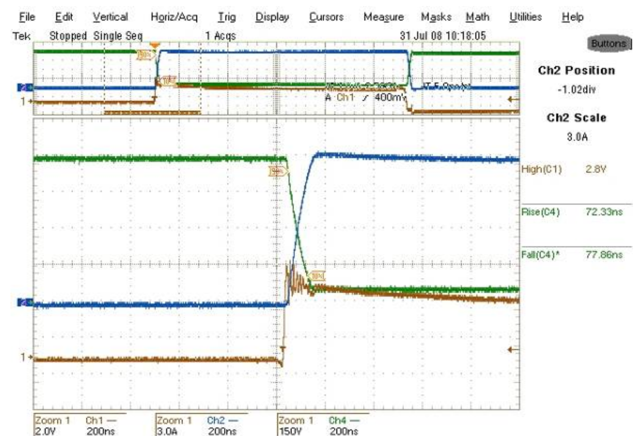


Figure 20. Rise time measurement. V_{DS} (top, 150V/div), I_D (middle, 3A/div), and V_{GS} (bottom, 2V/div)

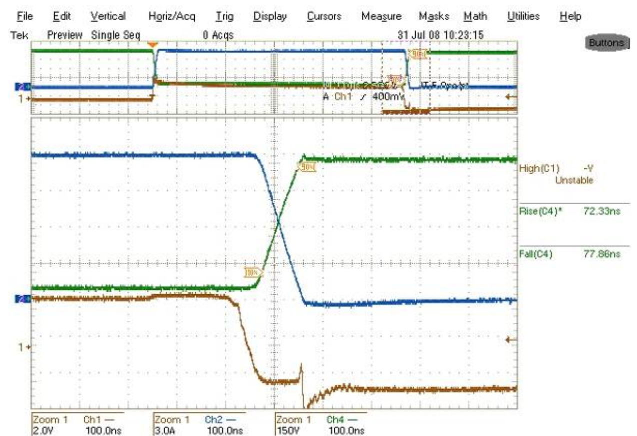


Figure 21. Fall time measurement. V_{DS} (middle, 150V/div), I_D (top, 3A/div), and V_{GS} (bottom, 2V/div)

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SemiSouth Laboratories, Inc.
201 Research Boulevard
Starkville, MS 39759 USA
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