ACT35

Preliminary, May 28, 2007

ActivePSR™ ACT35 Primary Switching Regulator

FEATURES

- Multiple Patent-Pending Primary Side Regulation Technology
- No Opto-coupler
- Best Constant Voltage, Constant Current Over All Accuracy
- Minimum External Components
- Integrated Line and Primary Inductance Compensation
- Integrated Output Cord Resistance Compensation
- Output Over-Voltage Protection
- Line Under-Voltage Protection
- Short Circuit Protection
- Over Temperature Protection
- Flyback Topology in DCM operation
- Complies with all Global Energy Efficient Regulations: 0.3W Standby Power and CEC Average Efficiency
- TO94 and SOT23-5 Packages

APPLICATIONS

- Chargers for Cell Phones, PDAs, MP3, Portable Media Players, DSCs, and Other Portable Devices and Appliances
- RCC Adapter Replacements
- Linear Adapter Replacements
- Standby and Auxiliary Supplies

GENERAL DESCRIPTION

The ACT35 belongs to the high performance, multiple patent-pending *ActivePSR™* Family of universal-input AC/DC off-line controllers for battery charger and adapter applications. It is designed for the Flyback topology working in a discontinuous conduction mode (DCM). In addition to being industry's most accurate primary side regulator, the ACT35 meets all of the global energy efficiency regulations (CEC, European Blue Angel, and US Energy Star standards) while using very few external components.

The ACT35 ensures safe operation with complete protection against all fault conditions. Built-in protection circuitry is provided for output over-voltage, output short-circuit, line under-voltage, and over-temperature conditions.

The ACT35 *ActivePSR™* is optimized for cost-sensitive applications, and utilizes Active-Semi's proprietary primary-side feedback architecture to provide accurate constant voltage, constant current (CV/CC) regulation without the need of an opto-coupler or reference device. Integrated line and primary inductance compensation circuitry provides accurate constant current operation despite wide variations in line voltage and primary inductance. Integrated output cord resistance compensation further enhances output accuracy. The ACT35 achieves excellent regulation and transient response, yet requires less than 300mW of standby power.

The ACT35 is available three power range options. The ACT35A is optimized for 2W to 3W applications. The ACT35B is optimized for 3W to 4W applications. The ACT35C is optimized for 4W to 5W applications. All three options are available in space saving 4-pin TO94 and 5-pin SOT23-5 packages.

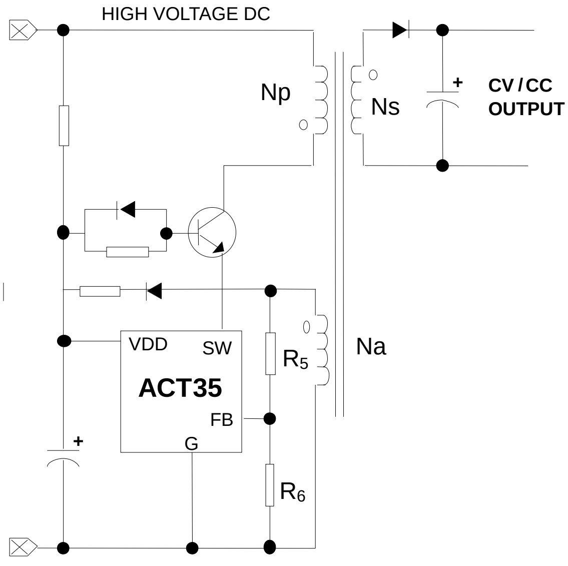
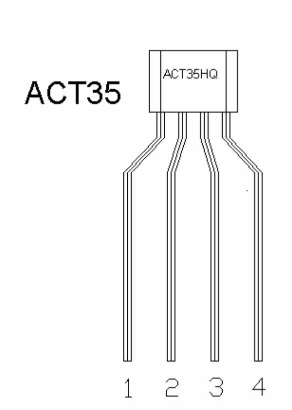


Figure 1 ACT35 Typical Application Circuit

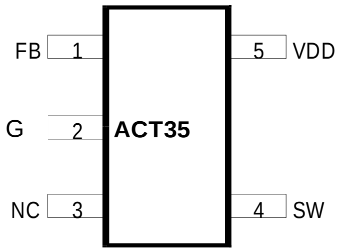
ORDERING INFORMATION

I_{LIM}	PART NUMBER	TEMP RANGE	PACKAGE	PINS	PACKING METHOD	TOP MARK
260 mA	ACT35AHQ-A	-40°C to 85° C	TO94	4	AMMO	ACT35AHQ
320 mA	ACT35BHQ-A	-40°C to 85° C	TO94	4	AMMO	ACT35BHQ
420 mA	ACT35CHQ-A	-40°C to 85° C	TO94	4	AMMO	ACT35CHQ
260 mA	ACT35AUC-T	-40°C to 85° C	SOT23-5	5	TAPE & REEL	WFJA
320 mA	ACT35BUC-T	-40°C to 85° C	SOT23-5	5	TAPE & REEL	WFJB
420 mA	ACT35CUC-T	-40°C to 85° C	SOT23-5	5	TAPE & REEL	WFJC

PIN CONFIGURATION



TO-94



SOT23-5

PIN DESCRIPTION

PIN NUMBER		PIN NAME	PIN DESCRIPTION
ACT35XHQ-A	ACT35XUC-T		
1	1	FB	Feedback from auxiliary winding
2	5	VDD	Power supply
3	4	SW	Switch drive for power NPN or MOSFET switch
4	2	G	Ground
	3	NC	No Connection

ABSOLUTE MAXIMUM RATINGS

(Note: Do not exceed these limits to prevent damage to the device. Exposure to absolute maximum rating conditions for long periods may affect device reliability.)

PARAMETER		VALUE	UNIT
VDD to G		-0.3 to 22	V
Maximum Continuous VDD Current		20	mA
FB to G		-0.3 to 6	V
SW to G		-0.3 to 22	V
Continuous SW Current		Internally limited	A
Maximum Power Dissipation	TO94 (derate TBDmW/°C above TA = 50°C)		W
	SOT23-5 (derate 5.3mW/°C above TA = 50°C)	0.53	
Junction to Ambient Thermal Resistance (θ_{JA})	TO94		°C/W
	SOT23-5	190	
Operating Junction Temperature		-40 to 150	°C
Storage Temperature		-55 to 150	°C
Lead Temperature (Soldering, 10 sec)		300	°C

ELECTRICAL CHARACTERISTICS

(V_{DD} = 15V, V_{OUT} = 5V, L_P = 1.7mH, N_P = 130, N_S = 10, N_A = 32, T_A = 25°C unless otherwise specified.)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
VDD Turn-On Voltage	V_{DDON}	V_{DD} Rising	18.5	19	20.5	V
VDD Turn-Off Voltage	V_{DDOFF}	V_{DD} Falling	7	7.5	8	V
VDD Clamp Voltage	$V_{DDCLAMP}$	10mA	19.5	20.5	21.5	V
Supply Current	I_{DD}			1.5	2	mA
Start Up Supply Current	I_{DDST}	V_{DD} = 15V, before turn-on		30	55	μA
Switching Frequency	f_{SW}	100% V_{OUT}, R_{FB1} = 30k		65		kHz
		50% V_{OUT}, R_{FB1} = 30k		32.5		
Minimum No Load Frequency		No Load		2		kHz
Effective Feedback Voltage	V_{FB}	FB in Regulation	3.45	3.50	3.55	V
Dynamic Load Step Response	ΔV_{OUT}	ΔI_{OUT} = 0 to 1A			10	%-2ms
FB Voltage OVP Threshold			5	5.25	5.5	V
Output Cord Resistance Compensation		Maximum Output Power		3.2		%
Switch Current Limit	I_{LIM}	ACT35A	-2%	260	+2%	mA
		ACT35B	-2%	320	+2%	
		ACT35C	-2%	420	+2%	
Maximum Duty Cycle	D_{MAX}	I_{SW} = 10mA	67	75	83	%
Minimum On Time	T_{ONMIN}	I_{FB} = 3.6mA	-20%	20	+20%	ns
		I_{FB} = 1mA		620		
Switch On-Resistance	R_{ON}	I_{SW} = 50mA		3.6		Ω
SW Rise Time		1nF load, 15Ω pull-up		30		ns
SW Fall Time		1nF load, 15Ω pull-up		20		ns
SW Off Leakage Current		V_{SW} = 22V,Switch is off		1	10	μA
Over-temperature Threshold				130		°C

FUNCTIONAL BLOCK DIAGRAM

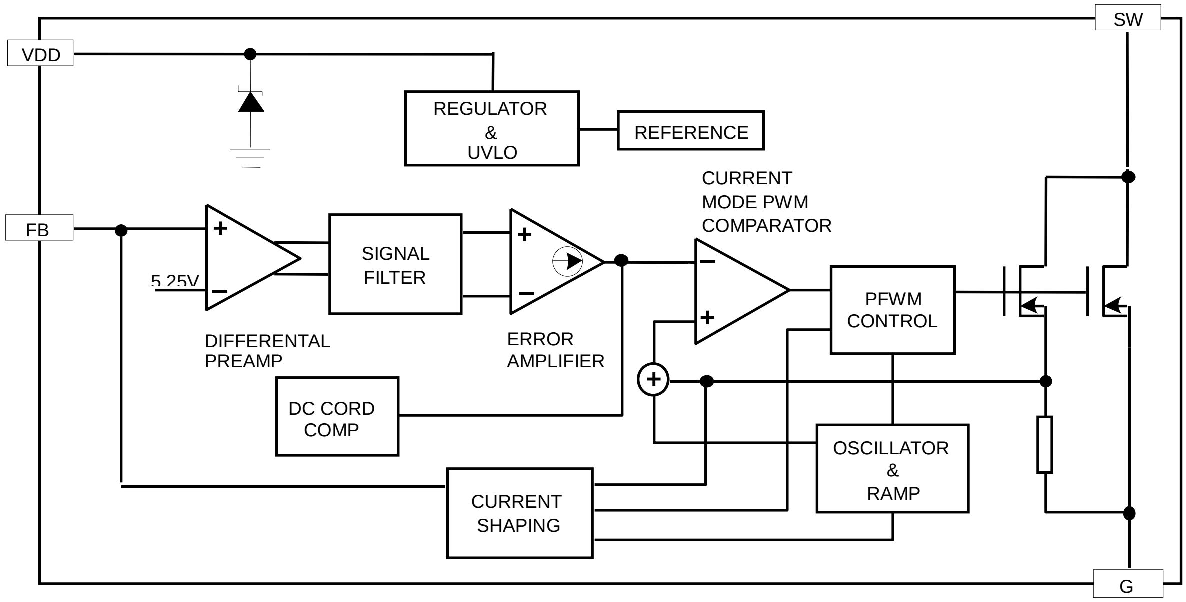


Figure 2 ACT35 Functional Block Diagram

FUNCTIONAL DESCRIPTION

Figure 2 shows the Functional Block Diagram of the ACT35. Feedback regulation is done via several circuit blocks to pre-amplify the FB pin error voltage relative to an internal reference, filter out the switching transients, and integrate the resulting useful differential error voltage for current mode PFWM (Pulse Frequency and Width Modulation) control.

SW is a driver output that drives the emitter of an external high voltage NPN transistor or N-channel MOSFET. This emitter-drive method takes advantage of the high VCBO of the transistor, allowing a low cost transistor such as ‘13003 (V_{CBO} = 700V) or ‘13002 (V_{CBO} = 600V) to be used for a wide AC input range.

STARTUP MODE

ACT35 Figure 1 VDD is the power supply terminal for the IC. During startup, the IC typically draws 30uA supply current. The bleed resistor from the rectified high voltage DC rail supplies current to VDD until it exceeds the V_{DDON} threshold of 18.5V. At this point, the IC enters normal operation with 1.5 mA supply current. Switching begins and the output voltage begins to rise. The VDD bypass capacitor must supply the IC and the NPN base drive until the output voltage builds up enough to provide power from the auxiliary winding to sustain the VDD. The V_{DDOFF} threshold is 8V, and therefore, the voltage on the VDD capacitor must not drop more than 10V while the output is charging up.

CONSTANT VOLTAGE MODE

In constant voltage operation, the IC captures the auxiliary flyback signal at FB pin (through a resistor divider network R3 and R4 in the Typical Application circuit). The FB pin is pre-amplified against the reference voltage, and the secondary side output voltage error is extracted based on Active-Semi's proprietary filter architecture. This error signal is then integrated by the Error Amplifier.

When the secondary output voltage is above regulation, the Error Amplifier output voltage decreases to reduce the switch current. When the secondary side is below regulation, the Error

Amplifier output voltage increases to ramp up the switch current to bring the secondary output back to regulation. The output regulation voltage is determined by the following relationship:

$$V_{OUTCV} = V_{REF} \bullet (1+R_5/R_6) \bullet (N_S/N_A) - V_F \qquad (1)$$

where R_3 and R_4 are top and bottom feedback resistor, N_S and N_A are numbers of transformer secondary and auxiliary turns, and V_F is the rectifier diode forward drop voltage at approximately 0.1A bias. The ACT35 includes internal feedback loop compensation to simplify application circuit design.

CONSTANT CURRENT MODE

When the secondary output current reaches a level set by the internal current limiting circuit, the IC enters current limit condition and causes the secondary output voltage to drop. As the output voltage decreases, so does the flyback voltage in a proportional manner. Internal current shaping circuitry adjusts the switching frequency based on the flyback voltage so that the transferred power remains proportional to the output voltage, resulting in a constant secondary side output current profile. The energy transferred to the output during each switching cycle is $\frac{1}{2}(L_P \bullet I_{LIM}^2) \bullet Eff$, where L_P is the transformer primary inductance, I_{LIM} is the primary peak current, and Eff is the conversion efficiency. From this formula, the constant output current can be derived:

$$I_{OUTCC} = \frac{1}{2} \bullet L_P \bullet (I_{LIM})^2 \bullet Eff \bullet f_{SW}/V_{OUT} \qquad (2)$$

where f_{SW} is the nominal switching frequency and V_{OUT} is the secondary output voltage. The constant current operation typically extends down to lower than 40% of output voltage regulation.

LIGHT LOAD MODE

When the secondary side output load current decreases to an internally set light load level, the IC's switching frequency is also reduced to save power. This enables the application to meet all current green energy standards. The switching frequency reduction is clamped at 2 kHz. However, the actual minimum switching frequency is programmable with a small dummy load (while still meeting standby power).

SHORT CIRCUIT MODE

When the secondary side output is short circuited, the ACT35 enters hiccup mode operation. In this condition, the auxiliary supply voltage collapses and the VDD voltage drops below the V_{DDOFF} threshold. This turns off the IC and causes it to restart. This hiccup behavior continues until the short circuit is removed.

OUTPUT OVER VOLTAGE PROTECTION

The ACT35 includes output over-voltage protection circuitry, which shuts down the IC when the output voltage is 40% above the normal regulation voltage or when no feedback signal is detected for 8 consecutive switching cycles. The IC enters hiccup mode when an output over voltage fault is detected.

LOOP COMPENSATION

The ACT35 integrates loop compensation circuitry for simplified application design, optimized transient response, and minimal external components.

PRIMARY INDUCTANCE COMPENSATION

The ACT35 includes built-in primary inductance compensation to maintain constant current regulation despite variations in transformer manufacturing.

PEAK INDUCTOR CURRENT LIMIT COMPENSATION

The ACT35 includes peak inductor current limit compensation to achieve constant input power over wide line and wide load range.

OUTPUT CORD RESISTANCE COMPENSATION

The ACT35 provides automatic output cord resistance compensation during constant voltage regulation, monotonically adding an output voltage correction up to a typical correction of 3.2% at full power. This feature allows for better output voltage accuracy by compensating for the output voltage droop due to the output cord resistance.

APPLICATION INFORMATION

EXTERNAL POWER TRANSISTOR

The ACT35 allows a low-cost high voltage power NPN transistor such as ‘13003 or ‘13002 to be used safely in flyback configuration. The required collector voltage rating for V_{AC} = 265V with full output load is at least 600V to 700V. As seen from Figure 5, *NPN Reverse Bias Safe Operation Area*, the breakdown voltage of an NPN is significantly improved when it is driven at its emitter. Thus, the ACT35+’13002 or ‘13003 combination meet the necessary breakdown safety requirement even though RCC circuits using ‘13002 or ‘13003 do not. Table 1 lists the breakdown voltage of some transistors appropriate for use with the ACT35.

The power dissipated in the NPN transistor is equal to the collector current times the collector-emitter voltage. As a result, the transistor must always be in saturation when turned on to prevent excessive power dissipation. Select an NPN transistor with sufficiently high current gain (h_{FEMIN} > 8) and a base drive resistor low enough to ensure that the transistor easily saturates.

Table 1 Recommended NPN Transistors

DEVICE	V_{CBO}	V_{CEO}	I_C	h_{FEMIN}	PACKAGE
MJE13002	600V	300V	1.5A	25	TO126
MJE13003, KSE13003	700V	400V	1.5A	25	TO126
STX13003	700V	400V	1A	25	TO92

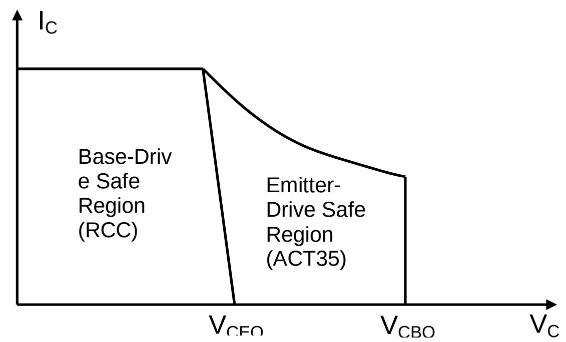


Figure 3 NPN Reverse Bias Safe Operation Area

CONSTANT OUTPUT CURRENT DESIGN

The ACT35A/B/C are able to cover 2W to 5W charger application by adjusting the feedback resistors and turn ratio of the transformer. The formula below is used to design the output constant current.

$$I_{out}=½•K•I_{LIM}•(N_P/N_S)•R_5• R_6/ (R_5+ R_6) •Eff \qquad (3)$$

K is the design constant 0.000063. EFF is the calculation efficiency. Usually 70% is used in general application. The feedback resistor R_5 is designed to have value between 24K and 36K. Table 2 lists the recommended design values for the transformer and feedback resistor R_5.

DESIGN PROCEDURE

Refer to Table 2 for initial key component value selection. Component value fine tuning is then based on the following procedure:

1) Based on the product of output voltage (Vo) and current (Io), or output power (Po), choose the closest design case from Table 2.

2) Use N_P, N_S, R_5 or R_6 based on Equation (3) to increase or decrease output current or power.

3) Use N_S, N_A, R_5 or R_6 based on Equation (1) to adjust output voltage while keeping V_{DD} around 17.5V.

DESIGN EXAMPLE #1 (5V / 750mA)

1) Based on the output power (= 5V x 750mA = 3.75W), we can choose the design case # 5 or # 6. The output current must be increased if design case # 5 is chosen. And, the output current must be reduced if design case # 6 is chosen. Assume we choose design case # 5.

2) Based on Equation (3), we can increase N_P, R_5 or R_6, or reduce N_S to increase output current. For simplicity, we can keep N_P and N_S unchanged and only adjust R_5 and R_6. Since Io must be increased 1.071 (=750mA/700mA) times, $(R_5•R_6)/(R_5+ R_6)$ must be increased to 1.071 times form the case # 5 initial component value.

$(R_5 \cdot R_6)/(R_5 + R_6)$

$= 1.071 \cdot (30k \cdot 7.77k)/(30k + 7.77k)$

Or,

$(R_5 \cdot R_6)/(R_5 + R_6) = 6.610k$ (4)

3) Since the output voltage is unchanged, we need to keep $R_6/(R_5 + R_6)$ the same value based on Equation (1).

$R_6 / (R_5 + R_6)$

$= 7.77k / (30k + 7.77k)$

Or,

$R_6 / (R_5 + R_6) = 0.206$ (5)

R5 & R6 CALCULATION

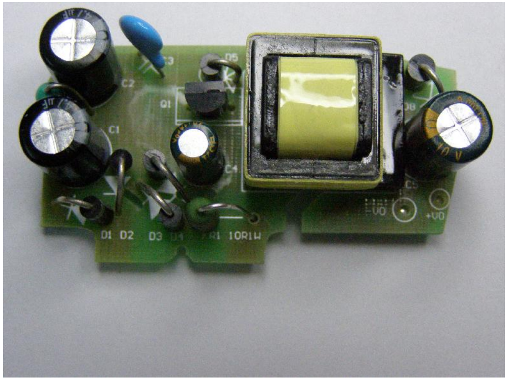
If we divide the whole Equation (4) by the whole Equation (5), we can obtain R_5 = 32.09k. We then apply this R_5 value back to Equation (5) to obtain R_6 = 8.32k.

Table 2 Initial Component Value

Design Case	Output			PSR		Transformer				Resistor network	
	V_O(V)	I_O(mA)	P_O(W)	P/N	I_{LIM}(mA)	N_P	N_S	N_A	L_M	R_5(kΩ)	R_6(kΩ)
1	5.0	400	2.0	ACT35A	260	100	13	40	1.50	30.0	7.77
2	5.0	500	2.5	ACT35A	260	130	13	40	1.80	30.0	7.77
3	5.0	600	3.0	ACT35A	260	130	11	35	2.00	30.0	7.77
4	5.0	600	3.0	ACT35B	320	130	12	38	1.80	31.6	8.16
5	5.0	700	3.5	ACT35B	320	130	10	32	1.80	30.0	7.77
6	5.0	800	4.0	ACT35B	320	130	10	32	1.80	34.8	9.09
7	5.0	800	4.0	ACT35C	420	130	12	38	1.90	29.8	7.68
8	5.0	900	4.5	ACT35C	420	130	12	38	1.90	32.4	8.35
9	5.0	1000	5.0	ACT35C	420	130	10	32	1.90	30.0	7.77

5V/700mA MOBILE PHONE CHARGER APPLICATION

◆ DEMO BOARD



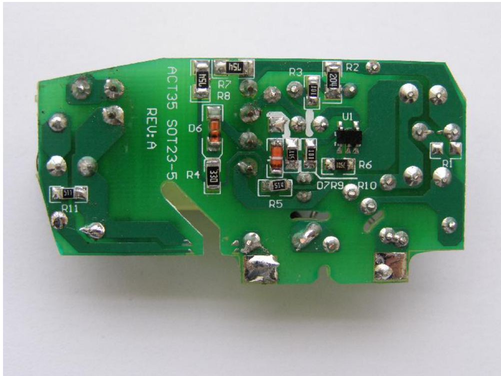


Figure 4 Demo Board Photo

◆ SCHEMATIC

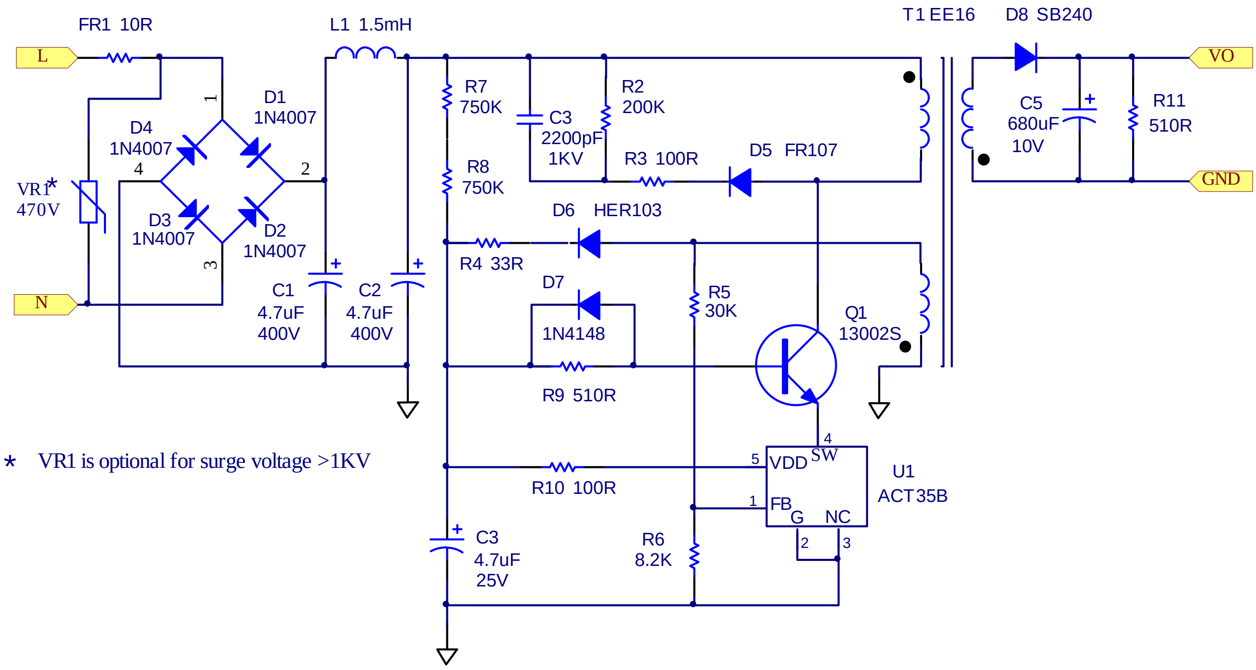


Figure 5 5V/700mA Charger Circuit

◆ BILL OF MATERIAL

Table 3 Build of Material for 5V/700mA Charger

Item	Reference	Description	QTY
1	C3	Capacitor, Ceramic, 2200p/1KV DIP	1
2	C1,2	Capacitor, Electrolytic, 4.7uF/400V, 8x11.5	2
3	C4	Capacitor, Electrolytic, 4,7uF/25V, 5x11	1
4	C5	Capacitor, Electrolytic, 680uF/10V, 6.3x11	1
5	D8	Diode, Schottky, 40V/2A SB240 DO-15	1
6	D5	Diode, Ultra Fast, FR107, DO-41	1
7	D1-D4	Diode, Rectifier, 1000V, 1A, 1N4007, DO-41	4
8	D6	Diode, Ultra Fast, 200V, 1A, HER103, DO-41	1
9	D7	Diode, Switching, 100V, 0.15A, 1N4148, DO-35	1
10	F1	Resistor, 1W, 10 ohm, 5%, DIP	1
11	L1	Inductor, 1.5mH, DIP	1
12	PCB	PCB, L*W*T=50x26x15mm, FR-4	1
13	Q1	Transistor, NPN, 600V, 1.5A, E13002S, TO-92	1
14	R4	Resistor, 33 ohm, 0805, 5%	1
15	R5	Resistor, 30K ohm, 0805, 1%	1
16	R6	Resistor, 8.2K ohm, 0805, 1%	1
17	R2	Resistor, 200K ohm, 1206, 5%	1
18	R3,10	Resistor, 100 ohm 0805, 5%	2
19	R7,8	Resistor, 750K ohm, 1206, 5%	2
20	R9,11	Resistor, 510 ohm, 0805, 5%	2
21	T1	Transformer, Lp=1.7mH, EE16	1
22	U1	IC ACT35B TO23-5	1
23	VR1*	Varistor, TVR05471KSY, 470V, DIP	1

◆ PCB LAYOUT

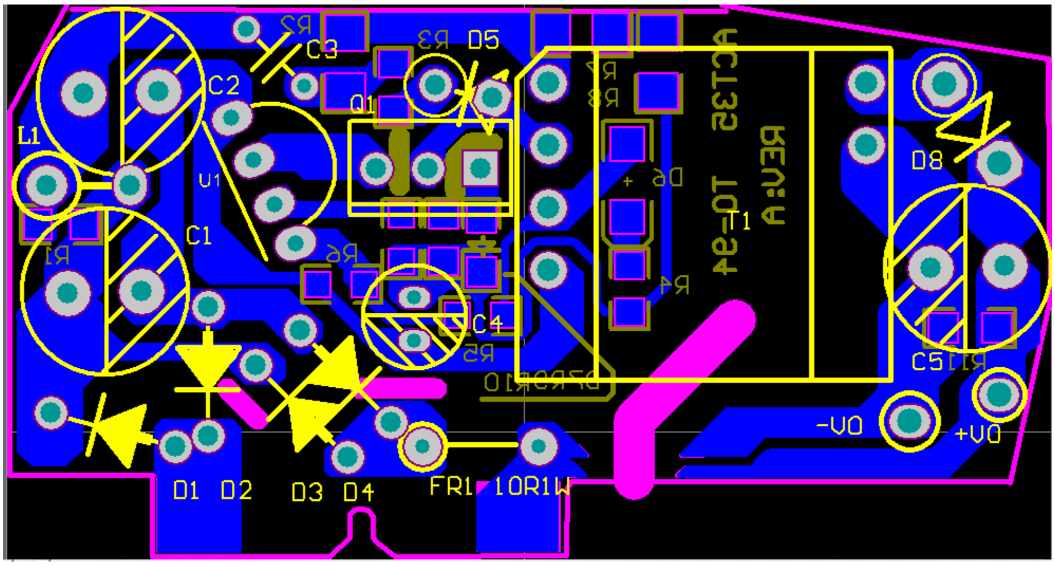


Figure 6 5V/700mA Charger PCB Layout

◆ TRANSFORMER SPECIFICATION

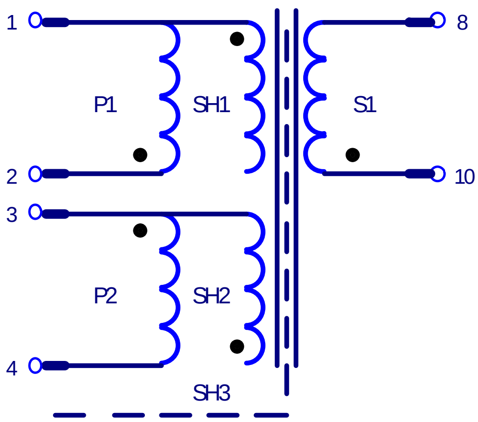


Figure 7 Transformer Schematics

Table 4 Build-up Table

Winding	Terminal		Turns	Wire			Insulation		Margin	
	Start	Finish		Type	Size*QTY	Layer	Thick/Wide	Layer	Pri side	Sec side
SH1	1	open	11	2UEW	0.15Φ*4	1	25u/8.5mm	2		
P1	2	1	130	2UEW	0.2Φ*1	4	25u/8.5mm	2		
SH2	4	open	11	2UEW	0.15Φ*4	1	25u/8.5mm	2		
S1	10	8	10	TEX-E	0.5Φ*1	1	25u/8.5mm	2		
P2	3	4	32	2UEW	0.18Φ*1	1	25u/8.5mm	2		
SH3	open	open	0.9	7mm Copper		1	25u/8.5mm	3		

Note: SH1 & SH2 are shielding, P1 & P2 are primary and S1 is secondary

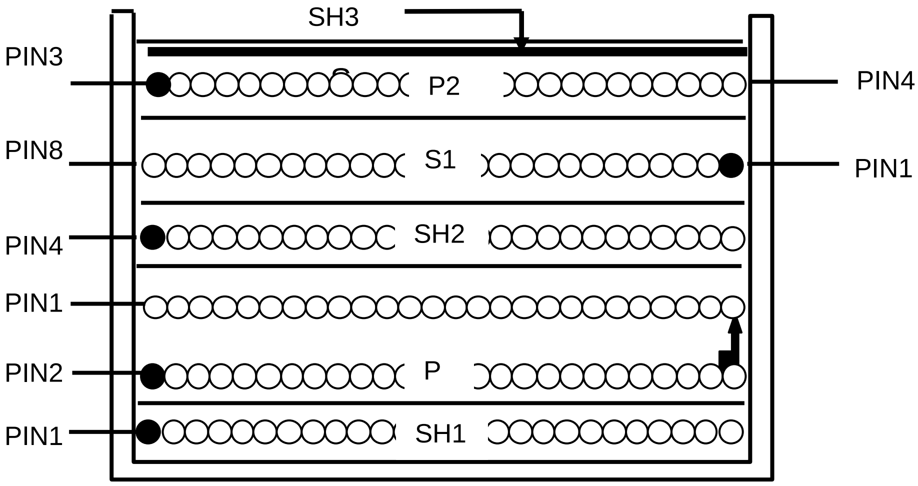


Figure 8 Transformer Build Diagram

◆ TYPICAL PERFORMANCE CURVES

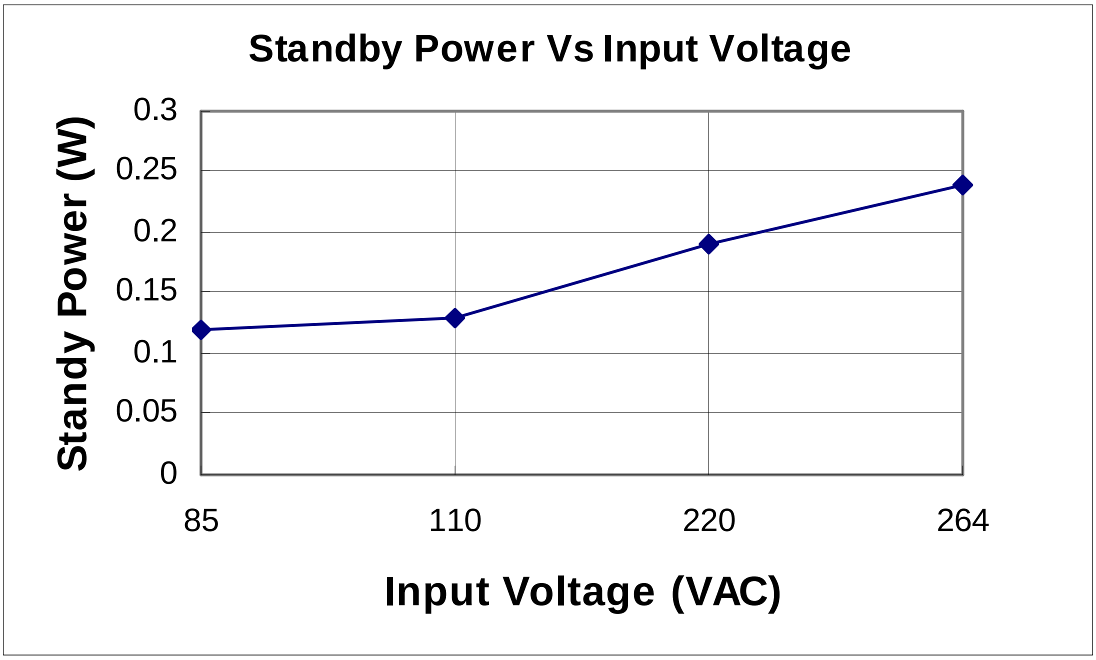


Figure 9 Standby Power Vs Input Voltage

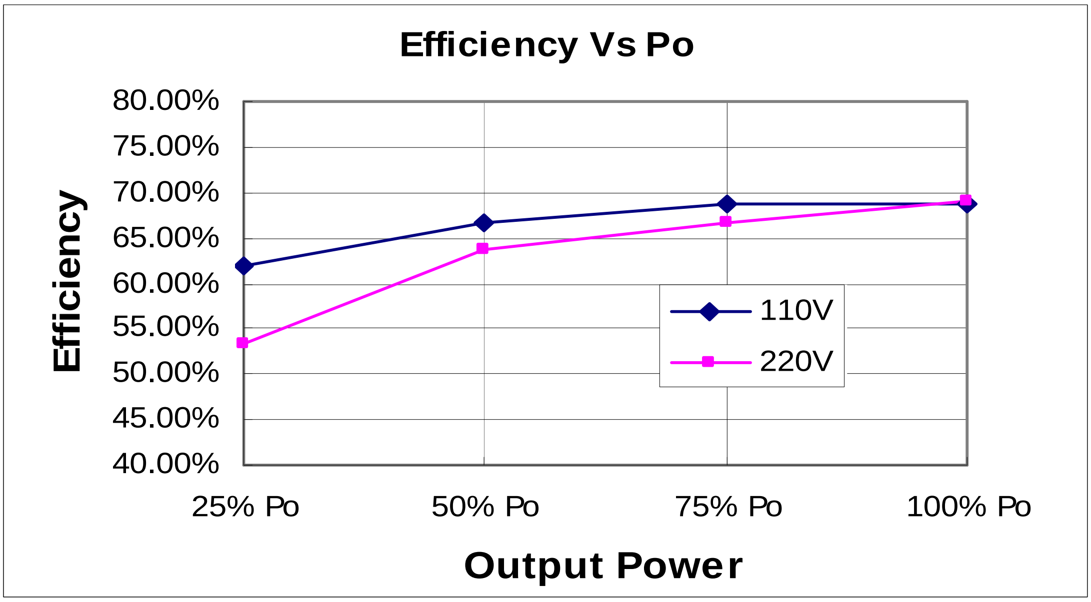


Figure 10 Efficiency Vs Ouput Power

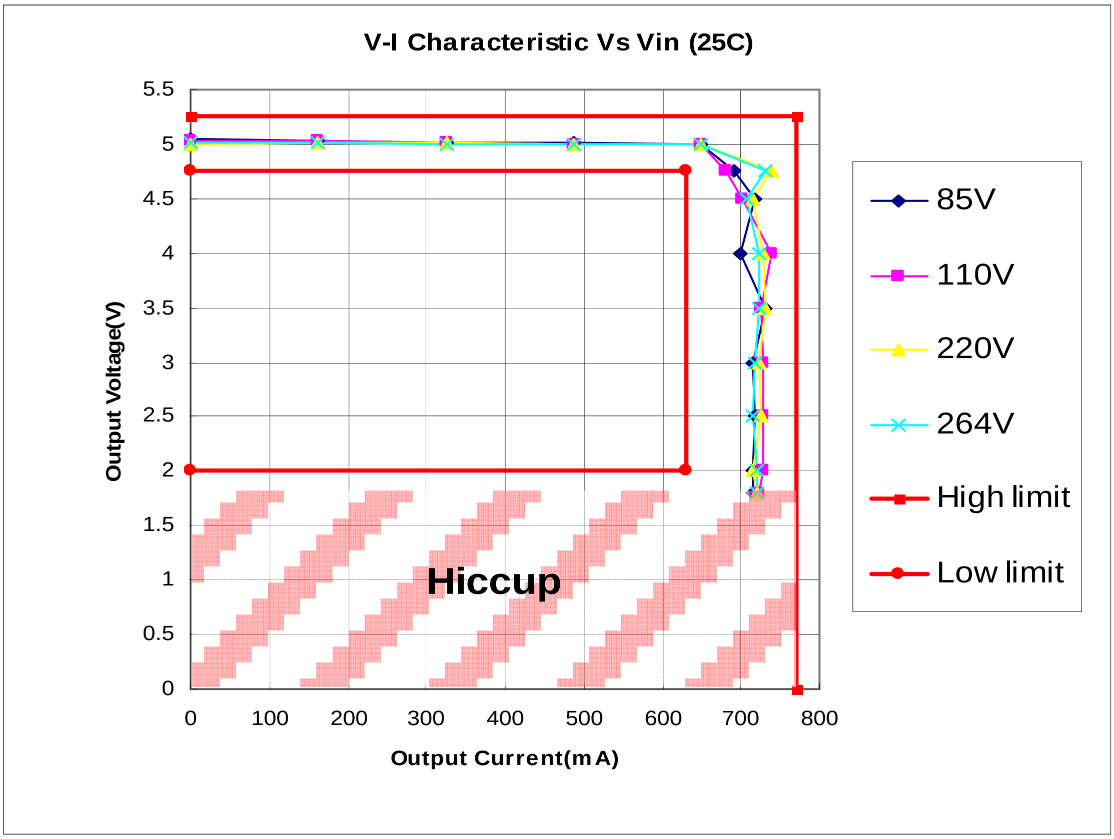


Figure 11 V-I Curves @ 25C

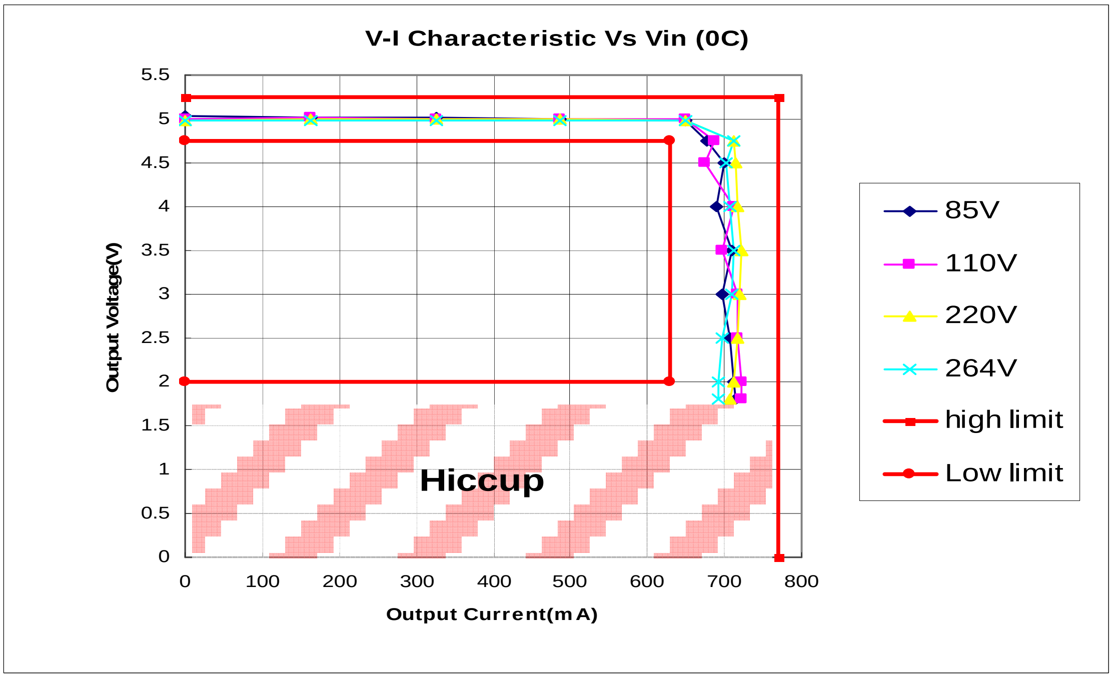


Figure 12 V-I Curves @ 0C

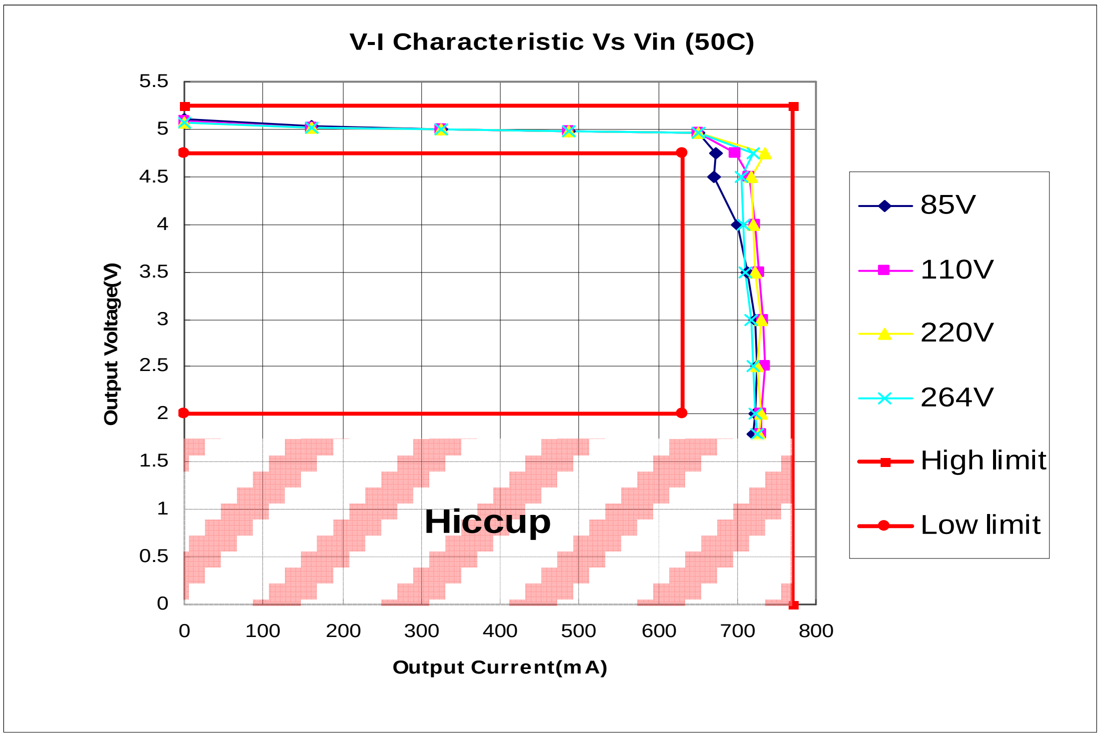


Figure 13 V-I Curves @ 50C

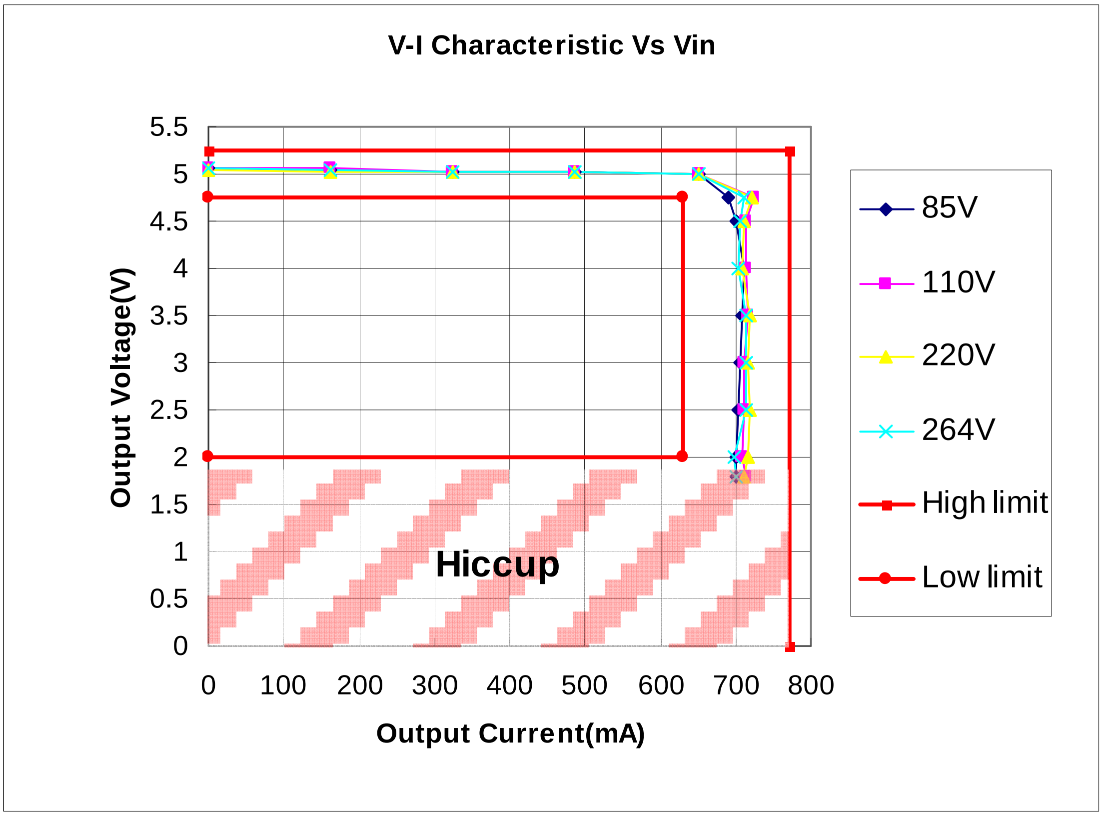


Figure 14 V-I Curves with Lm=1.58mH (Lm-10%)

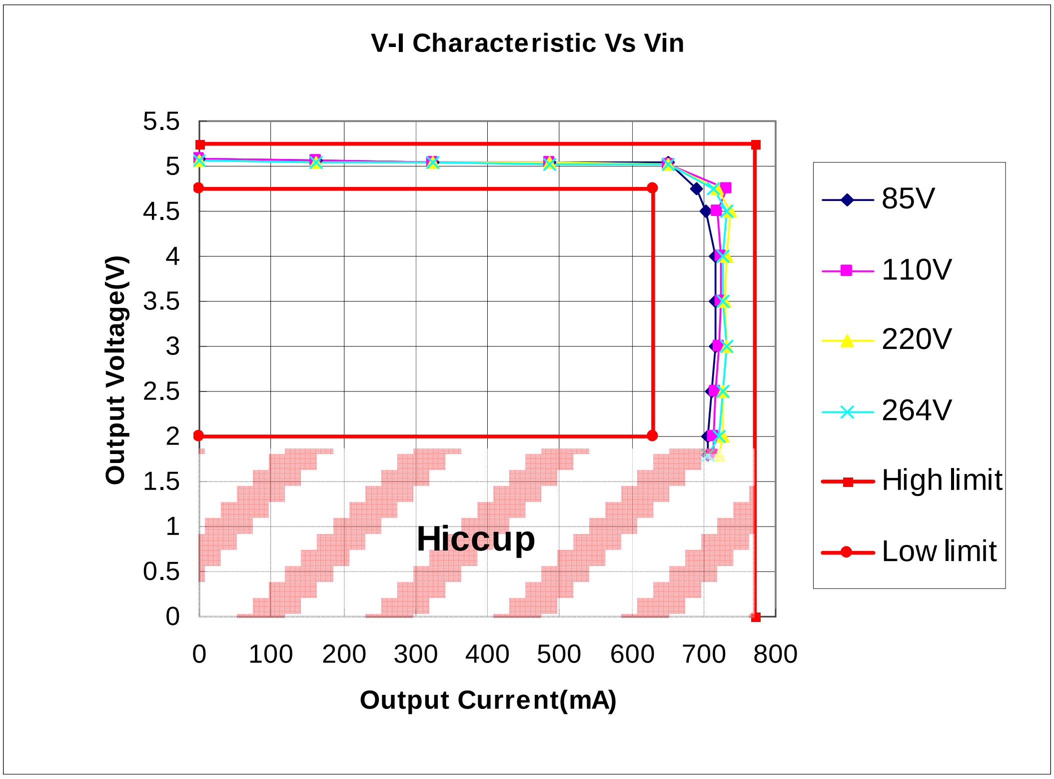
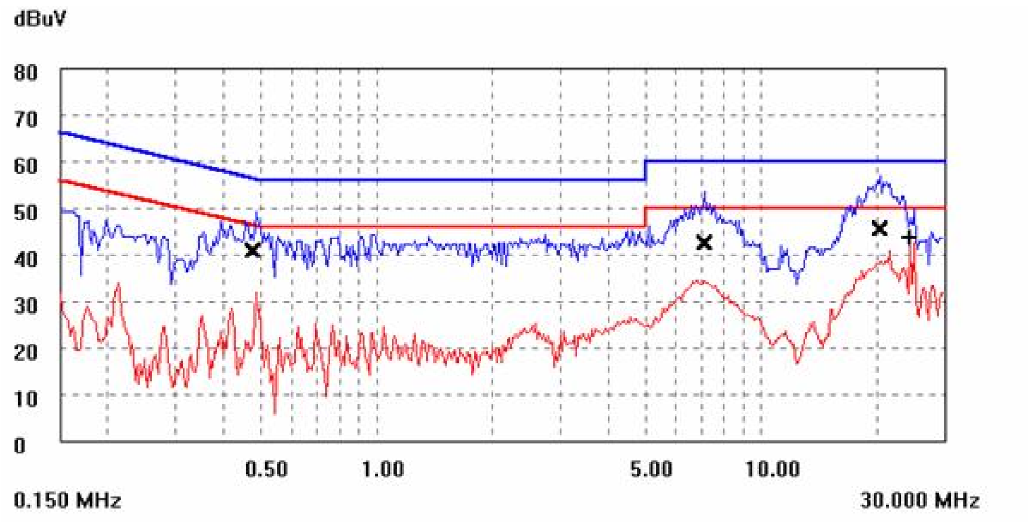


Figure 15 V-I Curves with Lm=1.82mH (Lm + 10%)



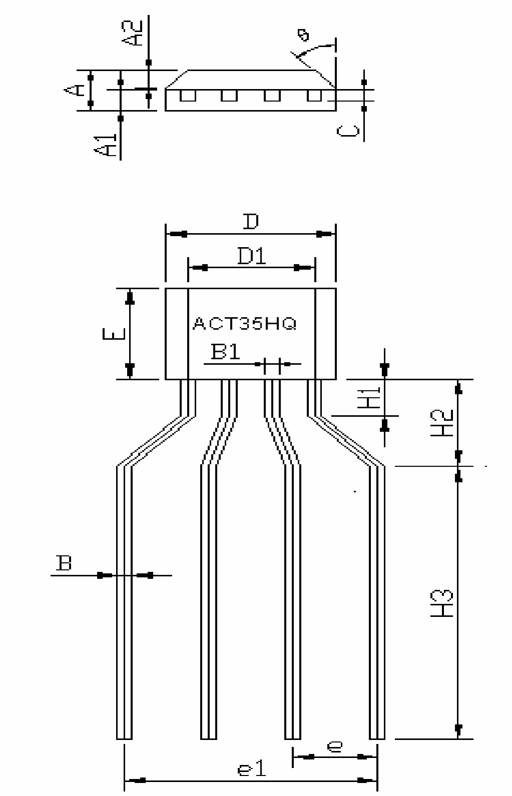
final test

	freq(MHz)	lev(dBuV)	Lim(dBuV)	△(lev-Lim)
(QP)	0.476	41.0	56.7	-15.7
	7.155	42.3	60.0	-17.7
	20.426	45.5	60.0	-14.5
(AV)	freq(MHz)	lev(dBuV)	Lim(dBuV)	△(lev-Lim)
	24.299	43.6	50.0	-6.4

Figure 16 Conducted EMI

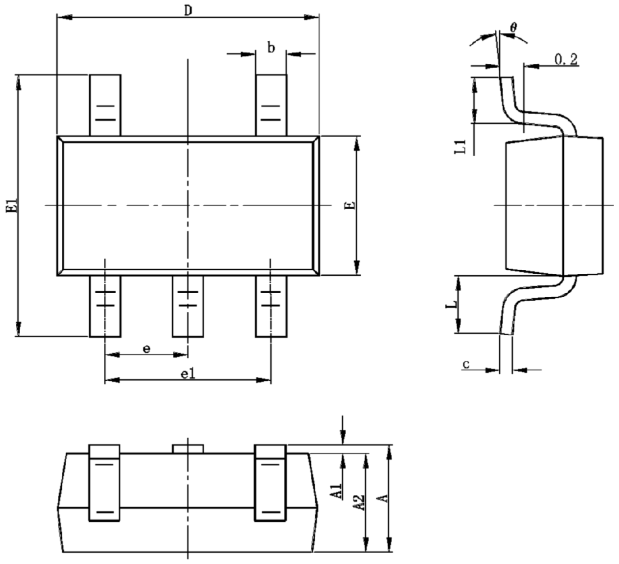
PACKAGE OUTLINE

TO-94 PACKAGE OUTLINE AND DIMENSIONS (AMMO TAPE PACKING)



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.400	1.800	0.055	0.071
A1	0.700	0.900	0.028	0.035
A2	0.500	0.700	0.020	0.028
b	0.360	0.500	0.014	0.020
b1	0.380	0.550	0.015	0.022
C	0.360	0.510	0.014	0.020
D	4.980	5.280	0.196	0.208
D1	3.780	4.080	0.149	0.161
E	3.450	3.750	0.136	0.148
e	2.200	2.800	0.086	0.110
e1	6.600	8.400	0.259	0.330
H1	1.350	1.650	0.053	0.065
H2	3.370	3.670	0.133	0.144
H3	10.830	11.130	0.426	0.438
θ	45^0TYP		45^0TYP	

SOT23-5 PACKAGE OUTLINE AND DIMENSIONS)



Symbol	Dimension in Millimeters		Dimension in Inches	
	Min	Max	Min	Max
A	1.050	1.250	0.041	0.049
A1	0.000	0.100	0.000	0.004
A2	1.050	1.150	0.041	0.045
b	0.300	0.400	0.012	0.016
c	0.100	0.200	0.004	0.008
D	2.820	3.020	0.111	0.119
E	1.500	1.700	0.059	0.067
E1	2.650	2.950	0.104	0.116
e	0.950 TYP		0.037 TYP	
e1	1.800	2.000	0.071	0.079
L	0.700 REF		0.028 REF	
L1	0.300	0.600	0.012	0.024
θ	0°	8°	0°	8°