Introduction to GreenChip III (TEA1750 & TEA1751)

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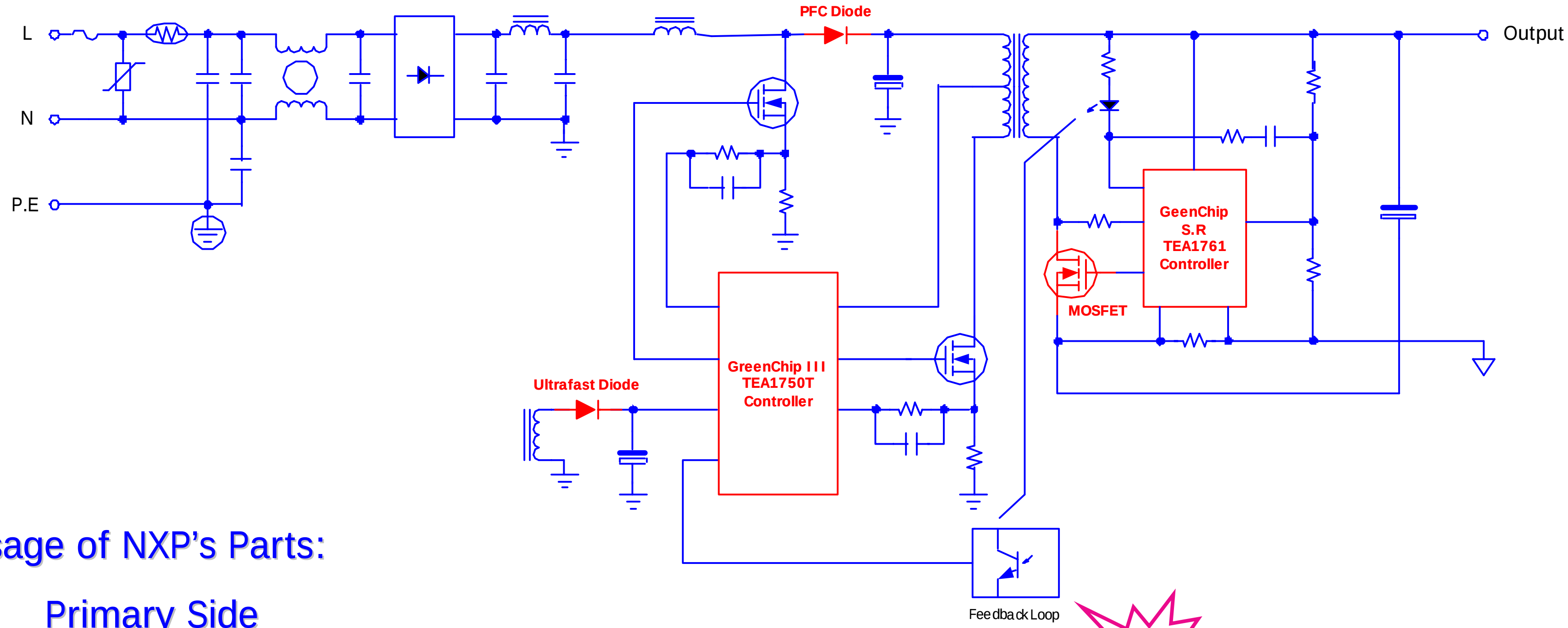
Agenda

- System Block Outline
- GreenChip III SMPS Control IC TEA1750 & TEA1751 General Features
- GreenChip III SMPS Control IC TEA1750 & TEA1751 Application Details
- Comparison of TEA1751 vs. TEA1750
- PCB Layout Considerations

System Block Outline

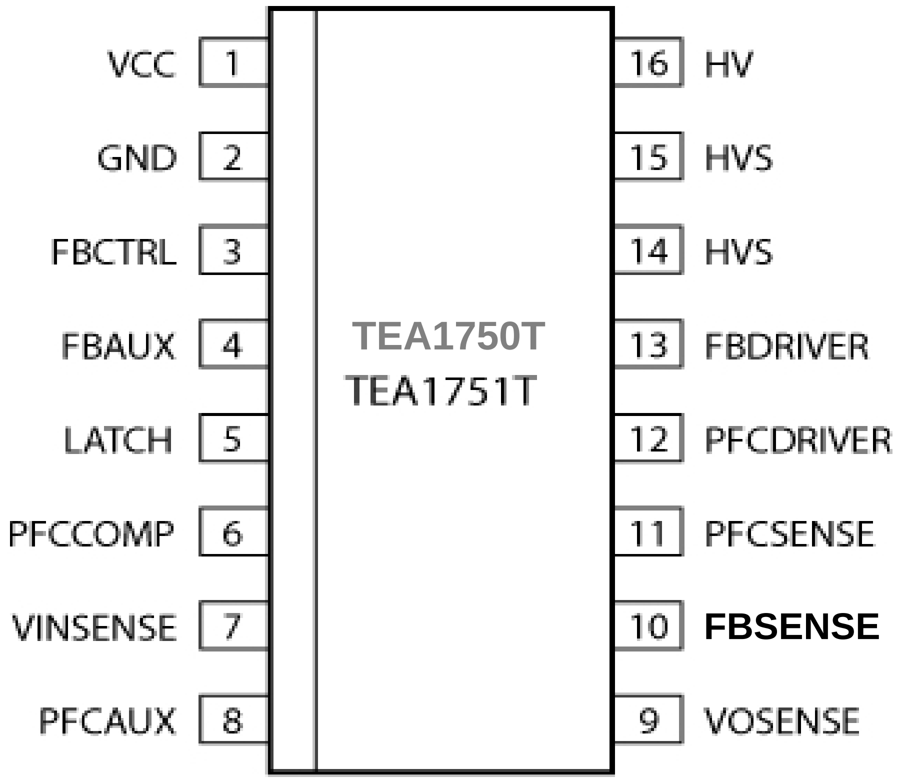


Usage of NXP's Parts:

- Primary Side
  - GreenChip III PFC/Flyback Combo IC, TEA1750 & TEA1751 *New!*
  - PFC Diode, BYC5-600 or BYV29-600 or BYV29X-600....
  - Ultra-Fast Diode, BAV103
- Secondary Side
  - GreenChip Synchronous Rectifier Controller, TEA1761, TEA1762 & TEA1791 *New!*
  - MOSFETs, PHP45NQ10T or PSMN015-100P or PSMN015-110P....

GreenChip III SMPS Control IC
TEA1750 & TEA1751
General Features

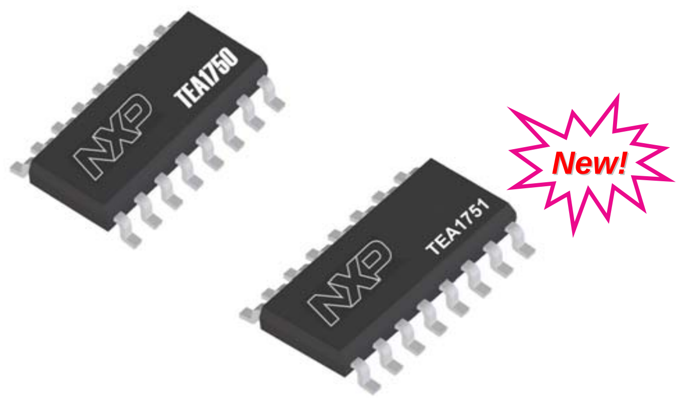
GreenChip III TEA1750/1, Pin assignment



Multi Chip Module in SO16

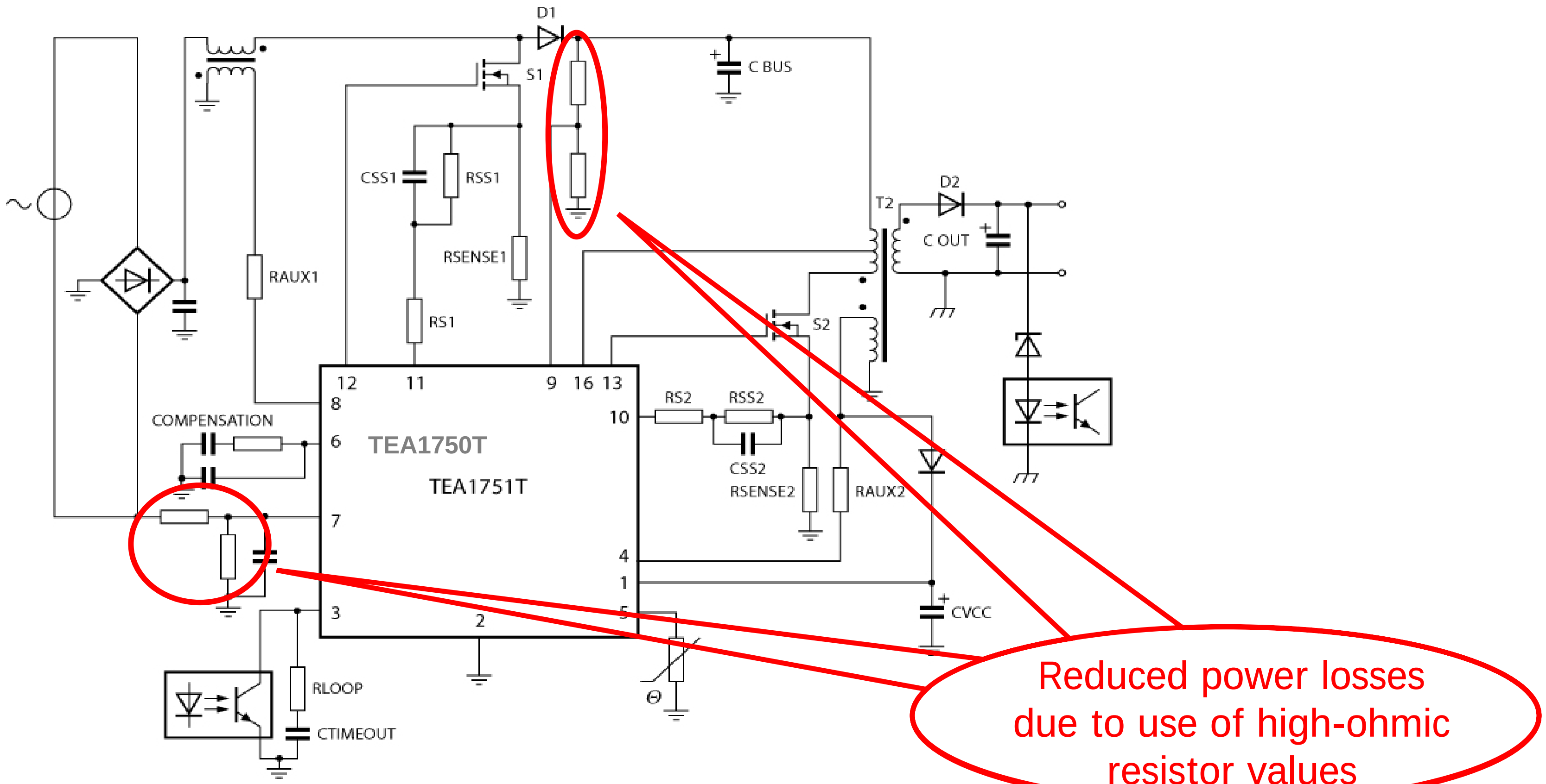
BCD800: High voltage startup and valley detect

ABCD2: Control part



GreenChip III TEA1750/51, **Basic application diagram**

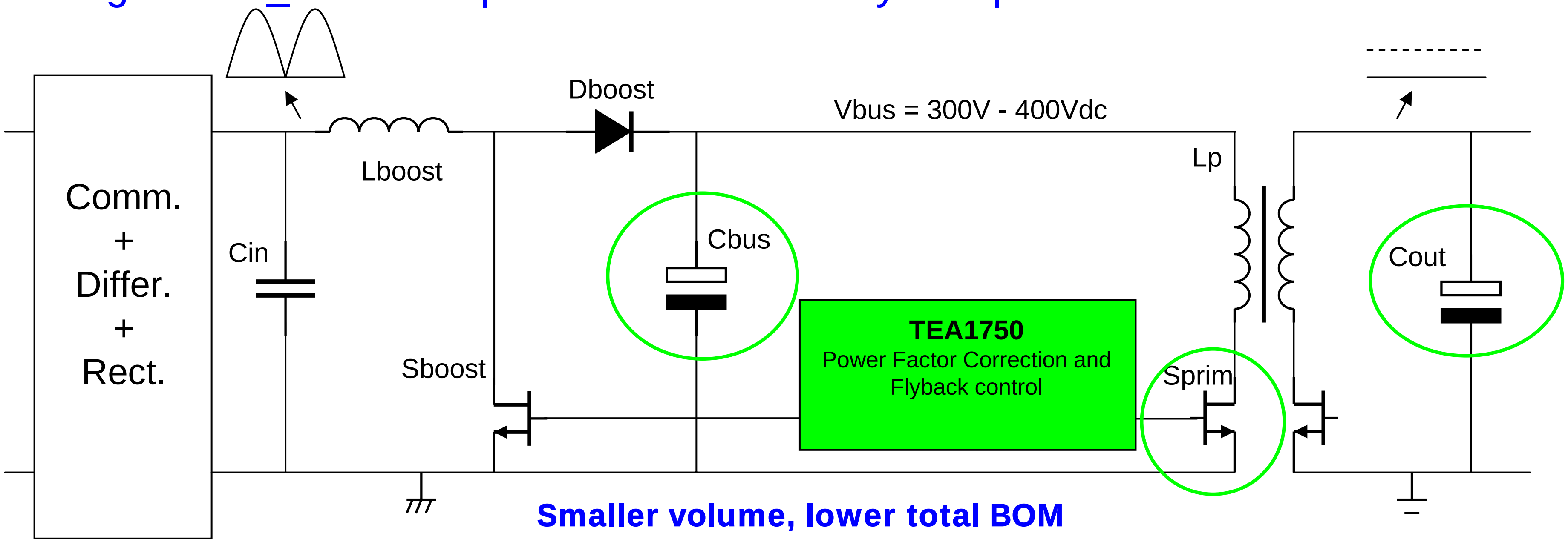
An almost 100mW standby power reduction in comparison to applications using conventional PFC solutions. The new GreenChip III technology allows a higher ohmic resistant ladder in the feedback loop)



GreenChip III TEA1750, Cost saving aspects

Due to dedicated functionality of the fixed boost PFC, including PFC that switches to low power mode during standby mode ☞ Flyback only has to operate from 300V.... 400Vdc

- ✓ Smaller mains electrolytic capacitor (Cbus) and smaller output electrolytic capacitor possible due to lower RMS currents in boost
- ✓ Possible cost reduction for the flback TR due to the fact that the flyback converter only has to operate from ~300V up to 400Vdc instead of ~120V up to 400Vdc
- ✓ Higher Rds_on for the power Mosfet in the flyback part

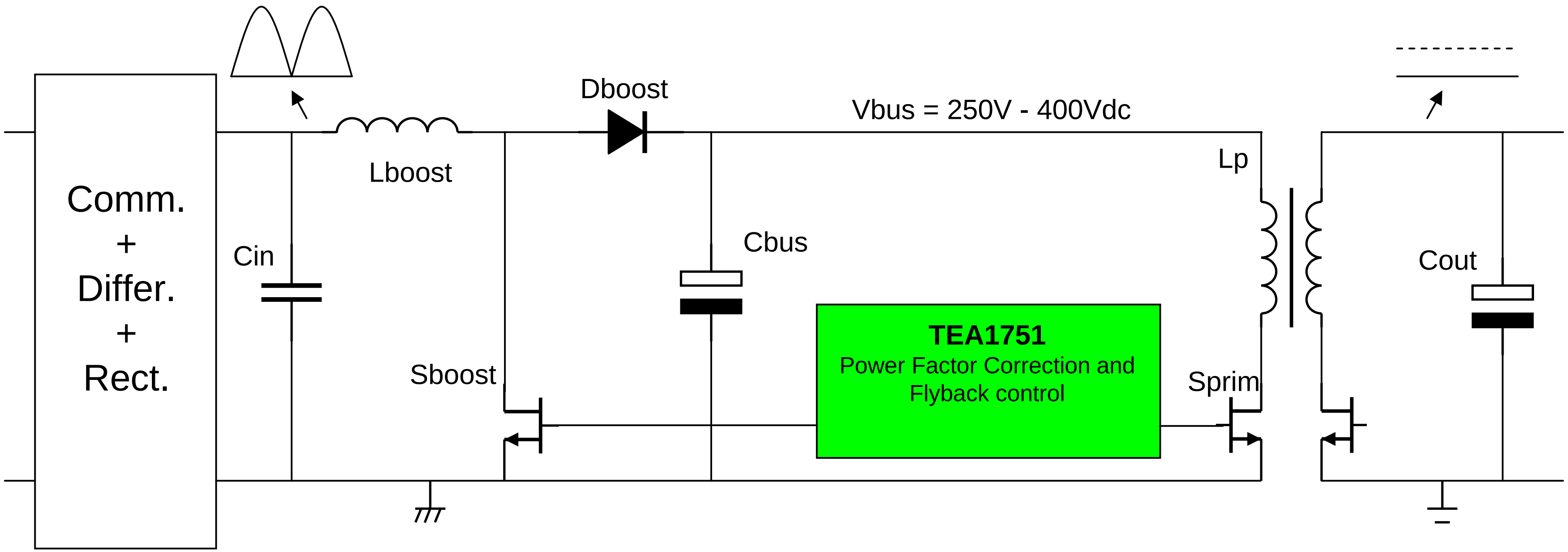


Smaller volume, lower total BOM

GreenChip III TEA1751, Choosing configuration

GreenChip III TEA1751, adapter solution

- Dual boost
- PFC switches automatically off during stand-by / low load



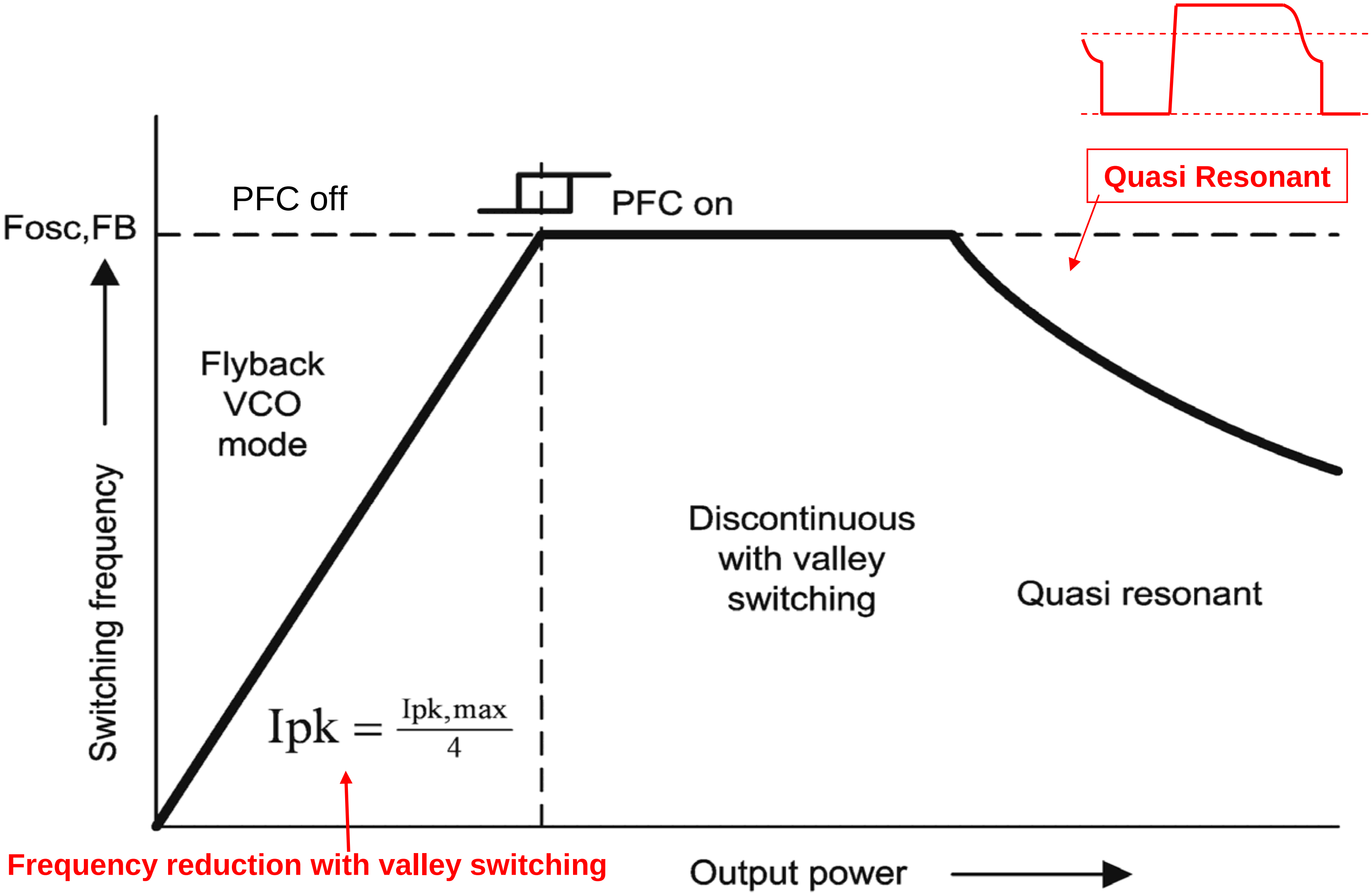
GreenChip III TEA1750/1, Design advantages

- Integrated PFC and flyback controller (reduced PCB space)
- Reduced design-in time
  - No interface issues between the two controllers
  - No additional hardware needed to communicate between the two controllers
  - Easy controlled start-up behavior
  - Easy Vcc management, only one Vcc Electrolytic Capacitor
- High protection level
- Significant reduction of SMD components
  - Reduction of throughput time at SMD placing machines

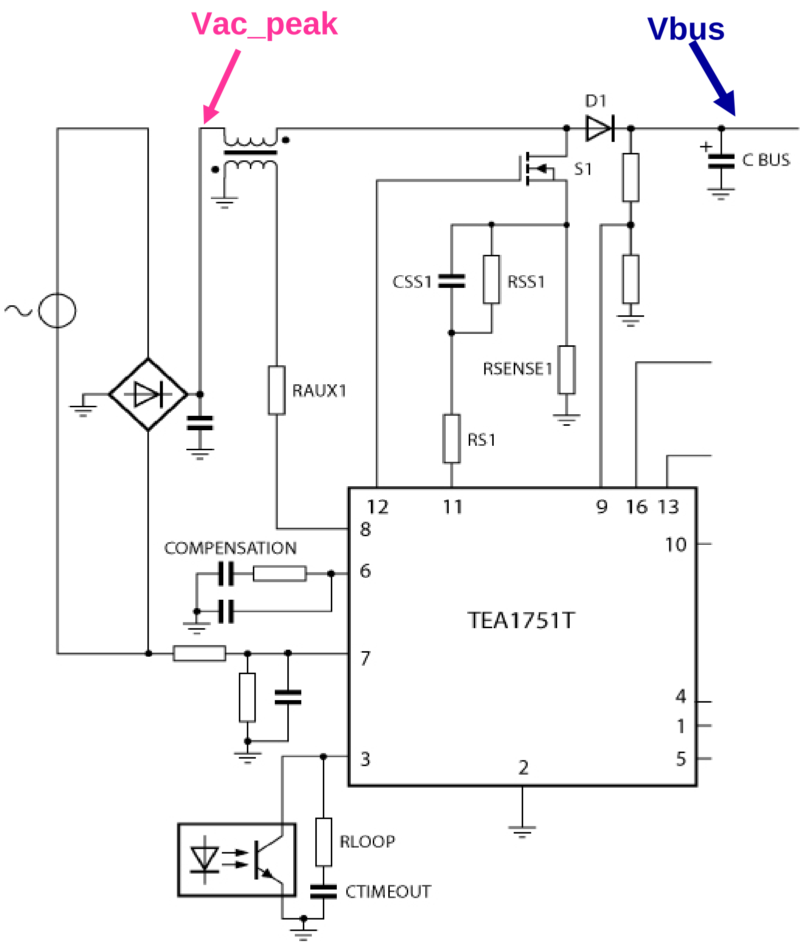
GreenChip III TEA1750/1, System implementation

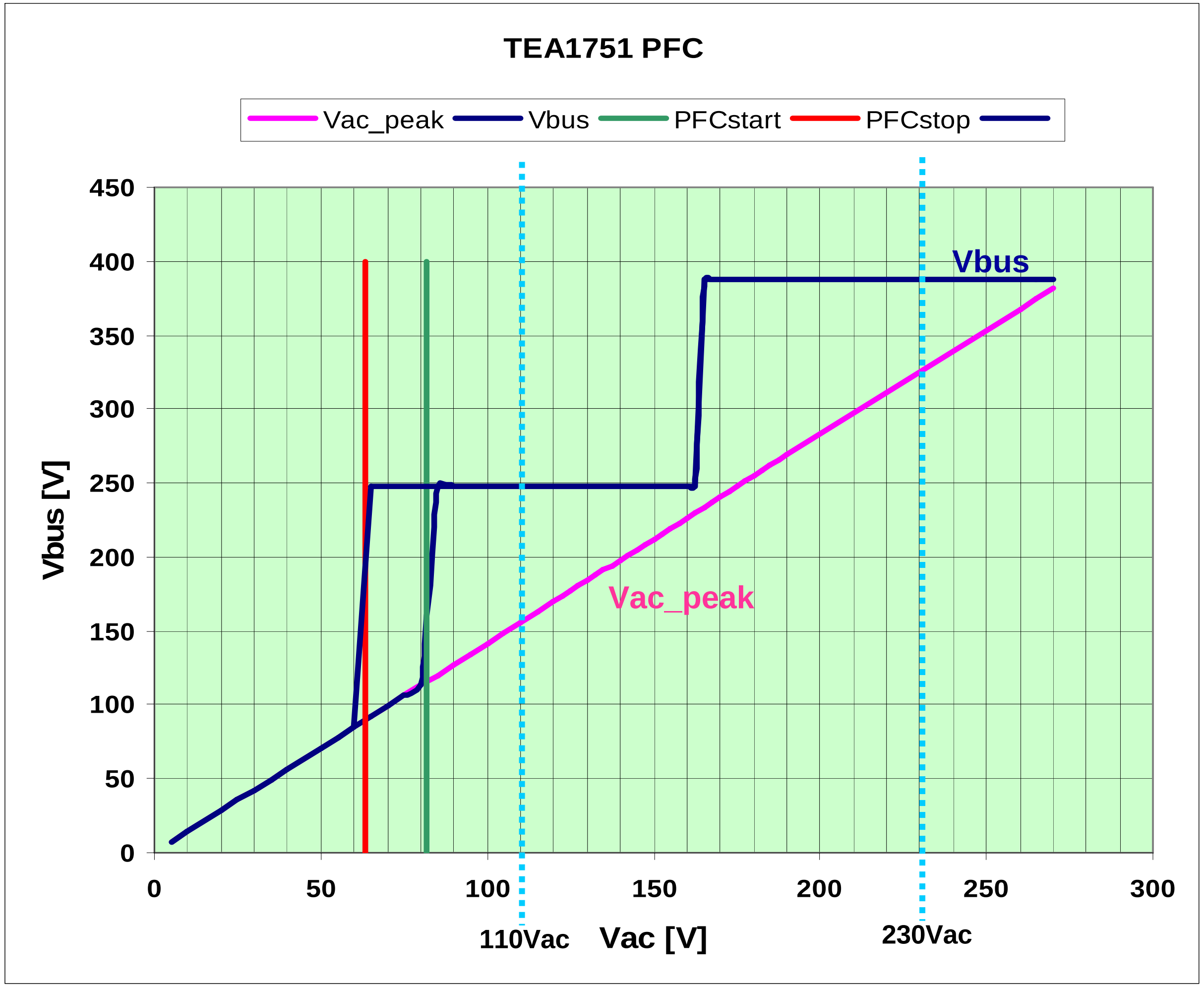
- PFC
  - Switches automatically off during stand-by / low load
  - Fixed/Dual boost (TEA1750/TEA1751)
- Flyback
  - Always active, start-up is defined by PFC start-up
  - QR mode
  - Ip_min = ¼ Ip_max to meet Energystar no-load requirements
- HV-current-source
  - Source current 5.2mA (typ)
  - Reduced source current during restart (safety)
  - Current-source is active till flyback starts
  - Vcc is regulated to Vcc_start as long as the current-source is active

GreenChip III TEA1750/1, Flyback converter operating modes



GreenChip III TEA1751, Operation of the PFC, dual boost





GreenChip III TEA1750/1, Protections

- PFC
  - M-level and brown-out through pin Vi-sense
  - Open pin detection @ pin Vi-sense and PFCaux
  - Short and open pin detection @ pin Vo-sense, therefore external OVP circuit is not required
  - OCP
  - (soft) OVP through pin Vo-sense

- Flyback
  - Open pin detection @ pin FBctrl and Fbaux
  - OCP
  - OVP through FB aux winding (accurate)
  - Time-out through pin FBctrl (auto restart)
  - Accurate Over Power Protection (OPP)

GreenChip III TEA1750/1, Protections (continued)

- System
  - Latch-pin with internal current-source
  - Fast latch reset through pin Vi-sense
  - Internal OTP at 150degC (typical value)
  - Reduction of HV charge current after detection of protection to reduce input power in auto-restart mode

GreenChip III SMPS Control IC
TEA1750 & TEA1751
Applications Details

PFC & Flyback Start-up Conditions

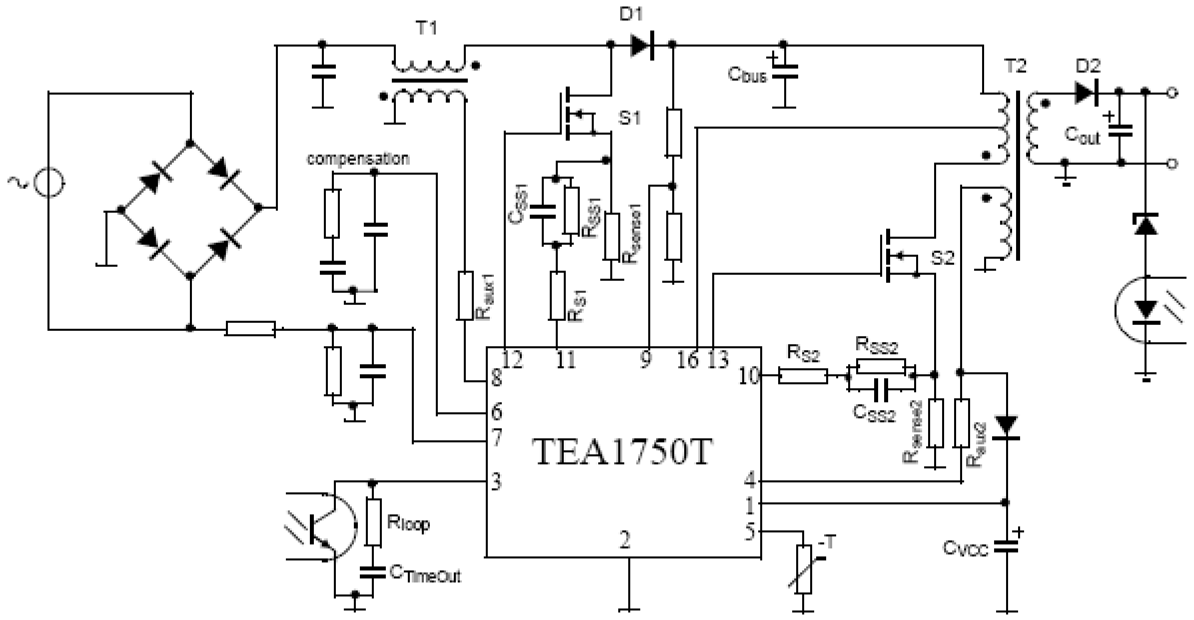


Fig 15. Typical application diagram.

Pin	Name
5	Latch
11	PFCsense
7	VinSense
9	VoSense

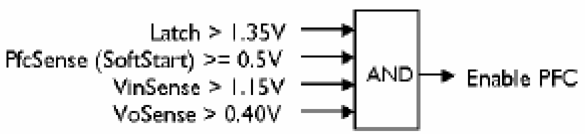


Fig 1. PFC start conditions

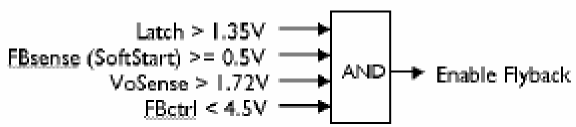
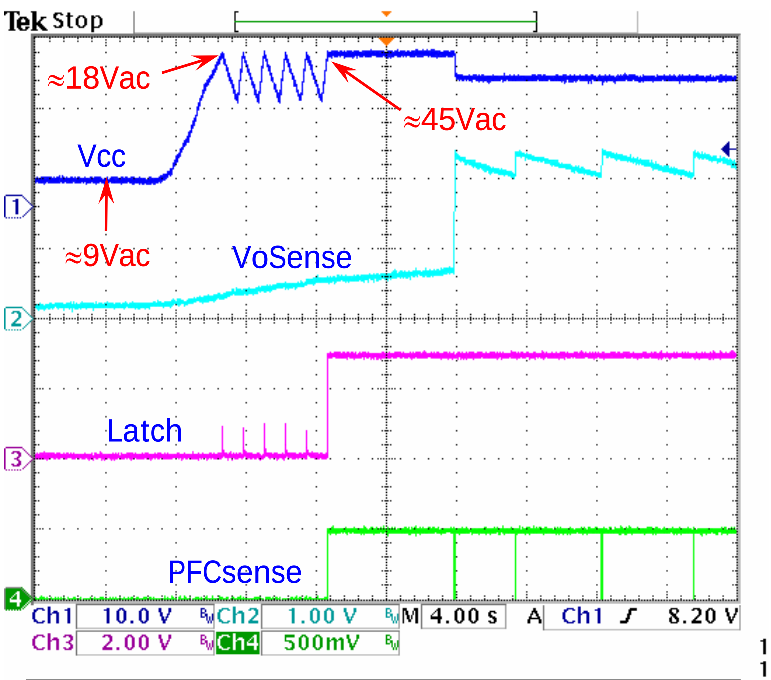


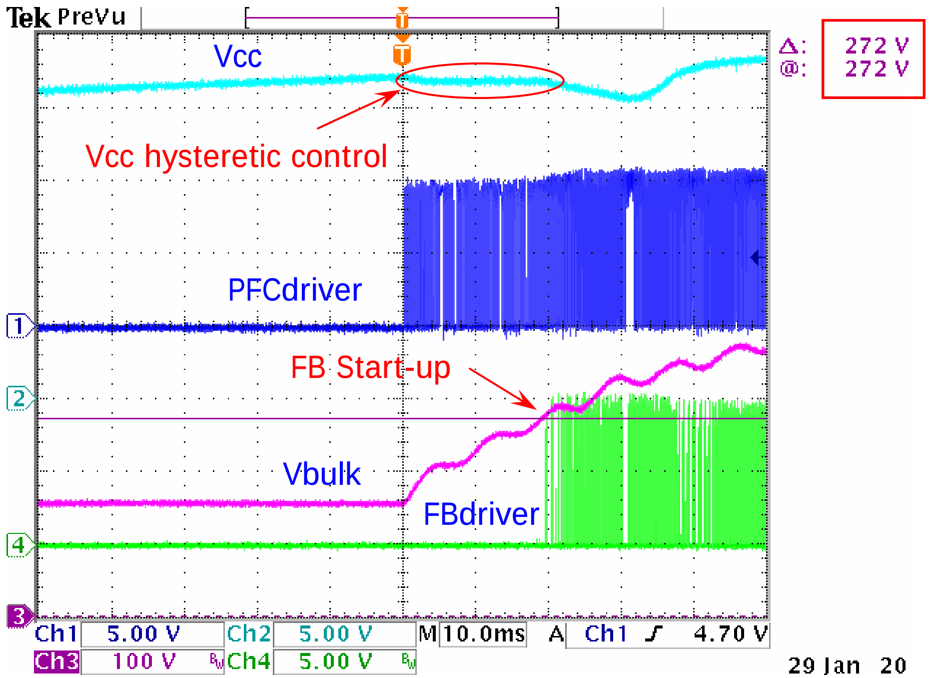
Fig 2. Flyback start-conditions

Pin	Name
5	Latch
10	FBsense
9	VoSense
3	FBctrl

PFC & Flyback Start-up – 1 (TEA1750)

UUT: APBADC015 (TEA1750+TEA1761)



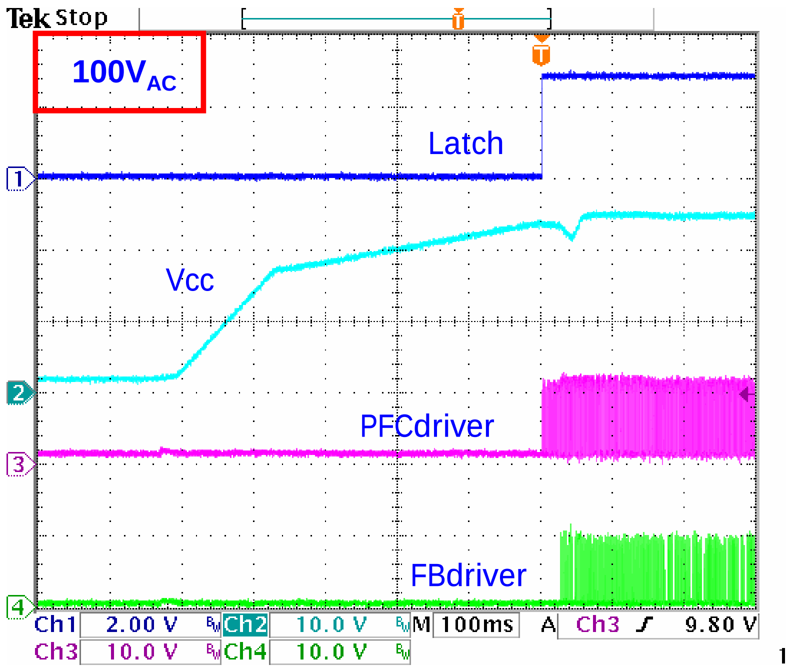


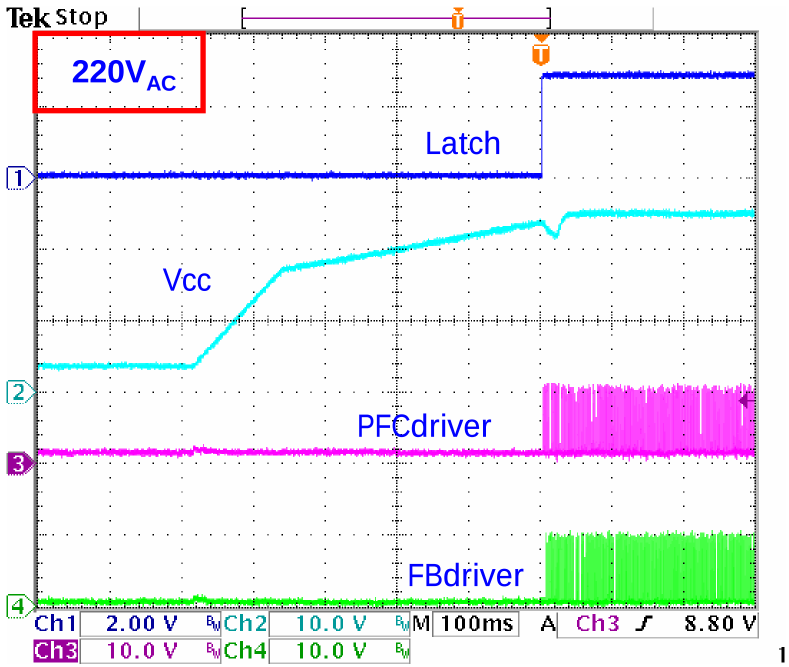
Latch > 1.35V
PFCsense ≥ 0.5V
VoSense > 0.4V
VinSense > 1.15V
- PFC Start Conditions -

Latch > 1.35V
FBsense ≥ 0.5V
FBctrl < 4.5V
VoSense > 1.72V
- FB Start Conditions -

PFC & Flyback Start-up – 2 (TEA1750)

- Start-up at low mains:
  - – PFC starts first
  - – If HV-bus > 250Vdc, then the flyback starts
- Start-up at high mains:
  - – PFC and flyback are starting at the same time

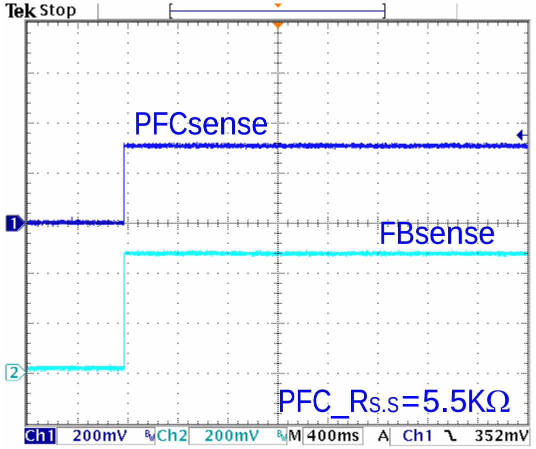




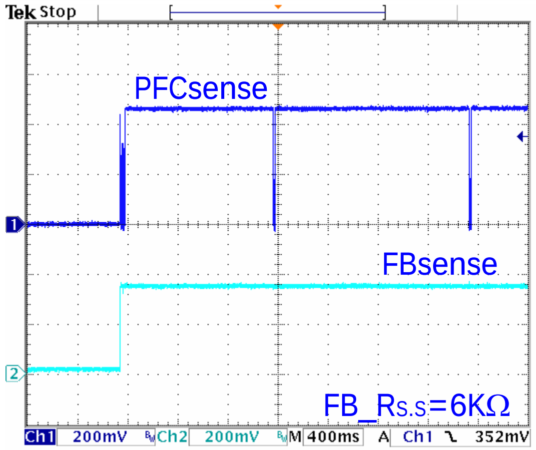
Minimum Soft-start Resistor(s)

Both soft start capacitors at pin PFCsense and pin FBsense have to charged up to 0.54V (max. soft start and enabling voltage) with the internal 45μA (min. soft start current) current-source, else both controllers will not start-up.

Soft start, soft stop PFC (pin PFCSENSE)					
$I_{start(soft)(PFC)}$	soft start current for PFC	−75	−60	−45	μA
$V_{start(soft)(PFC)}$	soft start and enabling voltage for PFC	0.46	0.50	0.54	V
$V_{stop(soft)(PFC)}$	soft stop voltage for PFC	0.42	0.45	0.48	V
$R_{start(soft)(PFC)}$	minimum required external soft start resistor for PFC	12			kΩ



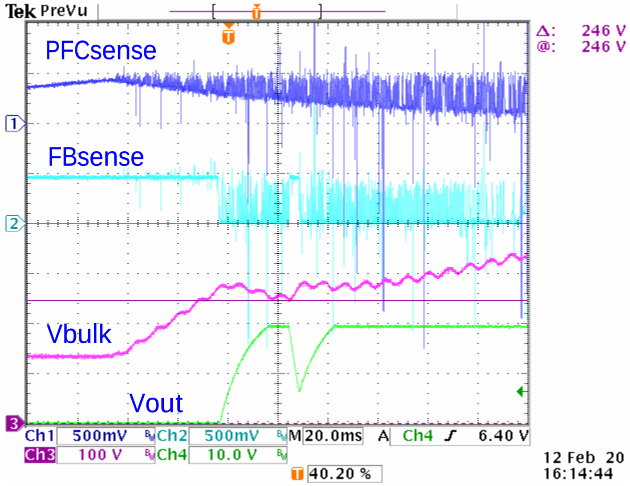
Rstart(soft)_min. = Vstart(soft)_max. / Istart(soft)_min.



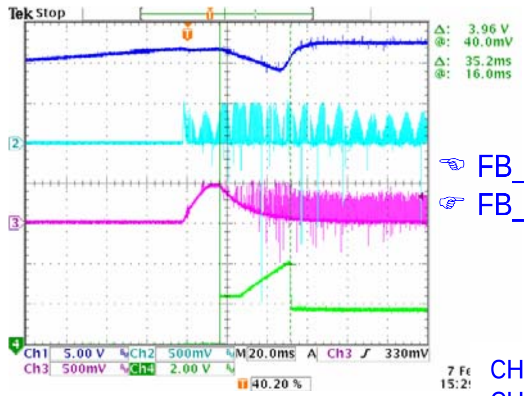
Soft start flyback (pin FBSENSE)					
$I_{start(soft)(FB)}$	soft start current for flyback	−75	−60	−45	μA
$U_{start(soft)(FB)}$	soft start and enabling voltage for flyback	0.46	0.5	0.54	V
$R_{start(soft)(FB)}$	minimum required external soft start resistor for flyback	12			kΩ

Soft-start Capacitor(s)

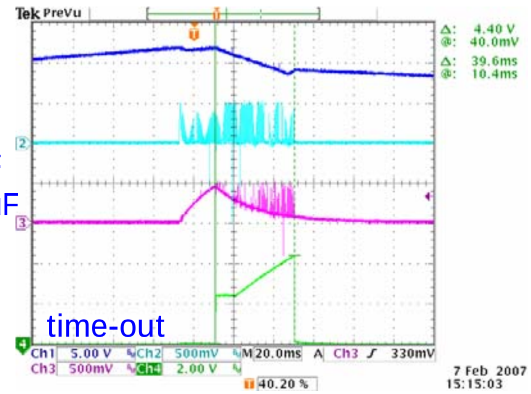
The charge time of the soft start capacitors can be adjusted such that the PFC starts before the flyback.



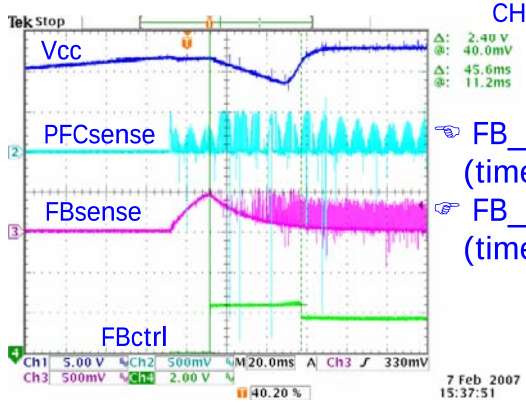
PFC_Cs.s (10µF) >> FB_Cs.s (22nF)



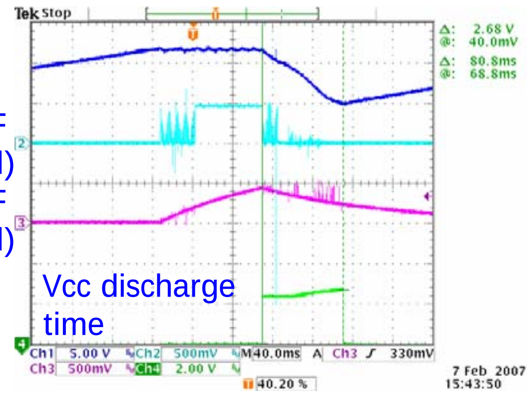
- FB_Cs.s = 1.1uF
- FB_Cs.s = 1.57uF



CH1: Vcc
CH2: PFCsense
CH3: FBsense
CH4: FBctrl

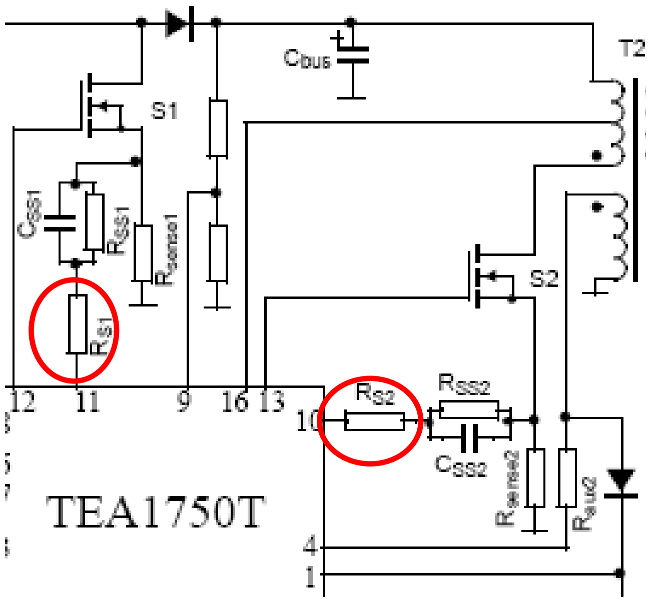


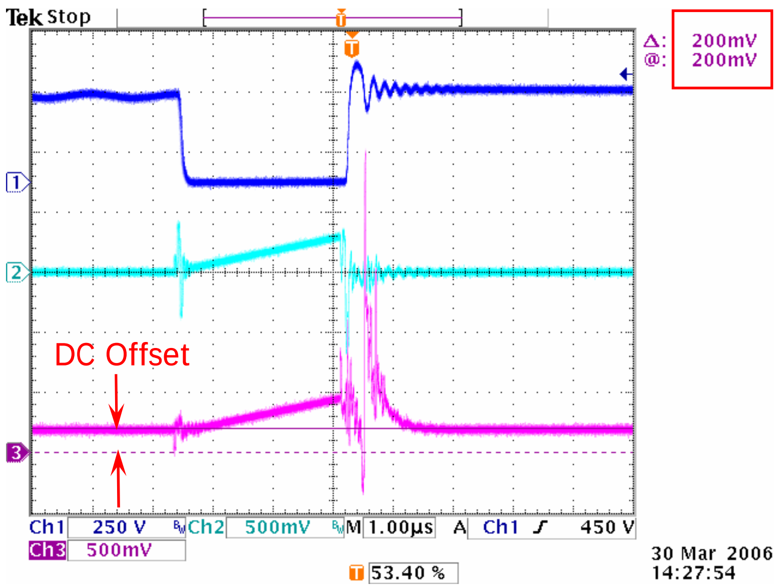
- FB_Cs.s = 1.57uF (time-out disabled)
- FB_Cs.s = 10.1uF (time-out disabled)



Start-up Problem – DC Offset at Sense pin (1/2)

Resistors R_{S1} and R_{S2} are added to prevent that the soft-start capacitors are charged during normal operation due to negative voltage spikes across the sense resistor. (shown on page 24 of TEA1750 datasheet)



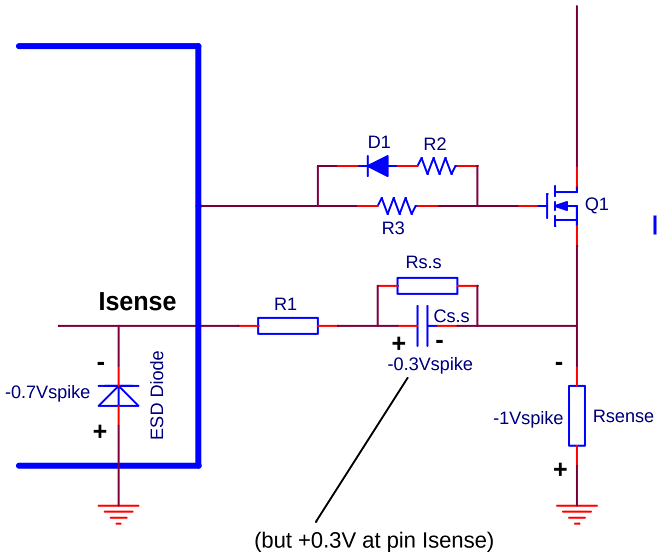


A DC offset at the sense pin therefore result in a reduction of the maximum peak current or even could not start-up smoothly.

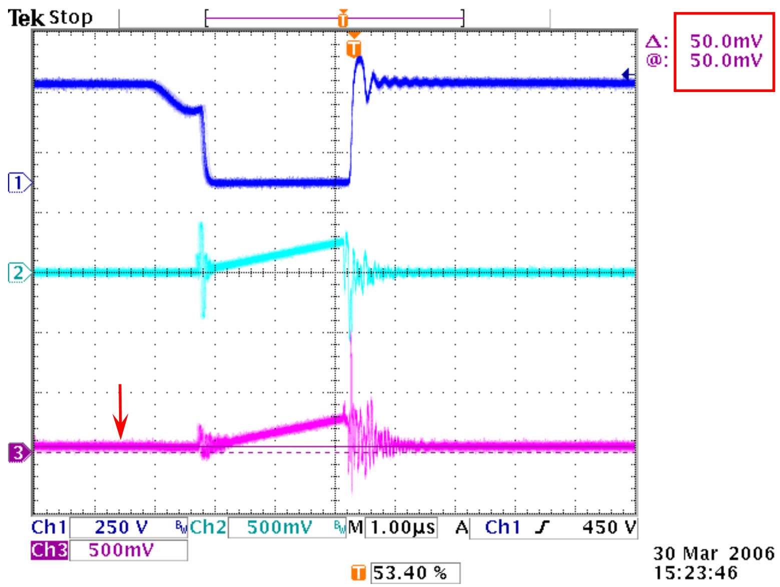
Start-up Problem – DC Offset at Sense pin (2/2)

The cause of that phenomenon is the parasitic voltage ringing across the sense resistor. The negative part of that voltage can charge the soft start capacitor, which is in series with the sense input pin of the IC. Internally the IC there is a diode path from ground to sense so if the sensed voltage is –0.7V the ESD diode conduct.

☞ Increasing the R1 resistor valve to limit the spike current depicated as below:



Increasing R1 value to 1K ~ 2.2K



Separate usage of the PFC or Flyback

Why we need to do this?

1. It’s hard to power up after made a careful check of the power supply.
2. With some uncertain reasons cause of an oscillation/disturbance behavior or generate an audible noise. PFC? FB?

Stop PFC: (if one of below condition happens, the FB can operate at high mains alone)

1. To short-circuit the gate pin of PFC MOSFET to ground directly, or
2. To short-circuit the VinSense pin to ground, or
3. With a larger resistor at VoSense pin (f.i from 62k to 100k) to trigger the PFC_OVP event at low mains.
4. ....

Stop Flyback:

1. Placing an 100KΩ resistor between the FBctrl and FBaux pin.
2. AC power up then apply an external power supply (>15V) via a diode to the Vcc pin then PFC will start switching.
3. ....

I_p Current in Burst Mode (TEA1750)

When the output power is low, the flyback converter switches over to VCO mode. When VCO mode is entered, the PFC circuit switches to burst mode control.

The PFC goes from normal operation into burst mode, the on-time is increased (as a result the peak current is increased). The reason for this is that the PFC has to deliver the same <u>average</u> output power, but is switched off now for a certain time. All the power has to be delivered in the up-going slope of burst mode, during the down going slope the PFC does not convert power.

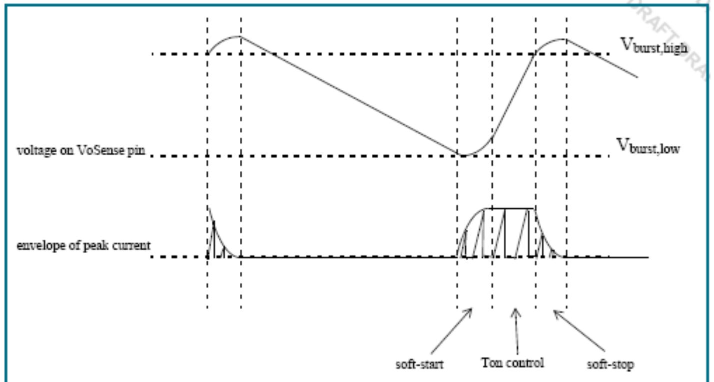


Fig 6. Burst mode control

No-Load Mode CEC Measurement in Burst Mode

- The TEA1750 will be operating in burst mode, where the converter draws power in 125KHz burst packets that are spaced 3~5 seconds apart. These intermittent bursts of current and power drawn from the line will result in inconsistent measurements from the power meter.
- Long integration mode, set to 60 seconds, is used to display continuous measurements taken at a high sample rate and averaged over an extended time period. In this way, several hunders of burst packet cycles are measured for an accurate representation of input no-load power.
- The input power of APBADC015 demoboard at no-load mode were measured as below: (Power Meter: Hioki, Model 3332)
  - 0.005Wh/60s=0.3W @115VAC
  - 0.010Wh/120s=0.3W @115VAC

Note:
An energy expenditure of 1 Wh represents 3600 joules.
To obtain joules when watt-hours are known, multiply by 3600.

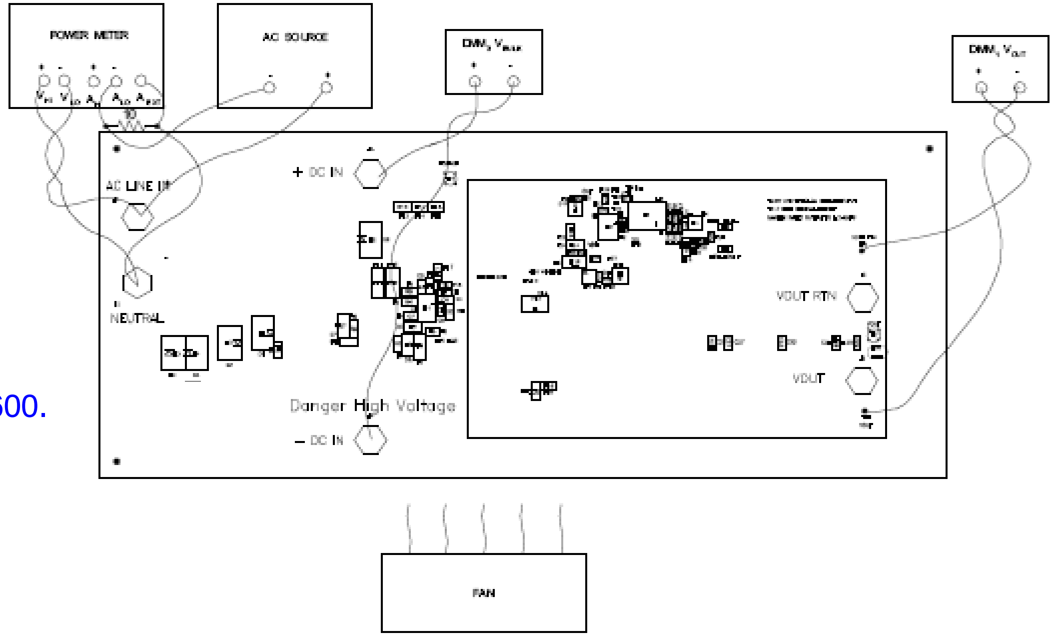


Figure 7. Equipment Set Up for Accurate No-Load Power Measurements

25% η_{CEC} Solution in Burst Mode

Application Problem:

The fixed boost voltage may cause a lower efficiency at 25% load result in failure to CEC minimum average efficiency in active mode requirements.

Possible Solution: (to lower the boosted voltage)

It is possible to increase the output-power level where the PFC is switched to burst mode by decreasing the flyback current-sense resistor.

PFC on/burst mode is controlled by the flyback. The PFC is switched to burst mode when Ip_flyback=0.25xIp_max. This is equal to point were the flyback VCO or frequency-reduction mode starts. At 0.25xIp_max, FBsense=0.13V.

Some drawbacks of increasing this switch-off level are:

- Higher OCP level.
- For customer manufacture, it's very difficult to measure the input-power level when unit run into the burst mode.

Note: With Yokogawa's WT210 series power meter, the measurement can become more faster in advance.

VinSense Calculation

The calculation of the brownout VinSense voltage at full load that the calcul-ation has a reasonable accuracy as long as the PFC is on (not in burst-mode).

If the full load brownout is calculated at 75Vac, then the AC turn on will be approximately 82Vac to 85Vac.

Calculation of the AC switch-on voltage is much more complicated because the voltage at the connection point of R1 and R2 does not go to 0V at the 0 deg phase of the AC voltage. This is also the reason why the brownout voltage is lower at very low loads.

$$Vav = \frac{1}{2\pi} \bullet \left\{ \int_0^{\pi} (Vm \bullet \sin wt) d(wt) + \int_{\pi}^{2\pi} (Vm \bullet \sin wt) d(wt) \right\} = \frac{2Vm}{\pi} = 0.636Vm$$

Refer to next page:

U1=the average voltage across R1 and R2 which is equal to $\frac{2\sqrt{2} \bullet Vac}{\pi}$

$$U2 = U1 \bullet \frac{\frac{R2 \bullet (R3 + R4)}{R2 + (R3 + R4)}}{R1 + \frac{R2 \bullet (R3 + R4)}{R2 + (R3 + R4)}}$$

☞ $$VinSense = U2 \bullet \frac{R4}{R3 + R4}$$

Note: The equivalent resistor value of R1-R4 can also be used for the calculation of the RC constant according to IEC-60950 chapter 2.1.1.7 "discharge of capacitors in equipement" (user accessible parts).

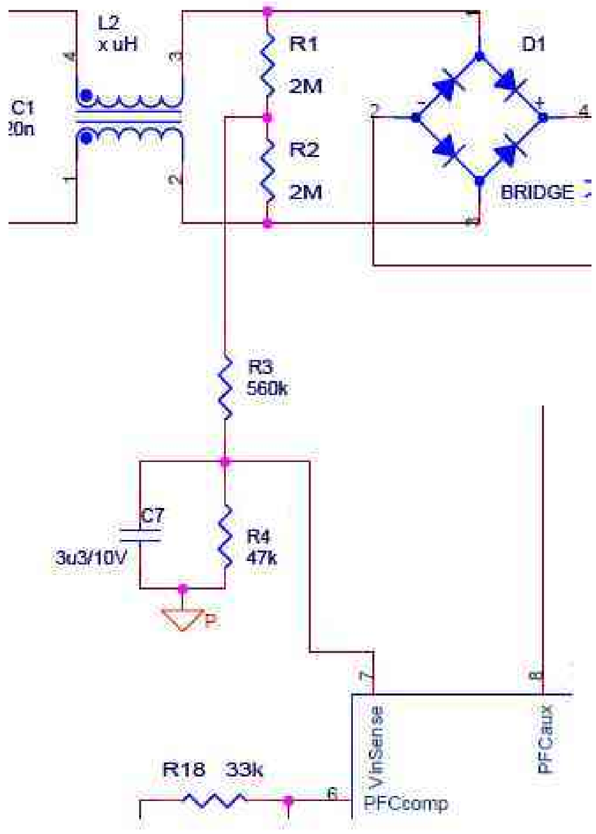
Fast Latch Reset (FLR)

In general, for a latched protection has to reset by means of the Vcc rail drop to its reset level via the bulk-elcap voltage discharge gradually but this may take times.

In TEA1750 with mains switch-off, the voltage at pin VinSense will drop below V_{FLR}. This will trigger the FLR circuit, but will not reset the latch. After mains switch on, the voltage at pin VinSense will rise again and when 0.85V is passed the latch will be reset then.

When the latched protection is set, the clamping circuit of the VinSense circuit is disabled.

The reverse leakage current of the bridge diode in hot condition may longer the FLR period of time.



Mains Undervoltage Lock-out/Brownout

The VinSense pin only stops the PFC when it drops below 0.9V. This is done for mains interrupts. The flyback has to continue working during short mains interrupts (Line Voltage Sag). The IC will clamp the VinSense pin to a level just below the start level. When the mains returns, the capacitor on the pin can be recharged to the start level quickly and restart the PFC.

$$Vac\_brownout = Vstop\,(vinsense) \bullet \frac{\pi}{2\sqrt{2}} \bullet \frac{R1 + \dfrac{R2 \bullet (R3+R4)}{R2+(R3+R4)}}{\dfrac{R2 \bullet (R3+R4)}{R2+(R3+R4)}} \bullet \frac{R3+R4}{R4}$$

Only if the VoSense pin drops below its stop level ($V_{stop(FB)}$=1.6V), the flyback also stops. (or if the maximum on-time is reached) This will prevent the application from overheating during long brownout situations.

Input Voltage Sensing PFC (pin VINSENSE)						
$V_{stop(VINSENSE)}$	Low input voltage detection level		0.87	0.9	0.93	V
$V_{start(VINSENSE)}$	Input voltage detection level		1.11	1.15	1.19	V
$V_{delta(VINSENSE)}$	Input voltage pull-up under $V_{start(VINSENSE)}$	active after $V_{stop(VINSENSE)}$ is detected		−100		mV
$I_{delta(VINSENSE)}$	Maximum input voltage pull-up current	active after $V_{stop(VINSENSE)}$ is detected	−55	−47	−40	μA

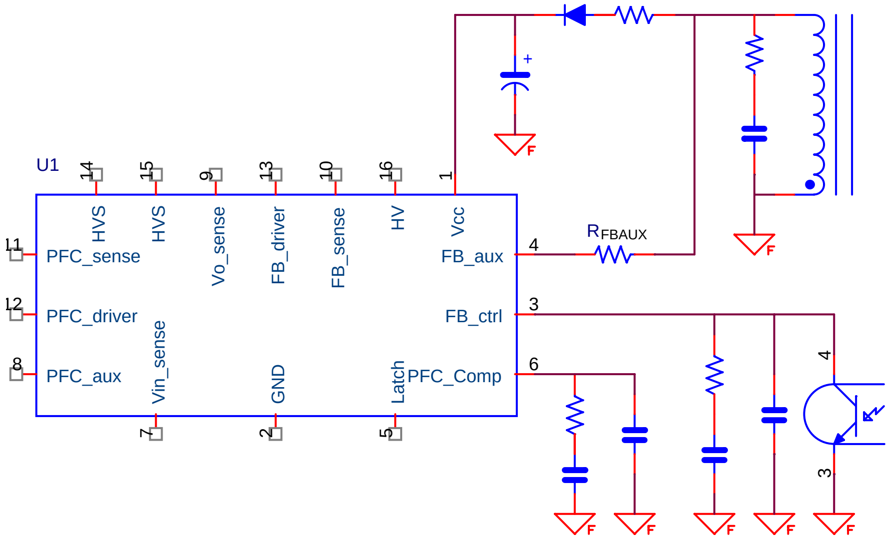
OVP Protection (PFC)

To prevent output overvoltage during load steps and mains transients, an over voltage protection circuit is built in. As soon as the voltage on the VOSENSE pin exceeds the Vovp(VOSENSE) level, switching of the power factor correction circuit is inhibited. Switching of the PFC recommences as soon as the VOSENSE pin voltage drops below the Vovp(VOSENSE) level again. When the resistor between pin VOSENSE and ground is open, the overvoltage protection is also triggered.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Output voltage sensing PFC (pin VOSENSE)						
$V_{th(ol)(VOSENSE)}$	open-loop threshold voltage on pin VOSENSE		0.35	0.40	0.45	V
$V_{start(fb)}$	flyback start voltage	[2]	-	1.72	-	V
$V_{stop(fb)}$	flyback stop voltage		1.55	1.60	1.65	V
$V_{burst(L)}$	LOW-level burst mode voltage		1.87	1.92	1.97	V
$V_{burst(H)}$	HIGH-level burst mode voltage		2.19	2.24	2.29	V
$V_{reg(VOSENSE)}$	regulation voltage on pin VOSENSE	$I_{O(PFCCOMP)} = 0$	2.475	2.500	2.525	V
$V_{ovp(VOSENSE)}$	overvoltage protection voltage on pin VOSENSE		2.60	2.63	2.67	V
$I_{I(VOSENSE)}$	input current on pin VOSENSE	$V_{VOSENSE} = 2.5$ V	5	45	100	nA

OVP Protection (Flyback)

The TEA1750 by sensing the auxiliary voltage via the current flowing into pin FBAUX during the secondary stroke. If the output voltage exceeds the OVP trip level, an internal counter starts counting subsequent OVP events. The counter has been added to prevent incorrect OVP detection which might occur during ESD or lightning events. As the protection is latched, the converter only restarts after the internal latch is reset. In a typical application the mains should be interrupted to reset the internal latch.



OVP Protection (Flyback)

The output voltage Vovp(FBAUX) at which the OVP function trips, can be set by the demagnetization resistor, R_{FBAUX}:

$$V_{o(ovp)} = \frac{N_S}{N_{aux}}(I_{ovp(FBAUX)} \times R_{FBAUX} + V_{clamp(FBAUX)})$$

Where Ns is the number of secondary turns and Naux is the number of auxiliary turns of the transformer. Current Iovp(FBAUX) is internally trimmed.The value of R_{FBAUX} can be adjusted to the turns ratio of the transformer, thus making an accurate OVP detection possible.

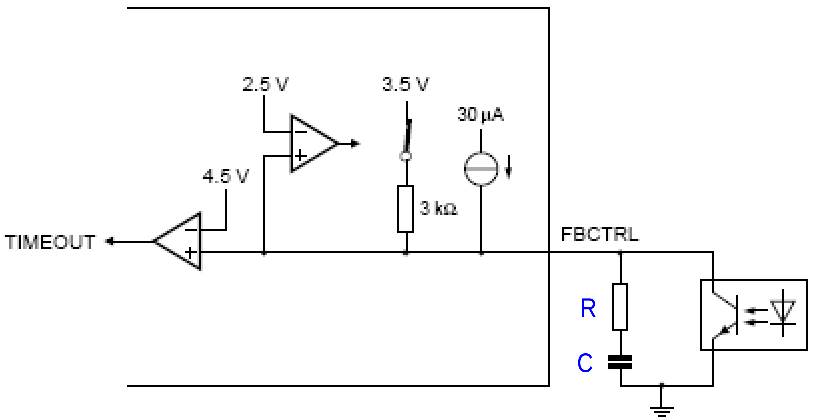
Overvoltage protection flyback (pin FBAUX)					
$I_{ovp(FBAUX)}$	overvoltage protection current on pin FBAUX	279	300	321	µA
$N_{cy(ovp)}$	number of overvoltage protection cycles	6	8	12	

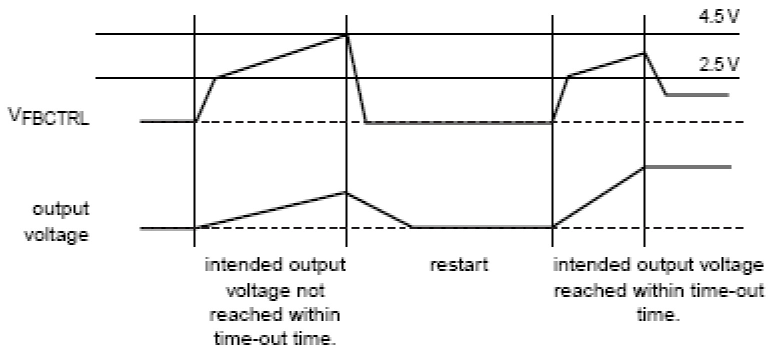
Time-out Functionality

The FBCTRL pin is connected to an internal voltage source of 3.5V via an internal resistor. As soon as the voltage on this pin is above 2.5V, this connection is disabled. Above 2.5V the pin is biased with a small current. When the voltage on this pin rises above 4.5V, a fault is assumed and switching is inhibited.

When a small capacitor is connected to this pin, a time-out function can be created to protect against an open control loop situation. The time-out function can be disabled by connecting a resistor (100k) to ground on the FBCTRL pin.

Time-out: $t = (C \times (V_{TO} - (I_{TO} \times R))) / I_{TO}$





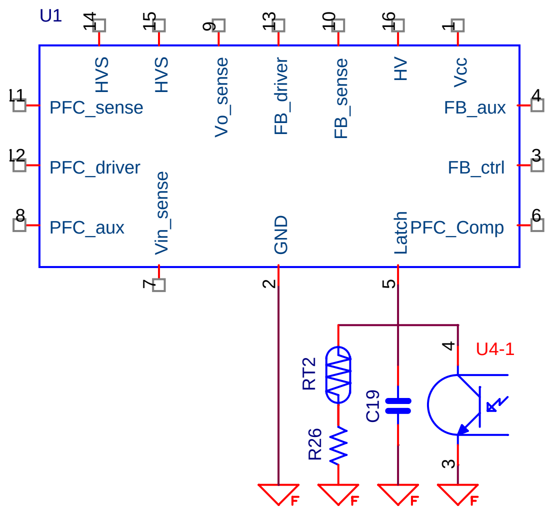
Latch Protection

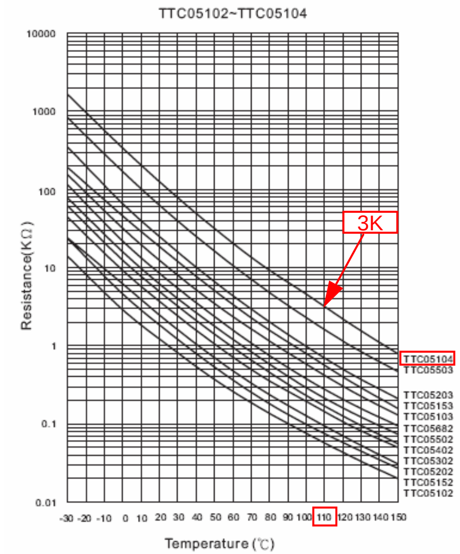
Pin LATCH is a general purpose input pin, which can be used to switch off both converters. The pin sources a current, $I_{O(LATCH)}$ on pin LATCH. Switching of both converters is stopped as soon as the voltage on this pin drops below 1.25V.

At initial start-up, switching is inhibited until the voltage on the LATCH pin is above 1.35V. No internal filtering is done on this pin. An internal zener clamp of 2.7V will protects this pin from excessive voltages.

In the example given, the LATCH pin is connected to a NTC resistor. When the resistance drops below $\frac{V_{prot(LATCH)}}{I_{O(LATCH)}} = 15.6\ k\Omega$, the protection is activated.

Here‘s a workable values ☞
where RT2=100KΩ (TTC05104)
R26=13.7KΩ without U4-1





Comparison of Gate Driver Capability

GC II:

V_{CC} management (pin 9)						
$V_{CC(start)}$	start-up voltage on V_{CC}		10.3	11	11.7	V
$V_{CC(UVLO)}$	under voltage lock-out on V_{CC}		8.1	8.7	9.3	V
Driver (pin 5)						
I_{source}	source current capability of driver	V_{CC} = 9.5 V; V_{DRIVER} = 2 V	–	–170	–88	mA
I_{sink}	sink current capability of driver	V_{CC}= 9.5 V; V_{DRIVER} = 2 V	–	300	–	mA
		V_{CC} = 9.5 V; V_{DRIVER} = 9.5 V	400	700	–	mA

GC III:

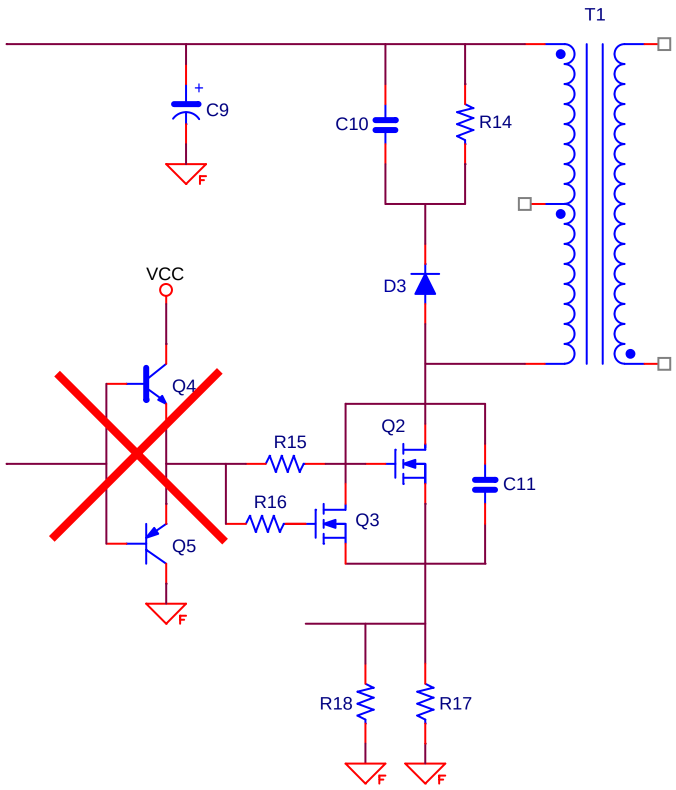
Supply voltage management (pin VCC)						
V_{trip}	VCC supply current trip point		0.55	0.65	0.75	V
$V_{startup}$	start-up voltage		21	22	23	V
V_{UVLO}	undervoltage lockout voltage		14	15	16	V
Driver (pin PFCDRIVER)						
$I_{src(PFCDRIVER)}$	driver source current PFC	$V_{PFCDRIVER}$ = 2 V	-	−0.5		A
$I_{sink(PFCDRIVER)}$	driver sink current PFC	$V_{PFCDRIVER}$ = 2 V		0.7		A
		$V_{PFCDRIVER}$ = 10 V	-	1.2	-	A
$V_{o(PFCDRIVER)}$	maximum driver output voltage PFC		-	11	12	V
Driver (pin FBDRIVER)						
$I_{src(FBDRIVER}$	driver source current flyback	$V_{FBDRIVER}$ = 2 V	-	−0.5		A
$I_{sink(FBDRIVER)}$	driver sink current flyback	$V_{FBDRIVER}$ = 2 V		0.7		A
		$V_{FBDRIVER}$ = 10 V	-	1.2	-	A
$V_{o(FBDRIVER)}$	maximum driver output voltage flyback		-	11	12	V

TEA1750/1 Driver Capability

With a higher supply voltage, the driver circuit to the gate of the power MOSFET has a current source capability of typically -500mA and a current sink capability of typically 1.2A. This permits fast turn-on and turn-off of the power MOSFET for high efficient operation.

Highlight:

- The TEA1750 was designed in a triple outputs 250W SMPS with a surge load up to approx. 500W.
- There's no extra totem pole (Q4 & Q5) driver circuitry needed for both PFCdriver and FBdriver pins anymore.



Comparison of TEA1751 vs. TEA1750
Additional Features

Comparison of TEA1751 vs. TEA1750 (1/3)

The main difference between the TEA1751 and the TEA1750 is the dual/fixed boost functionality and PFC control.
In the TEA1751 there is a dual boost implemented. The TEA1750 has a fixed output voltage for the PFC.
At low power conditions, the TEA1750 flyback controller switches the PFC to burst mode to maintain a relative high voltage on the output capacitor of the PFC (input voltage for flyback).
The TEA1751 switches off the PFC at low load conditions. The flyback will then operate on the rectified mains voltage.

Because the TEA1751 flyback runs on a larger input range, an over power protection (OPP) is build in. At higher mains voltages, the maximum peak current of the flyback will be limited. The mains voltage is measured by measuring the current on pin FBaux during the primary stroke of the flyback.
The TEA1750 does not need OPP, because the flyback operates on a fixed input voltage at normal and high load conditions.

At start-up the TEA1750 waits for the VinSense pin to cross $V_{start(VinSense)}$ (1.15V) to start the PFC, in order to ensure a high enough input voltage for the PFC converter to start.
To start the flyback the TEA1750 waits for the VoSense pin to cross $V_{start(FB)}$ (1.72V), in order to ensure a high enough input voltage for the flyback converter.

The TEA1751 starts the PFC and flyback converters simultaneously when the VinSense pin crosses $V_{start(VinSense)}$.

Comparison of TEA1751 vs. TEA1750 (2/3)

Pin	Symbol	TEA1751 (Dual Boost)	TEA1750 (Fixed Boost)
1	VCC	Supply voltage	Same as TEA1751
2	GND	Ground	Same as TEA1751
3	FBCTRL	Control input for flyback	Same as TEA1751
4	FBAUX	Input from auxiliary winding for demagnetization timing and OVP for flyback	Same as TEA1751
5	LATCH	General purpose protection input	Same as TEA1751
6	PFCCOMP	Frequency compensation pin for PFC	Same as TEA1751
7	VINSENSE	Sense input for mains voltage An additional voltage level detection for dual boost operation	Sense input for mains voltage N/A
8	PFCAUX	Input from auxiliary winding for demagnetization timing for PFC	Same as TEA1751 but additional capacitor & diode(s) are required for correct PFC demag and valley detection
9	VOSENSE	Sense input for PFC output voltage Built-in a current source for dual boost operation	Sense input for PFC output voltage A built-in detection circuitry for burst mode operation
10	FBSENSE	Programmable current sense input for flyback A built-in compensation circuitry with the current information where from FBaux pin for OPP correction at low/high mains	Programmable current sense input for flyback N/A
11	PFCSENSE	Programmable current sense input for PFC	Same as TEA1751
12	PFCDRIVER	Gate driver output for PFC	Same as TEA1751
13	FBDRIVER	Gate driver output for flyback	Same as TEA1751
14,15	HVS	High voltage safety spacer, not connected	Same as TEA1751
16	HV	High voltage start-up and valley sensing of flyback part	Same as TEA1751

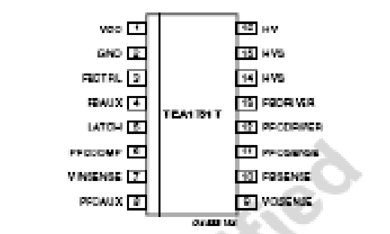


Fig 2. Pin configuration: TEA1751T (SOT109-1)

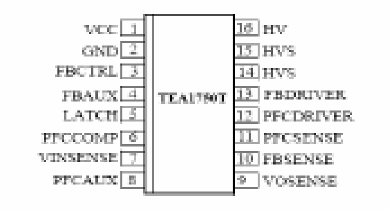
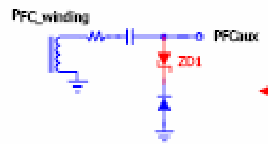


Fig 2. Pin configuration: TEA1750T (SOT109-1).

Comparison of TEA1751 vs. TEA1750 (3/3)

	Parameters	TEA1751	TEA1750
PFC			
	Boost Configuration	Dual Boost	Fixed Boost
1	VinSense pin Dual boost voltage	Current switch-over point=2.2V Switch-over region=200mV	N/A N/A
2	VoSense pin - PFC open-loop and short pin detection voltage - Dual boost output current - Start voltage for flyback converter - Stop voltage for flyback converter - Low voltage during burst mode operation - High voltage during burst mode operation - Input current VoSense pin	$V_{th(ol)(VoSense)}$=1.15V $I_{dualboost}$: -30nA to -15μA N/A N/A N/A N/A N/A	$V_{th(ol)(VoSense)}$=0.4V N/A $V_{start(FB)}$=1.72V $V_{start(FB)}$=1.6V $V_{burst(low)}$=1.92V $V_{burst(high)}$=2.63V $I_{i(VoSense)}$= 45nA
3	PFCsense pin PFC demag and valley detection	N/A	(refer to below drawing) Additional capacitor & diode(s) are required
4	PFCaux pin Soft-stop voltage for PFC	N/A	$V_{stopt(soft)(PFC)}$=0.45V
Flyback			
1	Maximum on-time for flyback	$t_{on(max)(FB)}$=40μs	$t_{on(max)(FB)}$=25μs
2	FBsense pin - Current in pin FBaux where the OPP curve starts - Current in pin FBaux current where Vsense(fb)(max) has reduced to 0.37V	- $I_{OPP(start)}$=-100μA - $I_{OPP(reduced)}$=-360μA	- N/A - N/A

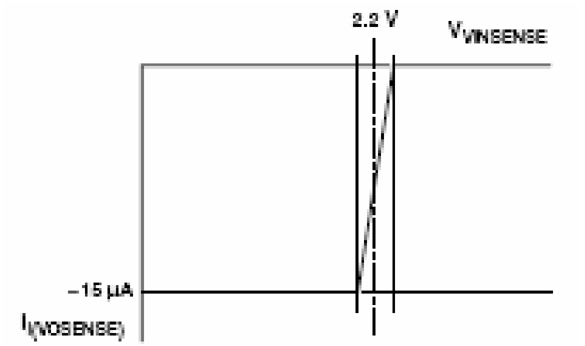


Vbulk_el-cap Calculation (TEA1751)

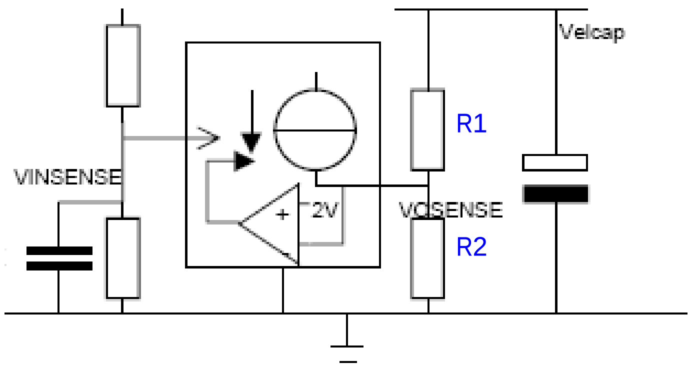
The VinSense voltage will control the current source as depicted below:

At high mains, the VinSense voltage is >2.2V. The injected current Ibst(dual) from the VoSense pin into R2 is 0μA. The Velcap is determined by the ratio of the R1 and R2 voltage devider which is $\frac{R1+R2}{R2} x 2.5V$.

At low mains, the current source (15μA) is injected from the VoSense pin into R2. The remaining current to set VoSense to 2.5V has to be supplied by R1. This remaining current is equal to $\frac{2.5V}{R2} - 15\,\mu A$. The Vbulk_el-cap is therefore calculated by $[(\frac{2.5V}{R2} - 15\,\mu A) x R1] + 2.5V$.



Voltage to current transfer function for dual boost PFC

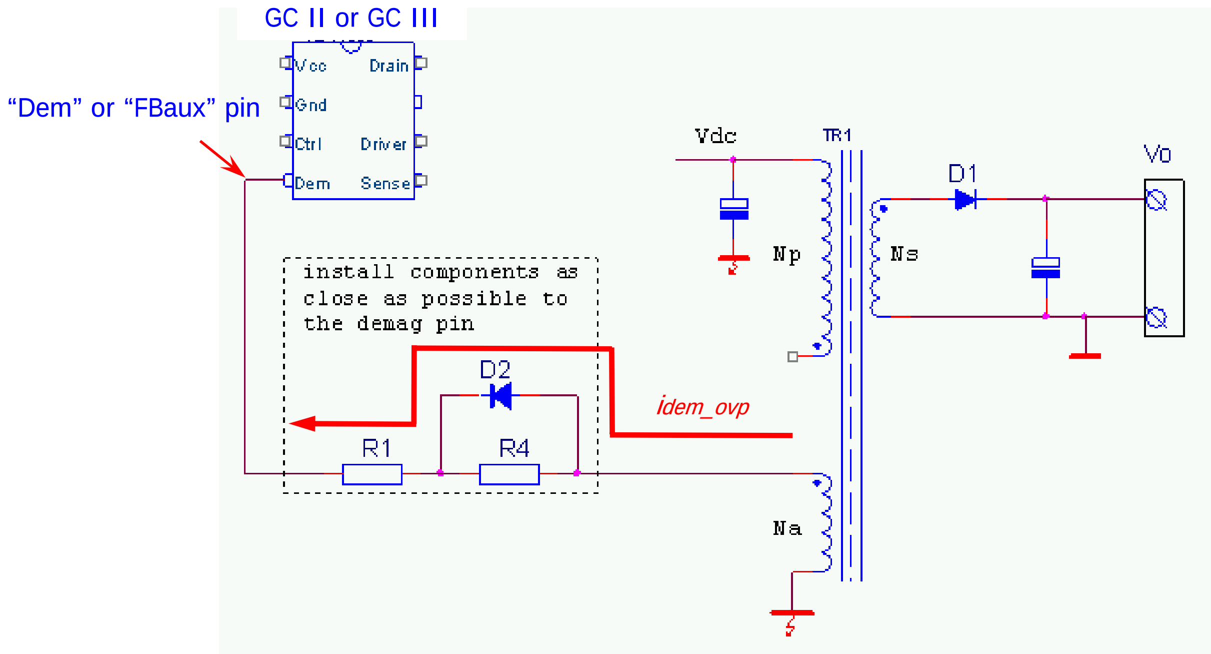


AC Mains (Vac)	VinSense (Vdc)
80	1.12
100	1.38
120	1.673
130	1.815
150	2.089
180	2.501
200	2.777
230	3.186
250	3.46
260	3.6

For example:
R1=9.3M (3.3M+3.3M+2.7M), R2=60.4K makes Vbulk_elcap=248Vdc at low mains and 387Vdc at high mains

OVP & Calculation (TEA1751)

An output overvoltage protection is implemented in TEA1751. By sensing the auxiliary voltage via the current flowing into pin FBaux during the secondary stroke. The auxiliary winding voltage is a well-defined replica of the output voltage. Voltage spikes are averaged by an internal filter.



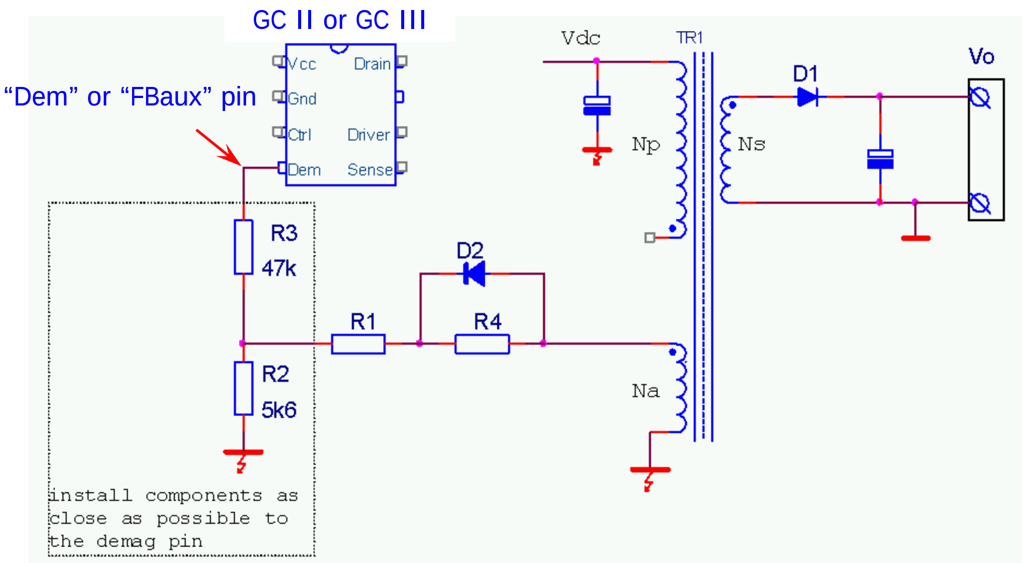
Calculation OVP resistor

$$R_1 = \frac{\frac{n_a}{n_s}\left(V_{o\_OVP} + V_{F\_D1}\right) - V_{F\_D2} - V_{dem\_clamp\_pos}}{i_{dem\_OVP}}$$

Calculation OPP resistor

$$R_4 = \frac{\frac{n_a}{n_p} V_{DC\_min} - V_{dem\_clamp\_neg}}{i_{dem\_OPP}} - R_1$$

OVP with Low Impedance Divider (TEA1751)



R3 and R2 should be chosen so, that the positive voltage across R2 is not lower than 2V.

Calculation OVP resistor

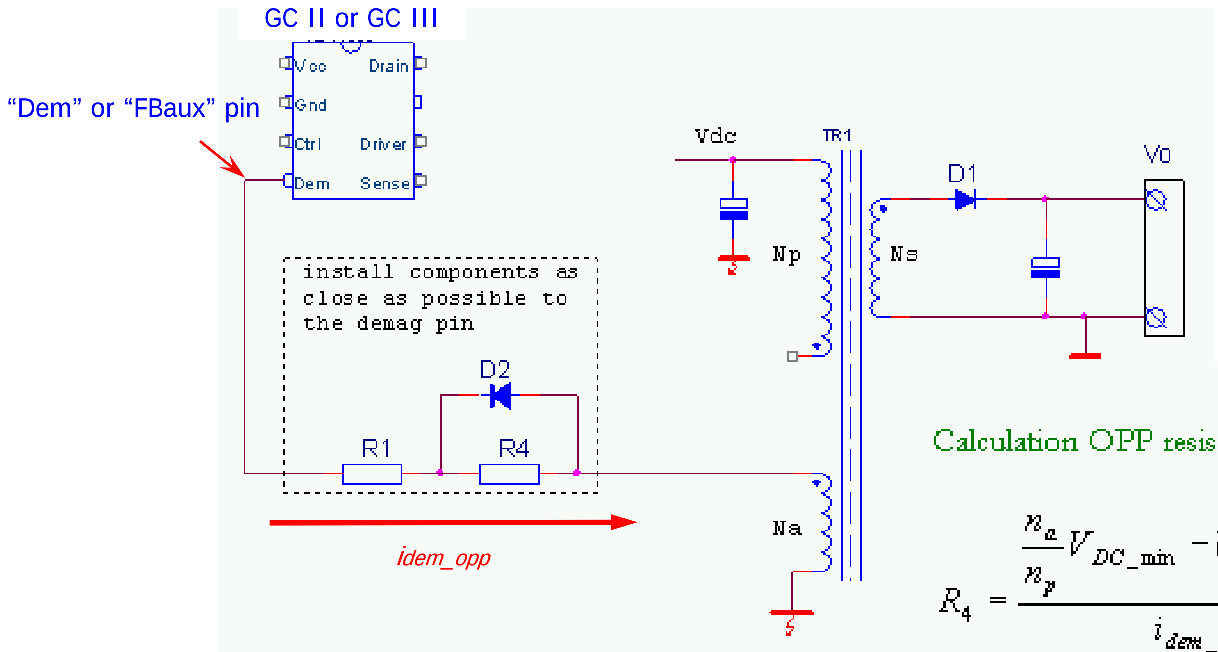
$$R_1 = \frac{\frac{n_a}{n_s}\left(V_{o\_OVP} + V_{F\_D1}\right) - \left(i_{dem\_OVP} \times R_3\right) - V_{F\_D2} - V_{dem\_clamp\_pos}}{i_{dem\_OVP} + \frac{i_{dem\_OVP} \times R_3 + V_{dem\_clamp\_pos}}{R_2}}$$

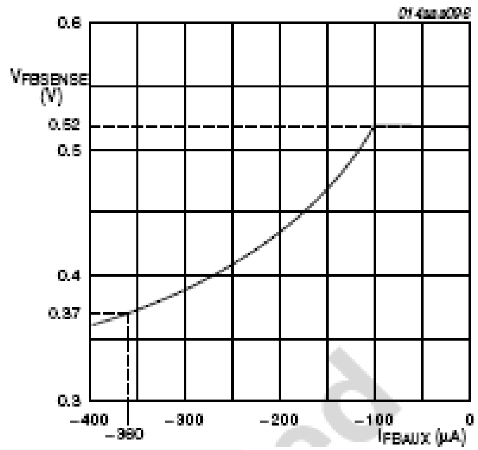
Calculation OPP resistor

$$R_4 = \frac{\frac{n_a}{n_p} V_{DC\_\min} - \left(i_{dem\_OPP} \times R_3\right) - V_{dem\_clamp\_neg}}{i_{dem\_OPP} + \frac{i_{dem\_OPP} \times R_3 + V_{dem\_clamp\_neg}}{R_2}} - R_1$$

OPP & Calculation (TEA1751)

During the primary stroke of the flyback converter the input voltage of the flyback converter is measured by sensing the current that is drawn from the pin FBaux. The current information is used to adjust the peak drain current of the flyback converter, which is measured via pin FBSENSE. The internal compensation is such that an almost input voltage independent maximum output power can be realized. The OPP curve is given below:





Over Power Protection curve

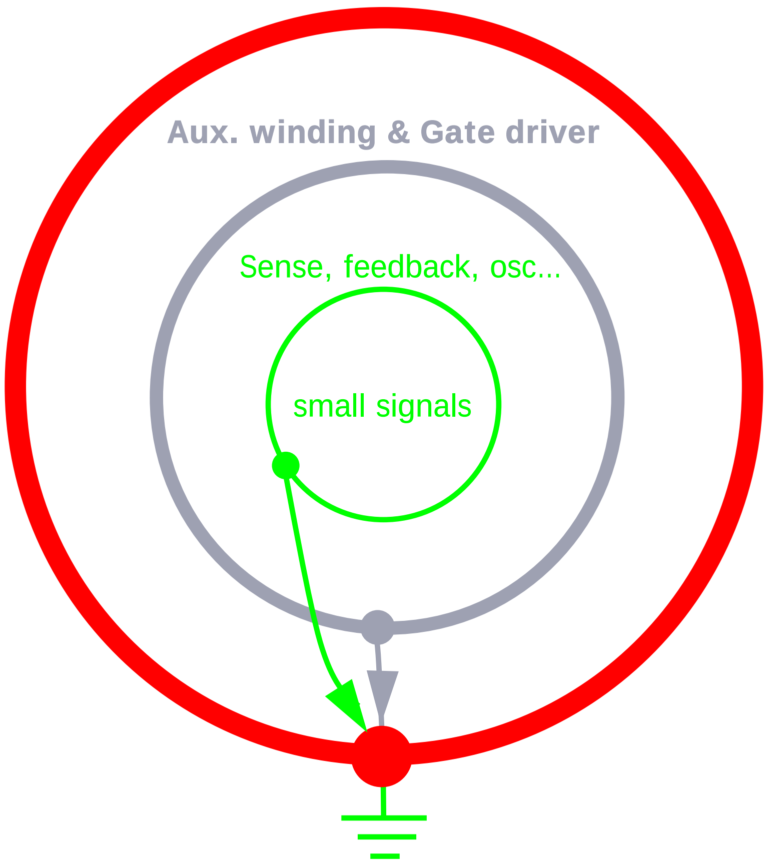
Calculation OPP resistor

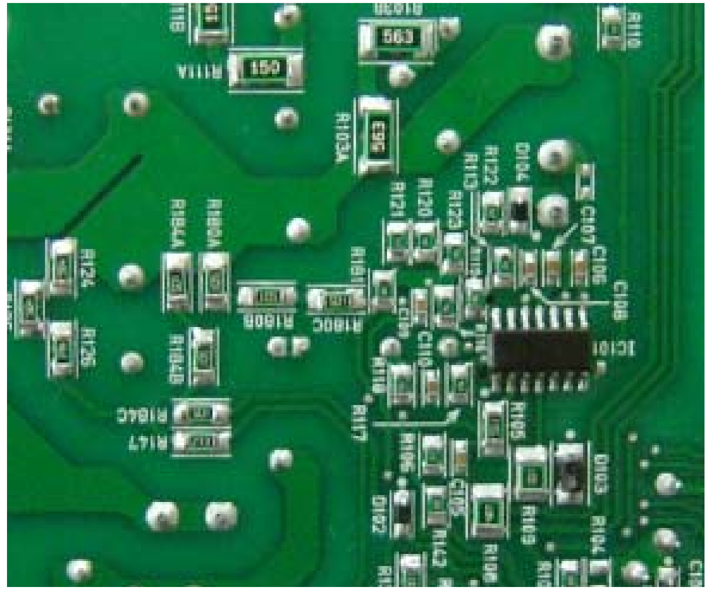
$$R_4 = \frac{\frac{n_a}{n_p} V_{DC\_min} - V_{dem\_clamp\_neg}}{i_{dem\_OPP}} - R_1$$

PCB Layout Considerations

The Basic Layout Concept - Grounding

Bulk el-cap, sensing resistor… high di/dt grounding





Poor grounding layout impacts:

1. Loop stability (oscillation, disturbance…etc)
2. DC offset on sense pin (power-up, peak load, PFC on/off…etc.)
3. More sensitive against lightning surge, ESD… events

Layout Considerations (1/3)

Proper layout techniques generally include minimizing high-current loops within the power stage, proper grounding of the control stage, and proper sizing of the traces to adequately handle the peak currents.

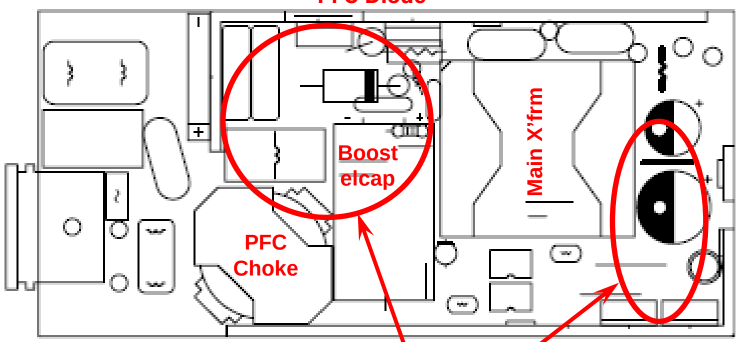
Switch Connections

In all cases care should be taken to keep the sense signals away from the high current loops.

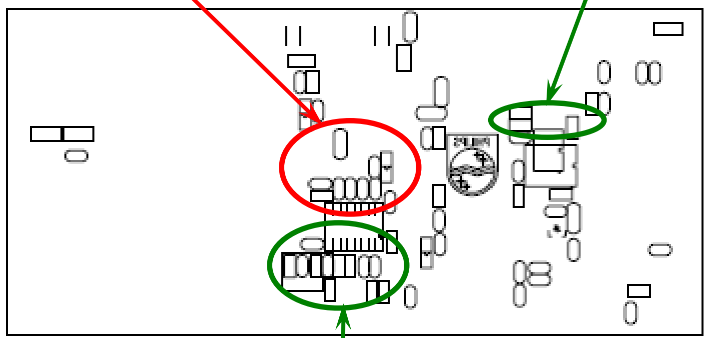
If at all possible keep the Vsense and Isense paths away from the power stages and FBsense & PFCsense paths.

PFC & Flyback FET

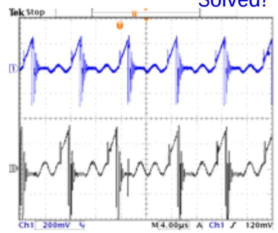
PFC Diode



S.R FETs



Solved!



Problem!

High Switching Voltage and Current Loops

Noise coupling can be greatly reduced by minimizing these loop areas.

Signal Connections

Sensitive low-level signals are away from the active switching components. All SMD parts should be mounted next to the controller to give the shortest possible routing.

Layout Considerations (2/3)

Item / Explanation
Capacitor Placement: ① A 1μF capacitor is physically as close as possible to the V_{CC} and ground pins, one SMD capacitor for each U1 & U3. ⇨ This ensures that the power running the internal logic of the IC is noise-free and stable. ② The boost elcap. (C3) should be located as close as possible to the Q1, Q2 and T1. ⇨ This reduces the high currents loop, reducing losses and minimize RFI noise disturbance. ③ It's recommended that to reserve a 100~470pF capacitor physically as close as possible to the PFCsense pin. ⇨ This helps prevent disturbance.
MOSFET Placement: ① The DRAIN and gate drive traces routing stays away from the quite analog sections of U1. ⇨ This prevents gate noise from upsetting the analog functions of the controller. ② When the gate lead trace is longer than approximately one inch, a small (10~47Ω) resistor should be placed in the trace near the MOSFET, one resistor for each MOSFET. ⇨ This minimizes trace inductance, reducing gate ringing.
Sense Resistor Placement: ① The sense resistor is physically located close to the MOSFET but do not across the DRAIN pin. ⇨ This minimizes the length of the power path, reducing losses and helps minimize noise pickup. ② The two sense resistors are as close together as physically possible, preferably located between Q1 and Q2 with "one point grounding" to each other if at all possible. ⇨ This minimizes the noise pickup into U1, and helps prevent crosstalk between PFC and flyback.

Layout Considerations (3/3)

Item / Explanation
GROUNDS ① All of the signal ground connections are attached together, and connect to the power ground plane at only one place, preferably the boost elcap. (C3) ground. ⇨ Separating signal and power ground avoids noise pickup into the analog functions of the controller. ② The controller IC (U1) has a continuous ground plane running underneath the entire chip area. ⇨ This helps minimize noise pickup into the analog functions of the controller. ③ The ground pin of U3 should go directly to the output ground plane after C37. ⇨ This minimizes ground bounce. ④ Use the ground plane as a shield for sensitive low-level signals away from the active switching components/traces. ⇨ This helps minimize noise pickup into U1.
Other Connections: ① The path from boost elcap. (C3) through the resistor divider (R5, R6 & R7) to the VoSense pin should be as short as possible, and also the R7/C4 should be located as closed as possible to the VoSense pin of U1. ⇨ This helps prevent both electric and lightning surge disturbances. ② R4, C20 & C21 should be located as closed as possible to the VinSense pin of U1. ⇨ This helps prevent disturbance. ③ The pin 5 of PFC choke (L2) should be located as closed as possible to the PFCaux pin of U1 via R27. ⇨ This helps prevent both electrical and lightning surge disturbances. ④ R4, C20 & C21 should be located as closed as possible to the VinSense pin of U1. ⇨ This helps prevent disturbance.

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