A HIGH POWER, HIGH FREQUENCY, DC TO DC CONVERTER FOR SPACE APPLICATIONS.

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ABSTRACT

This paper describes a regulated non-isolated Weinberg boost converter with the following advantages:

** Breadboard efficiency between 95 to 97% at from 500W to 1KW output power.*

** Continuous output current with small current ripple.*

** A Boost Regulator without the right half-plane zero effect giving a high bandwidth response.*

** Low switching losses (typically 1% at a switching frequency of 350kHz.).*

** Conductance control produces typical first order response.*

** Wide bandwidth voltage regulation loop (10KHz, with 80° phase margin) giving superior transient response and reduced output filtering.*

1. INTRODUCTION

As far as satellites are concerned, the available performances are inevitably limited by the capability of the launcher and a strong effort is made to convert any mass saving into extra payload capability. A constant research is carried out on every sub-system of the spacecraft platform and payload in order to reduce their mass and make their operations more efficient.

We therefore studied the Weinberg topology because it has inherently high efficiency. The topology was invented in 1974, Ref.[1], but since that time there has been a marked improvement in power components (FETs) and circuit techniques (conductance control, Ref.[2]). The authors were curious to see how this converter could be improved using these new techniques and devices.

The study was made for the topology when configured as a high power non-isolated boost converter because this type is necessary for most satellite power systems, especially when battery power storage is required to supply a regulated main voltage bus.

2. IDEAL OPERATION

In this section we explain the ideal operation of a Weinberg converter, develop its characteristic waveforms and its steady state DC gain. Figure 2.1 shows a Weinberg Converter without galvanic isolation. For the analysis in this section we will ignore the effects of leakage and magnetising inductances.

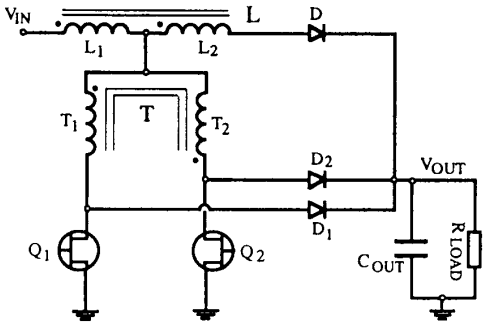

Fig. 2.1. Weinberg converter without galvanic isolation.

The basic operation mode of this converter has two states:

- Q_1 or Q_2 switched on, forcing D_2 or D_1 respectively to be also on, and D off.
- Q_1 and Q_2 switched (both) off, and D on.

By PWM control of Q_1 and Q_2 the output voltage of the converter can be controlled. This PWM action occurs twice every switching period of the converter and therefore effectively doubles the PWM switching frequency. This has the benefit of reducing the size of the magnetic and filter components and increasing the bandwidth of the converter, without increasing the switching losses.

<u>On state. (Q_1 on, Q_2 off, D_1 off, D_2 on, D off)</u>

Let's suppose that one of the MOSFETs is on and the other is off. Then, the equivalent circuit is as figure 2.2 shows:

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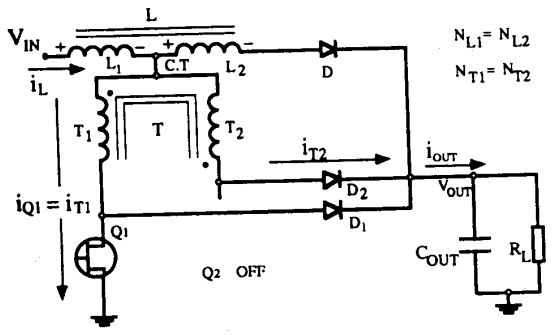

Figure 2.2. One of the states of operation.

Assuming Q_1 is turned on, and L_1 is feeding current to the centre tap, there is a current i_{T1} flowing through it and the primary winding T_1 of the transformer. If T_1 and T_2 have the same number of turns, the transformer effect forces T_2 to have the same magnitude of current ($i_{Q1} = i_{T2}$) flowing through it. Because Q_2 is off, this current flows through D_2 to the output. Therefore, T_2 is connected to the output. The transformer effect fixes the voltage in the centre tap (v_{CT}) to half the output voltage:

$$[v_{CT}]_{ON} = \frac{V_{OUT}}{2} \qquad (2.1)$$

This results in both D_1 and D being turned off, therefore the equivalent circuit is:

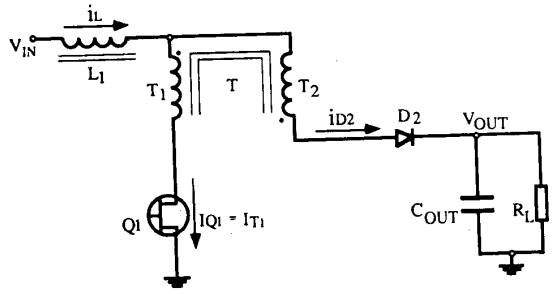

Figure 2.3. Equivalent circuit during the on-state.

Because the input current (i_L) passing through L_1, is equal to:

$$i_L = i_{Q1} + i_{D2} \qquad (2.2)$$

And, knowing that:

$$i_{Q1} = i_{D2} = i_{OUT} \qquad (2.3)$$

We have:

$$[i_L]_{ON} = 2\,[i_{OUT}]_{ON} \qquad (2.4)$$

The inductor current ripple is easily calculated, because the voltage across L_1 is :

$$v_{L_1} = V_{IN} - \frac{V_{OUT}}{2} = L_{ON}\frac{\Delta i_L}{\Delta t} \qquad (2.5)$$

where L_{ON} is the inductance of the main inductor during the on-time ($L_1 = L_{ON}$). This means:

$$\left[\frac{\Delta i_L}{\Delta t}\right]_{ON} = \frac{V_{IN} - \frac{V_{OUT}}{2}}{L_{ON}} \qquad (2.6)$$

From eq. (2.4), this last expression can be rewritten as:

$$\left[\frac{\Delta i_{OUT}}{\Delta t}\right]_{ON} = \frac{1}{2}\left[\frac{\Delta i_L}{\Delta t}\right]_{ON} = \frac{2V_{IN} - V_{OUT}}{4L_{ON}} \qquad (2.7)$$

Off state, (both FETs off, D on)

When we turn off Q_1, the voltage of the main inductor windings (L_1 and L_2) reverses to keep constant inductor ampere-turns and thus core flux constant.

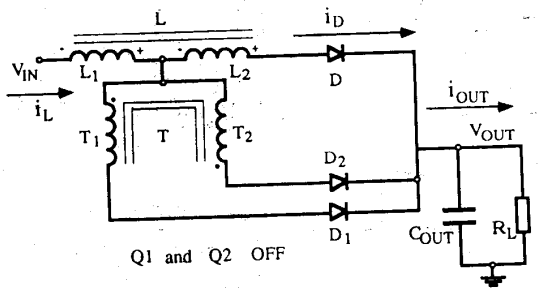

Figure 2.4. Equivalent circuit when both switches are turned off.

Once the voltage on the anode of D is equal to the output voltage, D becomes forward biased. The current flows also through the second winding of the inductor (L_2) to keep its flux constant.

Since both inductor windings have the same number of turns (N), the inductor value in this state is:

$$L_{OFF} = (N_{L1} + N_{L2})^2 A_L = 4N^2 A_L = 4L_{ON} \qquad (2.8)$$

The current through the inductor (and the diode D) is:

$$[i_L]_{OFF}\,2N = [i_L]_{ON}\,N \qquad (2.9)$$

Thus:

$$[i_{OUT}]_{OFF} = i_D = [i_L]_{OFF} = 1/2\,[i_L]_{ON} \quad (2.10)$$

So, by examining eqs. (2.4) & (2.10), it can be seen that the output current is continuous, and applying conductance control, the voltage feedback regulation will be first order. Now, we have:

$$\left[\frac{\Delta i_L}{\Delta t}\right]_{OFF} = \left[\frac{\Delta i_{OUT}}{\Delta t}\right]_{OFF} = \frac{V_{IN} - V_{OUT}}{4\,L_{ON}} \quad (2.11)$$

Because of the inductor coupling effect, we have:

$$V_{IN} - v_{CT} = v_{CT} - V_{OUT} \quad (2.12)$$

Giving:
$$[v_{CT}]_{OFF} = \frac{V_{IN} + V_{OUT}}{2} \quad (2.13)$$

As a resume of the principle of operation of this converter, the main ideal waveforms (fig.2.5) are compared to the actual ones (fig 2.6).

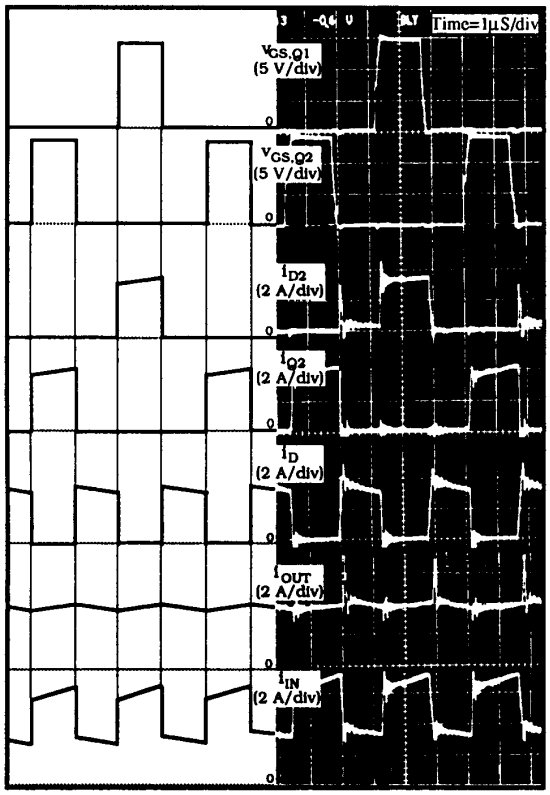

Fig. 2.5. Ideal waveforms. Fig. 2.6. Real waveforms.

Steady state DC gain.

For steady state conditions the rise in output current during the on-time is equal to the fall in current during the off-time. So, defining the duty cycle as:

$$D = \frac{t_{ON}}{T_{SWITCHING}} \quad (2.14)$$

where $T_{SWITCHING}$ is half the push-pull switching period, and looking at eqs. (2.7) and (2.11), we have:

$$\frac{2\,V_{IN} - V_{OUT}}{4\,L_{ON}} D = -\frac{V_{IN} - V_{OUT}}{4\,L_{ON}} (1-D) \quad (2.15)$$

Therefore:

$$V_{OUT} = (1+D)\,V_{IN} \quad (2.16)$$

This shows that the output voltage can reach any possible value between the input voltage and twice the input voltage, unlike a conventional boost which can increase the output voltage, ideally, to an infinite value.

Output current ripple variation with the duty cycle.

The output current ripple always satisfies eq. (2.7), that can be rewritten as:

$$\Delta i_{OUT} = \frac{2V_{IN} - V_{OUT}}{4\,L_{ON}} t_{ON} \quad (2.17)$$

Just substituting V_{IN} from (2.16) and t_{ON} from (2.14) in the last expression, we have:

$$\Delta i_{OUT} = \frac{\left(\frac{2}{1+D} - 1\right) V_{OUT}}{4\,L_{ON}} \frac{D}{f_S} \quad (2.18)$$

where f_S is the "effective" PWM frequency and is equal to $1/T_{SWITCHING}$. Rearranging (2.18), we have:

$$\Delta i_{OUT} = \frac{V_{OUT}}{4\,L_{ON}\,f_S}\left(\frac{2\,D}{1+D} - D\right) \quad (2.19)$$

Figure 2.7 shows the variation of output current ripple expressed in eq. (2.19).

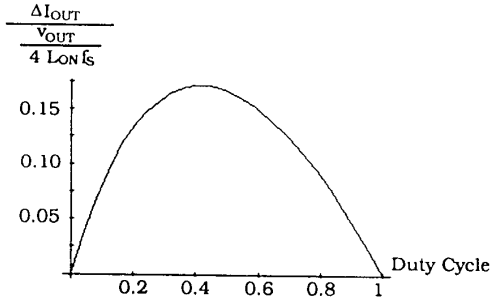

Fig. 2.7. Variation of output current ripple with duty cycle.

It's easy to find that the duty cycle for maximum output current ripple, is D = 41.4%. Therefore, the maximum output current ripple is, substituting in eq. (2.19):

$$\Delta i_{OUT} = 0.043 \frac{V_{OUT}}{L_{ON} f_S} = 0.17 \frac{V_{OUT}}{L_{OFF} f_S} \quad (2.20)$$

3. EFFECT OF PARASITIC ELEMENTS

In this section we will study the modifications of the ideal performance of a Weinberg converter due to its parasitic elements. The magnetising and leakage inductance of the transformer T and the leakage inductance of inductor L (as shown in fig. 3.1) change the actual performance of the converter as follows.

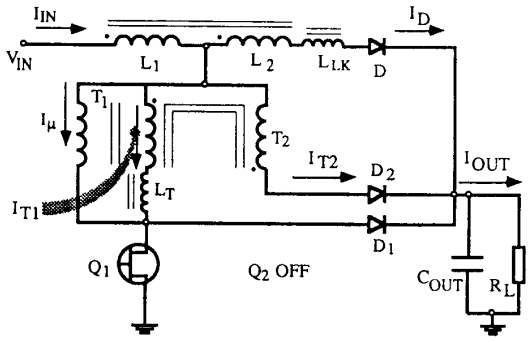

Fig. 3.1. Equivalent circuit with parasitic elements.

Transition from On to Off.

Consider first the case when Q_1 is conducting and diode D_2 is on. As we explained in the previous section, when we turn off Q_1, the voltages of the main inductor windings reverse to maintain constant inductor core flux. The centre tap voltage is clamped to V_{OUT} by D_1 and D_2. D becomes forward biased and the current starts to flow also through the second winding of the inductor (L_2) to keep its flux constant.

The main inductor leakage inductance (L_{LK}) however plays a role in the operation of the converter, during this period, because time is needed before current is built up in this inductance allowing D to conduct the total current. The equivalent circuit for this condition is shown in figure 3.2.

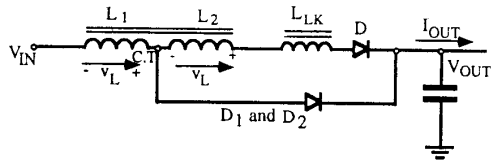

Figure 3.2. Effect of the leakage inductance.

Thus, during this transition (when v_{CT} is clamped to V_{OUT}), the voltage across winding L_1 (v_L) is:

$$v_L = V_{IN} - V_{OUT} \quad (3.2)$$

And:

$$v_{LK} = V_{OUT} - V_{IN} \quad (3.3)$$

Therefore, the increase of current through the diode D is:

$$\frac{\Delta i_{LLK}}{\Delta t} = \frac{v_{LLK}}{L_{LK}} = \frac{V_{OUT} - V_{IN}}{L_{LK}} \quad (3.4)$$

As the current in winding L_2 rises the current in winding L_1 falls at the same rate to keep a constant ampere-turns in the core, until i_{L2} equals i_{L1} and the central tap voltage reaches the expected value for the ideal case already calculated in the equation (2.13). In this transition i_{L1} keeps flowing to the output through D_1 and D_2, producing a spike in the output current. Its duration is:

$$t_{spike} = \frac{L_{LK}}{V_{OUT} - V_{IN}} I_{OUT} \quad (3.5)$$

Figure 3.3 shows the waveforms from the breadboard for the currents involved in the discussion above.

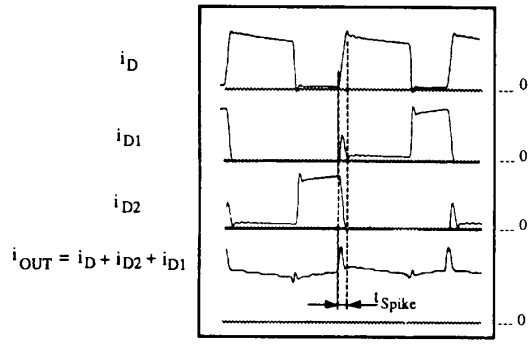

Fig. 3.3. Graphical explanation of the output current spike.

During the off time, the magnetising current of the transformer forces one of its winding extremes to reach V_{OUT}. Because the centre tap is also fixed, see eq. (2.13), it can be seen that the other winding extreme goes to V_{IN}. Figure 3.4 shows clearly this effect on the drain-source voltages of the switches.

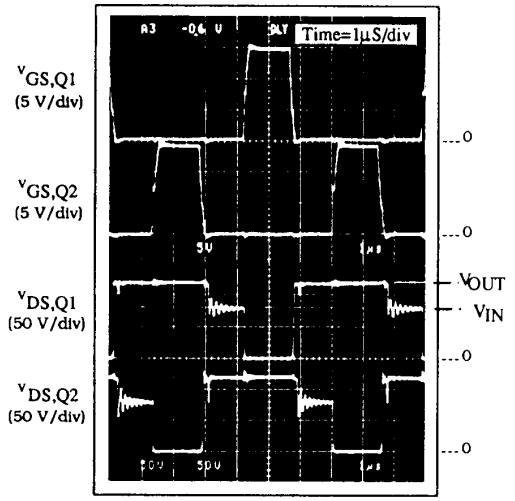

Figure 3.4. Voltage waveforms in both switches.

Transition from Off to On.

Figure 3.5 shows the equivalent circuit during this transition:

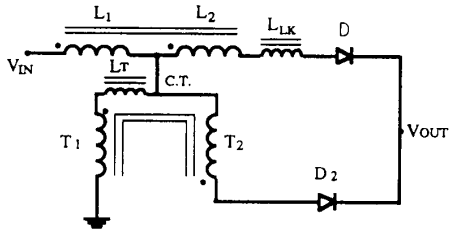

Figure 3.5. On transition with parasitic inductance.

Just the instant before turning on one of the FETs, all the current is flowing through the diode D and the voltage in the centre tap is:

$$v_{CT} = \frac{V_{IN} + V_{OUT}}{2} \qquad (3.6)$$

The current in the transformer does not build up instantaneously, due to the leakage inductances. It can be shown that the increase of current is:

$$\frac{\Delta i_{L_T}}{\Delta t} = \frac{v_{L_T}}{L_T} = V_{IN}\left(\frac{1}{L_T + L_{LK}}\right) \qquad (3.7)$$

4. CURRENT SENSING

For conductance control we need to sense the output current. As we have seen in figure 3.3 the output current has a spike which disturbs the measurement of this current. To overcome this problem we implemented a technique based on constant ampere-turns of the main inductor.

In section 2, we saw that during the on time, the current through the main inductor flowed in one of its windings, with a value that was twice the output current. During the off time both windings of the inductor conduct the output current. This is, of course, dictated by the need to keep constant ampere-turns in the inductor L for both states.

So, the addition of the current flowing in both windings of the main inductor is always twice the output current. The only difference between the real output current and the measured one is the current spike as figure 4.1 shows:

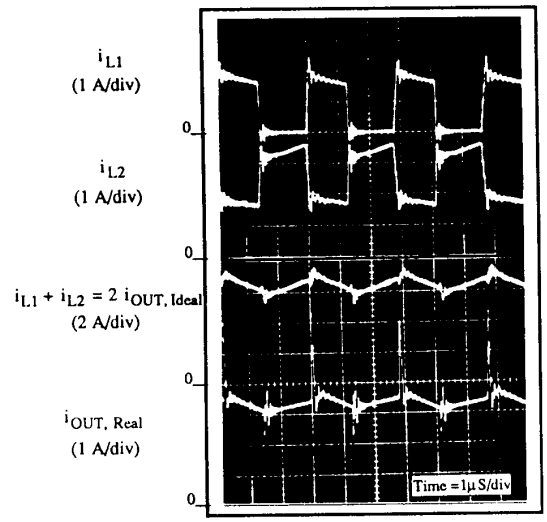

Figure 4.1. Measurement of the output current, using two current probes and summation to avoid the spike.

The current sensor built is based in a Hall Effect Device Current Sensor [Ref. 3]. And to sum the currents as above, two equal primary current sensor windings were used, each connected in series with the main inductor windings, as figure 4.2 shows:

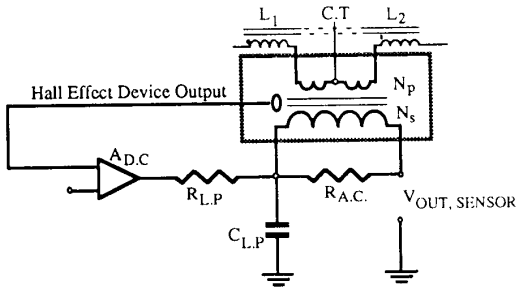

Figure 4.2. Hall Effect Device Current Sensor.

5. DYNAMIC RESPONSE.

Since our equivalent switching frequency is 350 KHz, a proper design of the current loop, employing conductance control, will allow us to close the current loop around 111 KHz with a phase margin close to 90°. The pole effect of the error amplifier (LM118) and the control circuit delay, start to decrease the phase margin from 90° to 74°, as figure 5.1 shows:

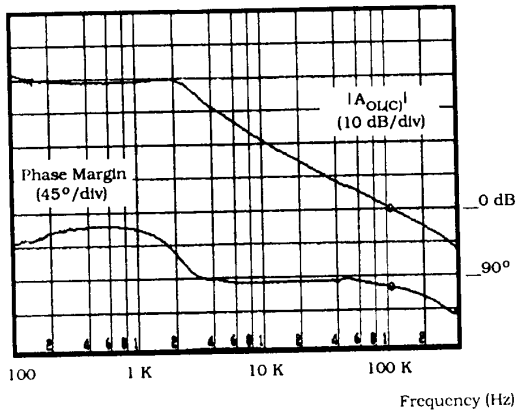

Figure 5.1. Open loop current transfer function.

The voltage loop is closed a decade lower than the current loop. This allows the second order system to appear as a first order one. Thus, a bandwidth of about 10 KHz with a phase margin of 80° is achieved, as shown in figure 5.2 .

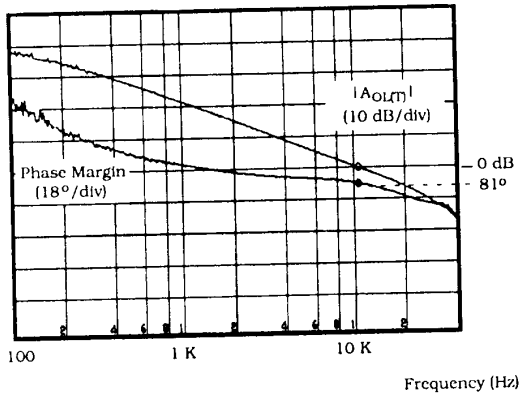

Figure 5.2. Open loop total transfer function.

Finally, adding an integrator in the voltage loop a decade lower than its bandwidth, it is possible to improve the regulator response. Figure 5.3 shows the output voltage response for a step load change with integrator in the voltage loop. The output voltage was 120 volts and the output DC current 5 amps.

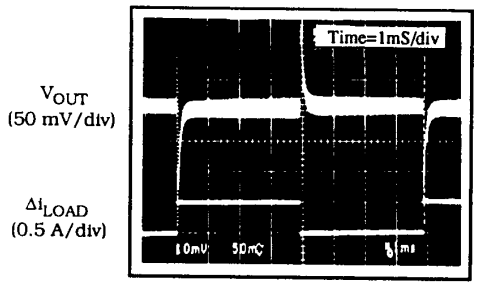

Figure 5.3. Step load response (time 1ms/div).

6. CURRENT LIMITATION

Because of conductance control, output and input current limitation can easily be achieved by clamping the voltage error signal.

This has the additional advantage of limiting the maximum current in the power semiconductors to a well defined value in the event of an overload. But like all non-isolated boost regulators, the output current limitation only operates correctly if V_{OUT} is greater than V_{IN}. This is because there is a direct DC path for unlimited current to flow if V_{OUT} falls below V_{IN}. Some input current limitation or fusing must be added to give overload protection for this case.

7. EFFICIENCY

We have just seen, in section 3, that slopes of the switching off and on transitions are controlled by the main inductor and transformer leakage inductances. For the switch-on case these inductances limit the switching losses, by controlling the slope of the current rise during the on transition, which will give nearly zero crossing between current and voltage and therefore a better efficiency. This is unlike a conventional boost or buck regulator which have a large switch on loss due to the reverse recovery loss of the output diode. Figure 7.1 shows this transition.

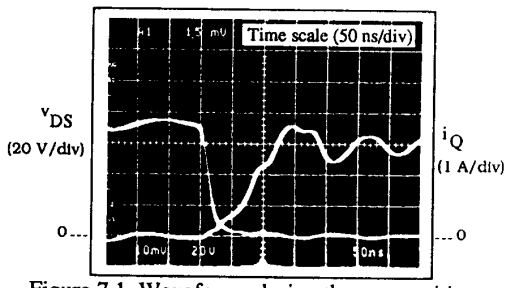

Figure 7.1. Waveforms during the on transition.

Figure 7.2 shows the main switch voltage and current crossing during the turn-off. From this picture, switching losses can be estimated as follows:

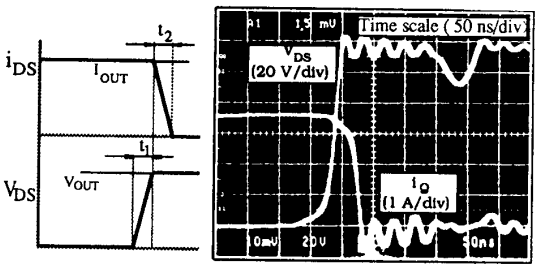

Figure 7.2. Off transition.

Because t_1 and t_2 are similar, we can write that:

$$P_{losses} = \frac{t_1}{T_S} I_{OUT} V_{OUT} \qquad (7.1)$$

This means that in our case the expected switching losses at 350 KHz are:

$$P_{losses} = 1.1\% P_{OUT} \qquad (7.2)$$

Figure 7.3 shows the efficiency measurements performed on a 1kW breadboard operating with a push-pull frequency of 175kHz and V_{OUT} 120Volts. Even with this high switching frequency a 600w breadboard efficiency does not fall below 95.5% .

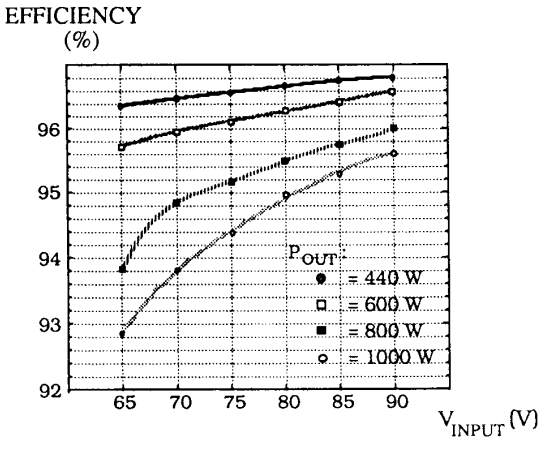

Figure 7.3. Efficiency for different power levels.

Figure 7.3 shows how the efficiency decreases when the power levels increase and when the input voltage decreases, as is the case in other conventional boost regulators.

8. CONCLUSION

The Weinberg converter just described is a boost regulator that gives continuous output current with only two reactive elements. This together with conductance control makes its small signal analysis especially simple. A high effective PWM switching frequency assures a dynamic response that is faster than other conventional PWM regulators in the same power range. Test results prove the regulator to be extremely stable.

It presents an excellent performance with respect to efficiency, low mass and power handling capability. Such a performance was achieved without any special effort being made. By the reduction of the copper losses, use of turn-off snubbers and parallel FETs, more optimum results could be obtained. In addition, integrated magnetic techniques would reduce the input current ripple, Ref. [4]. Peak currents and voltages are well defined.

By using a common feedback error voltage, conductance control allows an unlimited number of the similar converters to be connected in parallel, this can give unlimited output power and redundant operation Ref. [5].

The paper shows that the topology provides an excellent solution to high power conversion and being public domain is free for everyone's use.

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