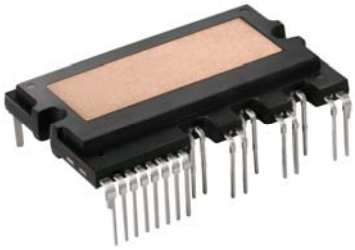
Application Note

PCB design guidance
Using SPM and PFCM for A/C system



This application-note is written by the urgent request of customer in Chaina so that the reader should consider its incompleteness. The final version will be officially opened a few months later. Thanks.

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Motion Control System
HV PCIA
FAIRCHILD SEMICONDUCTOR

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1. Introduction

Normally, PCB designers have to considerate of noise and current-rating when they design a PCB for applying to their system. Current-rating is relatively easy to design, but noise is not easy. Unfortunately, the solutions of A/C(air-conditioner) system are looking for cheapest one which is method using shunt-resistor instead of current transducer, so they have nothing to be sensitive to noise. In order to avoid mis-operating, basically PCB designers have need of minimizing the noise by PCB-layout. Thus, this application note is going to propose the PCB guidance for reducing the noise.

2. How to design the PCB for A/C

2.1. Air-Conditioner system

First, it is important that designers should know the root-cause of noise in the system. And then, designers is looking for reducing the noise indeed.

Figure(1) is shown in block of general A/C system.

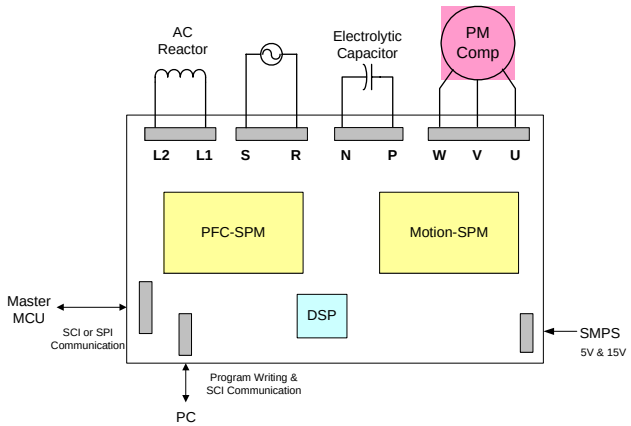


Figure 1. The block of A/C system

Generally, we already know what to divide between signal and power ground in a PCB design. But, it is not easy to divide between signal and power ground because A/C system has two kinds of power module such as Motion SPM and PFC-SPM.

We recommend that the PCB layout of A/C system is based on the single SPM layout because Inverter system requires more current-signals for control than PFC. Therefore, it should design the layout of PFC part after designing the single SPM layout in advance.

2.2. PCB design guidance for SPM

Figure(2) is shown in application circuit for **SPM**. When SPM design, the designers have to design considering following five things.

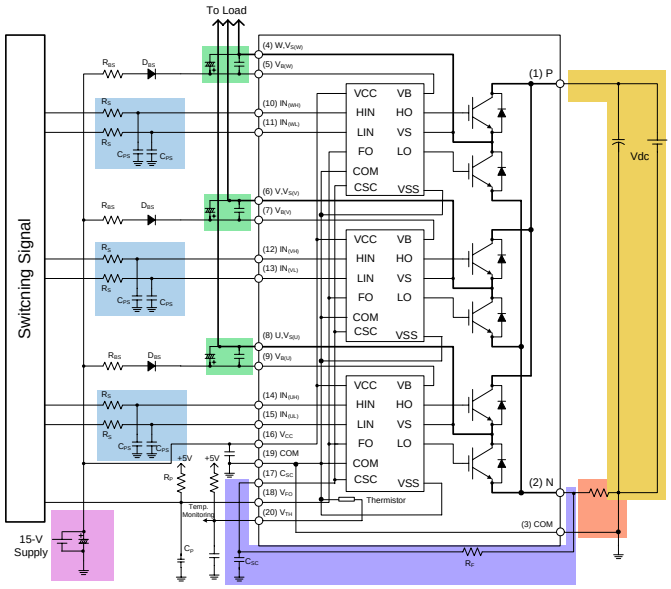


Figure 2. Important factors of SPM PCB pattern

1st, bootstrap capacitor and bypass-capacitor for Vbs of SPM are located near by SPM as closely as possible. The reason is because the Cbs of charged energy has to supply switching power for High-side IGBT. Figure(3) is shown in current-loop

for High-side IGBT.

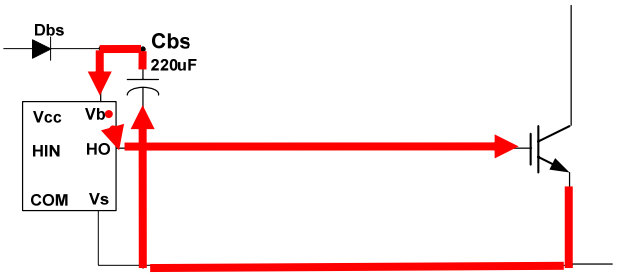
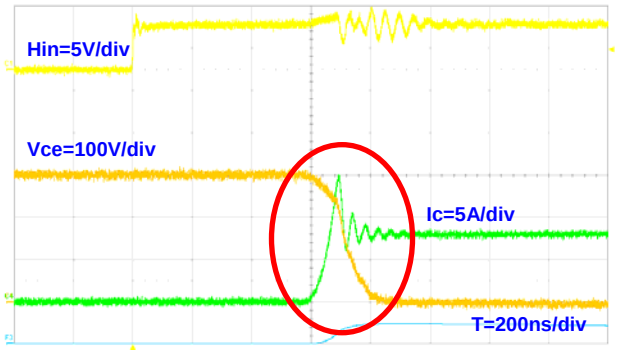


Figure 3. HVIC Current-loop for IGBT switching

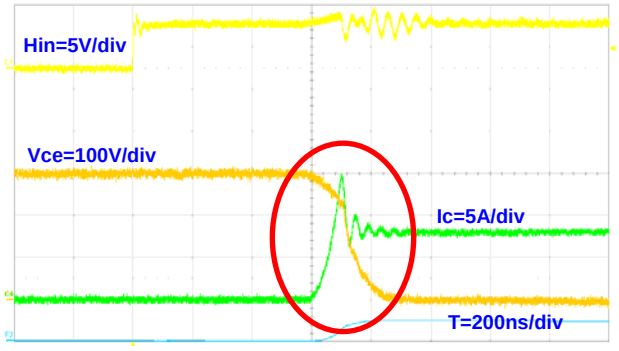
In case of IGBT, the characteristic of Ton depends on gate circuit, but the characteristic of Toff depends on IGBT characteristic. So, the length of Cbs(Bootstrap capacitor) pattern has an effect on Ton of IGBT. Figure(4) is shown in characteristic of Ton according to Cbs length.

In result, the longer Cbs pattern length makes the slower dv/dt and di/dt value and the larger switching loss in Ton switching. **It seems that switching-loss is increasing around 8 percent.** Also, LVT(Low Voltage Trip) is happened by Vbs ripple under long pattern test.

2nd, CE-capacitor (Condenser Electrolytic) and bypass-capacitor for Vcc of SPM are located near by SPM as closely as possible. The longer Vcc capacitor pattern length makes bigger oscillation and higher surge voltage in the Vcc-Com of SPM as shown in Figure(5). Furthermore, this oscillation and surge voltage might happen input signal noise and mis-operation in the HVIC/LVIC of SPM.



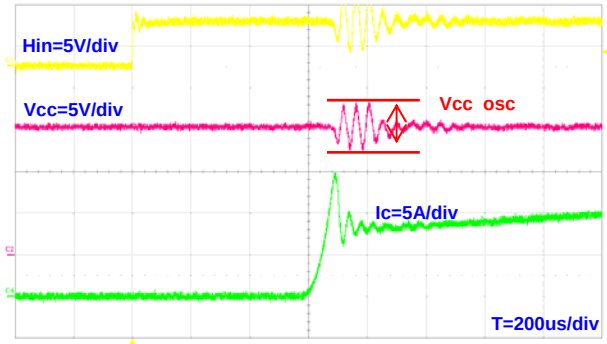
(a) Cbs Pattern length 1Cm



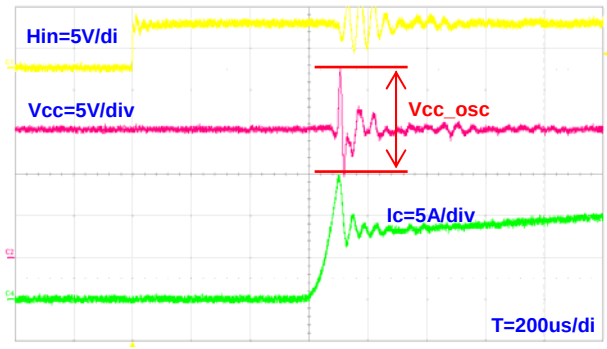
(b) Cbs Pattern length 15Cm

Test condition : Vdc = 300[V], Vcc = 15[V], Ic = 8[A]

Figure 4. Ton Characteristics by Cbs pattern



(a) Vcc-Cap Pattern length 2Cm

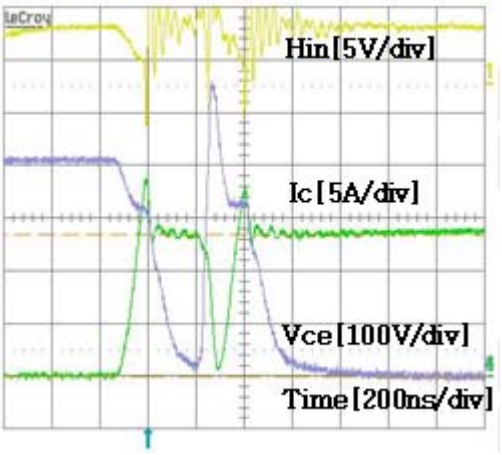


(b) Vcc-Cap Pattern length 10Cm

Test condition : Vdc = 300[V], Vcc = 15[V], Ic = 8[A]

Figure 5. AC Characteristics by Vcc cap. Pattern

3rd, the low-pass filter for input signal is located near by SPM. Usually, designers used to make a mistake in the location of filters near by MCU instead of SPM. If the filter's location were close by MCU, input signal would occur to big noise in the input-pin of SPM while IGBT turn on. At that time, the noise level of input signal gets through the input-hysteresis band and SPM may be mis-operateed. Figure(6) is shown in mis-operation of SPM by input-signal noise. If input filters were close by SPM, it might be clear.



Test condition : Vdc = 400[V], Vcc = 16.5[V], Ic =26[A]

Figure 6. Mis-operation by input-signal noise

4th, the most important thing is one point connection between signal and power ground when PCB design. In case of SPM, Com of SPM and DCN of Power is also connected by one point. This connected-pattern is not only gate current-loop for Low-side IGBT, but also makes the same electric-potential between signal and power ground. Furthermore, designers should considerate of measuring the currents from shunt resistors without noise.

PCB has to minimize sharing pattern of current pass as to reduce the noise. In case of Power ground, we recommend the DCN-side pin of shunt resistor when connecting the signal ground with power ground. In signal case, we recommend the ground pin of Vcc-com capacitor for SPM. In other words, the separating point should be DCN–side pin of shunt resistor and the connected pattern is as short as possible. The reason is because it becomes gate current-loop for Low-side IGBT.

Figure(7) is shown in gate current-loop for Low-side IGBT and Figure(8) is shown in how to connect with ground pattern on the PCB.

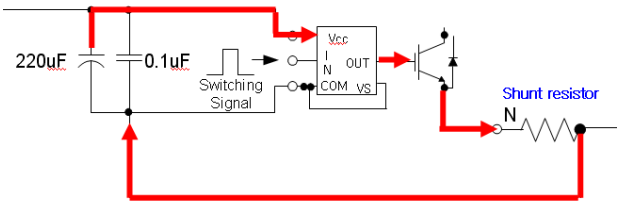


Figure 7. LVIC Current-loop for IGBT switching

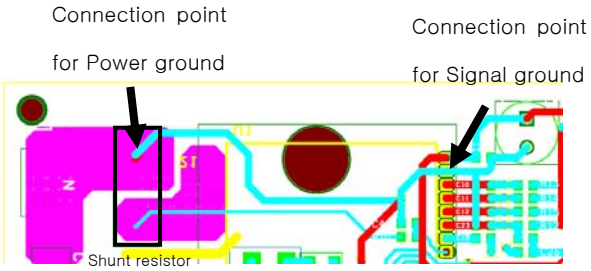


Figure 8. How to connect with ground pattern

Lastly, it is not difficult to detect the current from shunt resistor. We already connect with the signal and Power ground. Now, it has only to find the measuring point. Normally, the value of shunt-resistor is too small so we need to minimize the resistance of PCB pattern by location of current-sensing.. The most separating point is the SPM-side pin of shunt-resistor as shown in Figure(9).

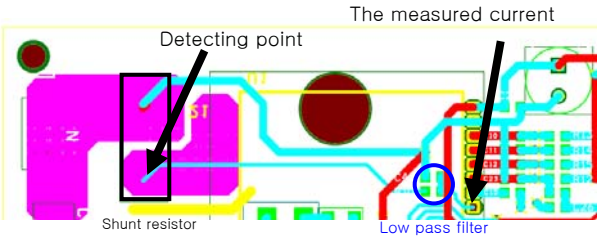


Figure 9. How to detect the current from Rshunt

5th, the snubber capacitor for protecting the IGBT is located near by SPM as close as possible. As see the Figure(10), the "B" position surge suppression effect is greater than the location 'A' or 'C'. The 'C' position is a reasonable compromise with better suppression than in location 'A' without impacting the current sensing signal accuracy. For this reason, the location 'C' is generally used.

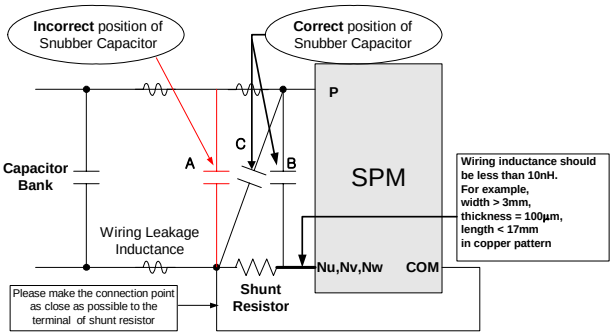


Figure 10. Recommended wiring of snubber cap.

And designers also considerate of DC-link Capacitors position. The Section 2.4 will describe the mutual relation with CE-capacitor of DC-link and snubber capacitor in detail.

2.3. PCB design guidance for PFC

We have almost finished the PCB design for SPM. The layout of PCB for PFC has to begin from here. Figure(11) is shown in application circuit for **PFCM**. In case of PFC, important factors of PFC pattern makes the same electric-potential for switching, detecting the current and deciding snubber location. When we design the SPM, it was already connecting with signal and power ground. Therefore, PFCM never connect the signal ground with power ground on the layout of PFC. The designers just considerate of detecting current and snubber location.

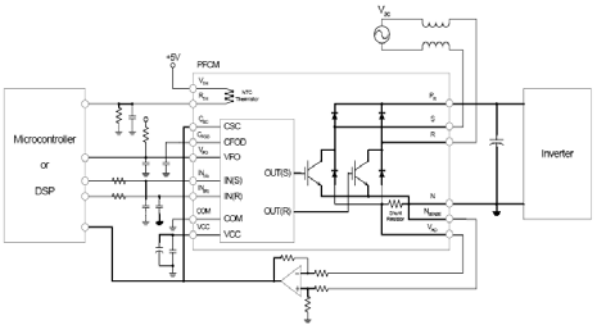


Figure 11. The application circuit for PFC-SPM

When we measure the current in the PFC, it is not easy to avoid the ground noise of PFC because the layout of PFC does not connect with signal and power ground. But, we are possible to remove the noise using differential amplifier because detected noise is common mode noise. Figure(12) is shown in how to detect the current for PFCM. In here, Nsens(22) pin of PFCM is Power ground including common mode noise. Therefore, OP-amp inputs directly connect with 21 and 22 pins of PFCM without another pass or pattern share.

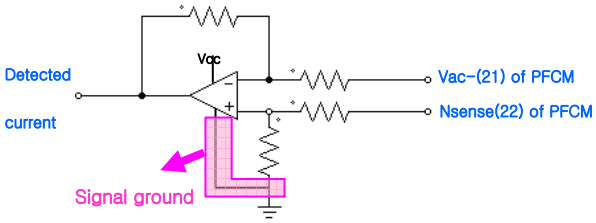


Figure 12. How to detect the current for PFCM

Lastly, the snubber location is very similar with SPM. Snubber capacitor has to install the same method as a SPM.