A Unique Four Quadrant Flyback Converter

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ABSTRACT

The flyback converter can be modified to provide 4-quadrant operation with additional switches and windings. This topology presents certain advantages over the full-bridge class-D amplifiers for low frequency high voltage output signal generation required for low power UPS systems, ring generators and audio amplifiers. This paper presents a detailed operational analysis of a versatile ring signal generator using the flyback topology.

INTRODUCTION

Power conversion requirements for DC/AC inverters or switch-mode amplifiers differ significantly from the conventional AC/DC or DC/DC power supplies. This class of converters requires a true 4-quadrant operation where the output voltage and current polarities can have any of the four possible combinations. Many low power inverter implementations involve linear amplifiers, as they provide simple and effective means of achieving the AC outputs. However, linear amplifiers suffer from high power losses and low efficiency operation.

Conventional switching power converters can be modified to satisfy the requirements for bi-directional power flow and bipolar outputs. A synchronous buck converter, for example, can function as a boost converter in reverse direction and provides two quadrant operation. It is, however, restricted to a single output polarity. When the buck concept is extended to the full-bridge converter, full four quadrant operation is feasible. Again, the power return mode is boost equivalent. With the full-bridge switching amplifier, the output voltage can be controlled to any level(s) between the rail voltages. However, as with most other buck derived converters, the output voltage can not exceed the input voltage. The complexity of this approach is high as it requires four switches and floating drive circuits. It also requires LC filtering on both legs of the bridge to filter out the high frequency component.

There is a wide range of applications which require a compact, high efficiency solution for generating high amplitude, low frequency AC output. These applications include high power audio amplifiers, small UPS systems, motor drives, laboratory AC sources and telephone ring generators. Both the linear and the full-bridge switching converter approaches require high rail voltages for operation. A front-end power supply that generates the high rail voltages from a conventional input voltage (e.g. -48V for telecom circuits) and provides safety isolation is almost always required with these implementations. The high rail voltages contribute to the switching stresses and limit the flexibility. The four quadrant flyback converter [1] provides an ideal, single stage solution for the applications mentioned above.

FOUR QUADRANT FLYBACK CONVERTER

Figure 1 shows the power stage diagram of the four quadrant flyback converter. The conventional flyback converter is modified to include additional secondary and primary windings and extra steering switches in the secondary. The extra secondary winding enables the dual output voltage polarity. The winding turns are normalized with respect to the secondary winding in series with D2 and Q2 having a single turn. In practice, N1, N2 and N3 are turns ratios from the respective windings to the number of turns of the secondary winding in series with D2, Q2. The switches Q2 and Q3 serve a dual purpose. In forward power transfer mode (input to output), they act as synchronous rectifiers to steer the current. When the reverse power is required, one of these switches is pulse width modulated to direct the energy from output into the flyback transformer/inductor. The stored energy is returned to the source through the extra primary winding and diode D1.

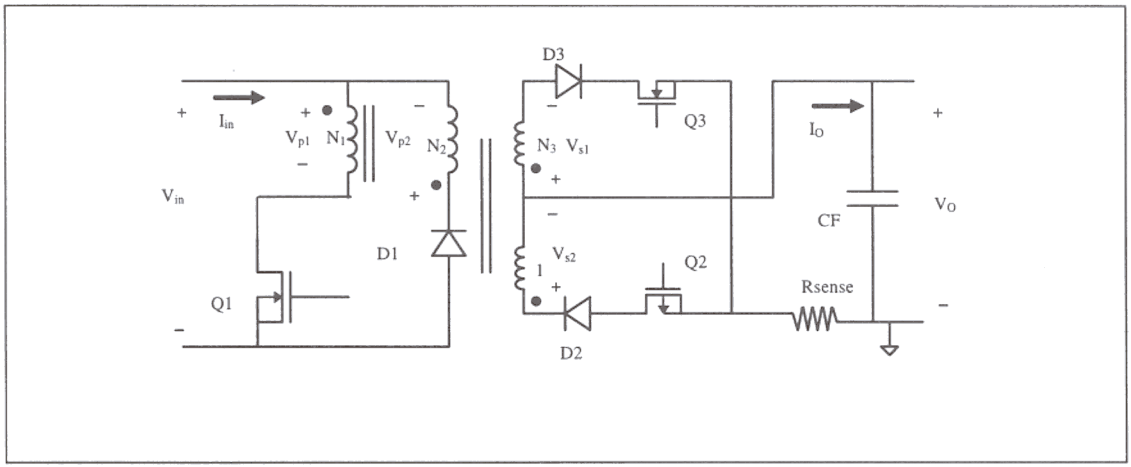


Figure 1. Four Quadrant Flyback Converter Topology

With these modifications, the circuit shown in Figure 1 offers all the benefits of the flyback converter to the DC/AC inverters. These include ease of implementation (only a single magnetic structure), isolation and voltage scaling ability. Compared to the multi-stage power conversion approaches described above, the flyback solution provides simplicity and higher conversion efficiency. The inherent characteristic of the flyback converter is that the input to output voltage ratio has no restrictions. It is also interesting to note that the converter in Figure 1 still operates as a flyback converter in the reverse power transfer mode.

Table I summarizes the four operating modes of the power converter and Figure 2 depicts the relationship of the output voltage and current for each mode. Figure 2 is drawn for a purely reactive load where there is a 90° phase difference between the output voltage and current for clear depiction of modes. If the load is purely resistive, the two waveforms will be in phase and the converter will only operate in modes 1 and 3. Most real load conditions will fall between pure resistive and pure reactive and will involve all 4 modes of operation. It is also likely that sudden load or line variations force the control loop to change modes even when the reference voltage is not crossing mode boundaries.

It can be clearly seen that Mode 1 is essentially identical to the conventional DC-DC flyback converter with the exception that the reference and the output voltages are constantly changing (increasing). Another minor but significant variation is that the output rectifier needs to be turned on by turning Q2 on after the modulating switch (Q1) has been turned off. Without turning Q2 on, the power transfer to the output is not possible. In this mode, Q3 has to be kept off to prevent any cross conduction at the output. In mode 2, when the power is being returned to the input, Q3 is PWMed and the other two switches are held off. The rectification (or flyback mode) is accomplished through D1 when Q3 is turned off. While mode 2 acts as an inverted flyback mode, the con-

Mode	Output Current	Output Voltage	Power Flow	E.A. output	Source (PWM) Switch	Rectifier Switch
1	+	+	+	-	Q1	Q2
2	-	+	-	+	Q3	(D1)
3	-	-	+	+	Q1	Q3
4	+	-	-	-	Q2	(D1)

Table I. Operating Mode determination for sinusoidal signal

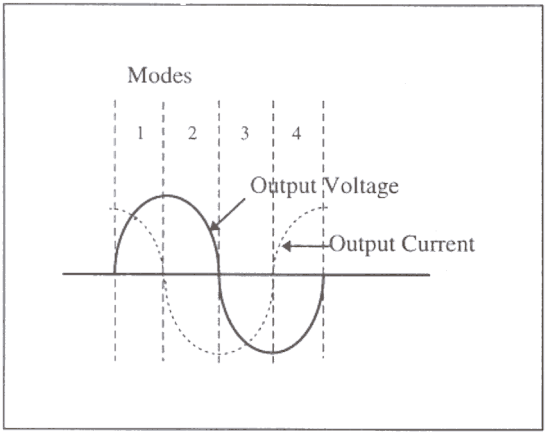


Figure 2. Operating Modes

trolled variable is still the output voltage and the feedback control has to accommodate this mode of operation. It can be easily shown that modes 3 and 4 are symmetrical to the first 2 modes with the output polarity reversed. For the sake of clarity, the PWM and rectifier sub-modes within each mode are graphically depicted in Figures 3a - 3h. The active sections of the circuit during each mode are highlighted and the critical node voltages are shown.

The flyback converter can operate in continuous conduction mode (CCM) or discontinuous conduction mode (DCM). The trade-offs between these operating modes have been well documented [2]. In CCM, the peak current is lower, but compensation is harder to design due to the presence of a RHP zero. For many low power applications, the higher peak current of DCM operation is an acceptable penalty to pay for the overall simplicity of implementation. Since the four quadrant flyback is primarily aimed at the low power applications, DCM operation is assumed for the remainder of this paper. In the DCM mode, the input to output voltage relationship is given by:

$$Vo = Vin * D * \sqrt{\frac{R_o * T_s}{2 * L_p}} \qquad (1)$$

As seen from (1), the output voltage is dependent on input voltage (Vin), PWM switch duty cycle (D), load resistance (Ro), transformer magnetizing inductance (Lp) and switching period (Ts). Like any power converter, the duty cycle is varied to accommodate changes in the input voltage or load conditions. Furthermore, the duty cycle needs to be varied to change the output voltage with the slowly varying reference voltage.

As with any switch-mode amplifier or inverter, the switching frequency has to be much higher than the output waveform frequency. In fact, the unity gain crossover frequency of the switching amplifier has to be higher than the maximum required output frequency. From the switching converter design point of view, this difference in frequencies allows the amplifier to be treated in the same manner as a DC-DC switching converter because the input or output voltages do not change over a period of several switching cycles. However, the converter must be designed for the peak power required by the output and that can be much higher than the average or RMS value of the output power.

RING GENERATOR REQUIREMENTS

As a vehicle for describing the four quadrant flyback converter, a ring generator application is chosen. The telephone ring signal has to be an accurate low frequency, high amplitude sinusoidal signal. Typical North American bells require a >45V, 20Hz (+/- 1 Hz) signal for ringing. In other national phone systems, the ring frequency is different, but the amplitude requirements are similar. With the decentralization of telecom function generation and the emergence of distributed networks such as Fiber-to-the-curb (FTTC) and Wireless Local Loop, the ring generation has moved away from the central office and closer to subscriber premises. With that comes the need for lower power capacity per ring

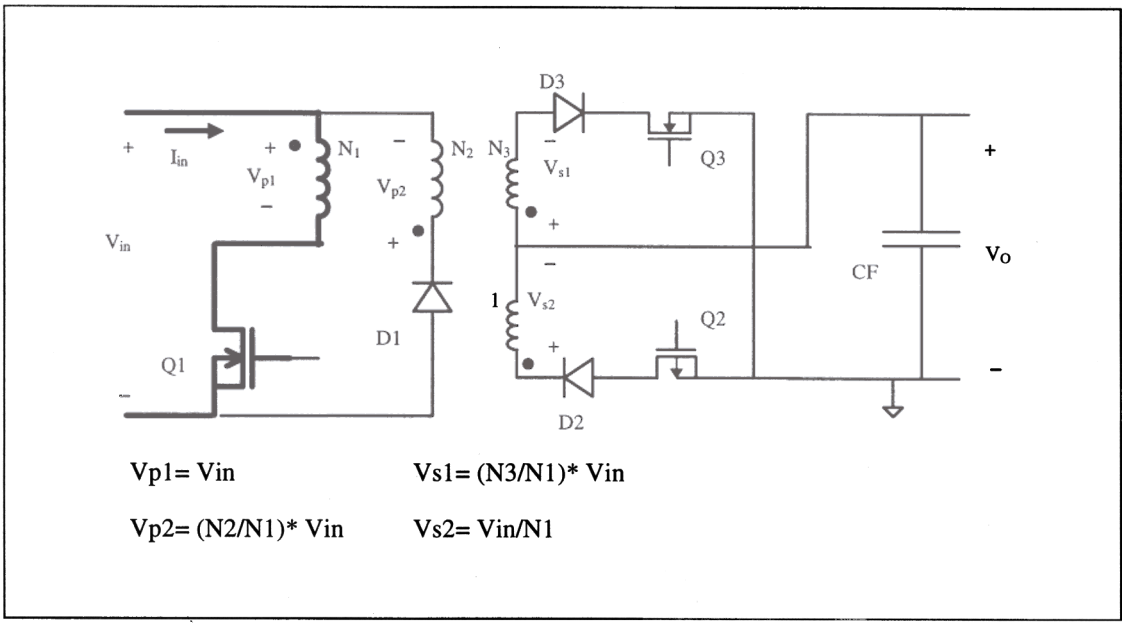


Figure 3a. Mode 1A - Forward Power Transfer (Positive Vo) - PWM Interval

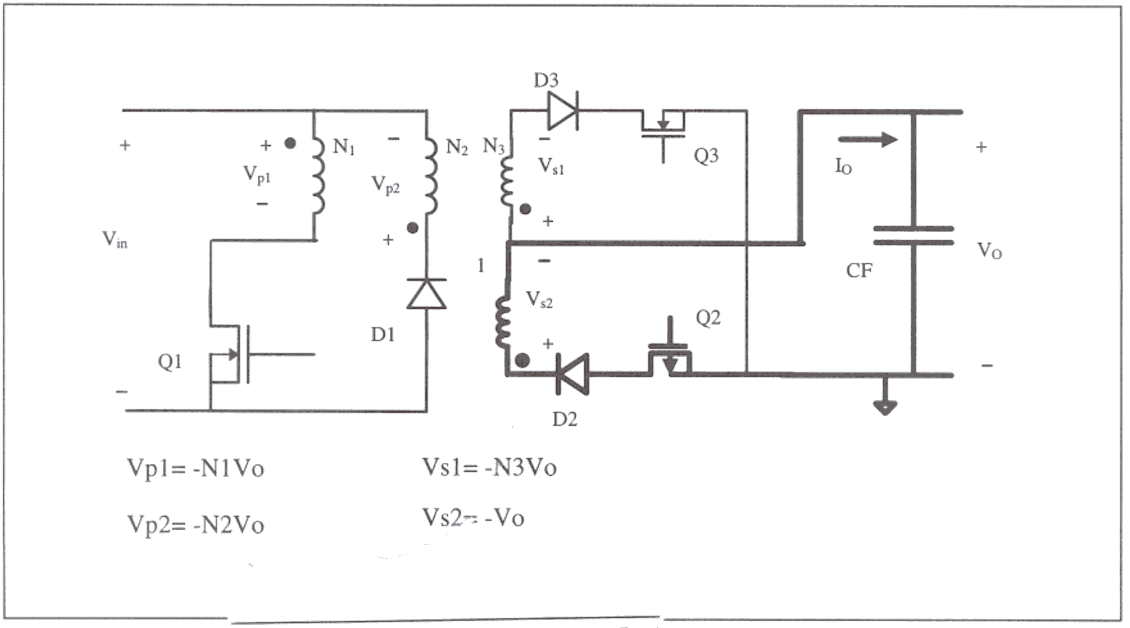
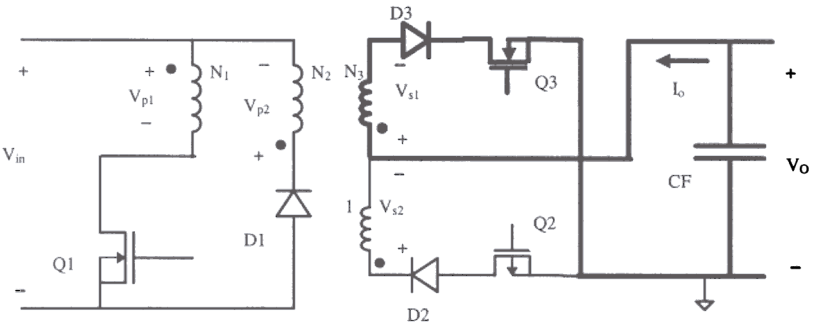


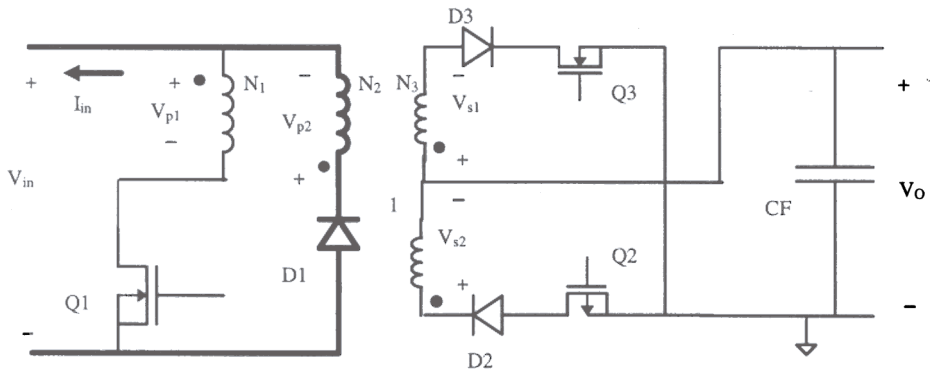
Figure 3b. Mode 1B - Forward Power Transfer (Positive Vo) - Rectification Interval



Vp1= (N1/N3)*Vo Vs1= Vo

Vp2= (N2/N3)* Vo Vs2= Vo/N3

Figure 3c. Mode 2A - Reverse Power Transfer (Positive Vo) - PWM Interval



Vp1= -(N1/N2)*Vin Vs1= -(N3/N2)*Vin

Vp2= -Vin Vs2= -Vin/N2

Figure 3d. Mode 2B - Reserve Power Transfer (Positive VO) - Rectification Interval

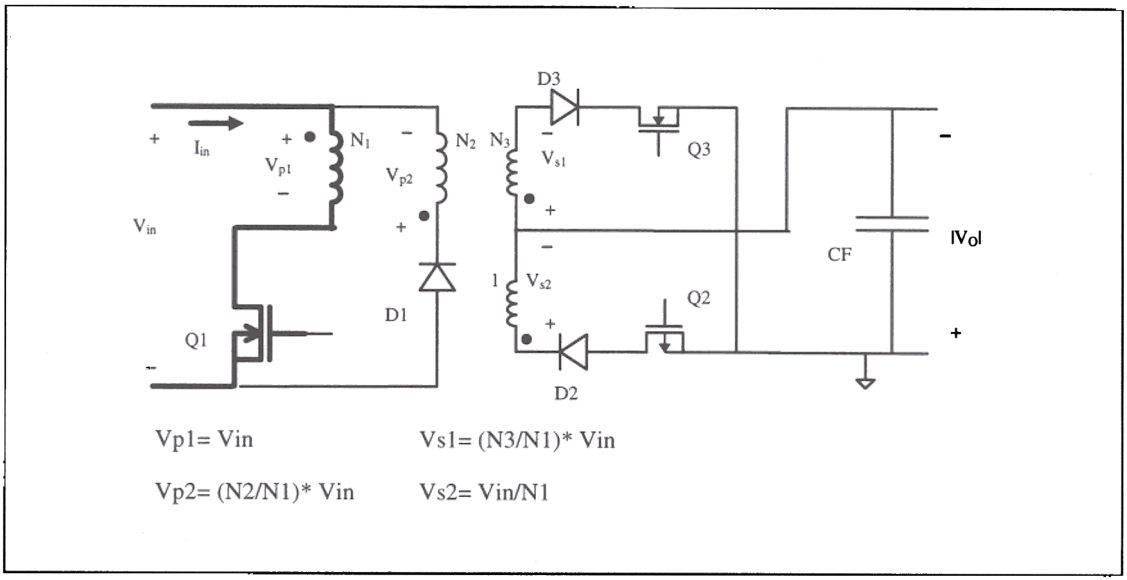


Figure 3e. Mode 3A - Forward Power Transfer (Negative Vo) - PWM Interval

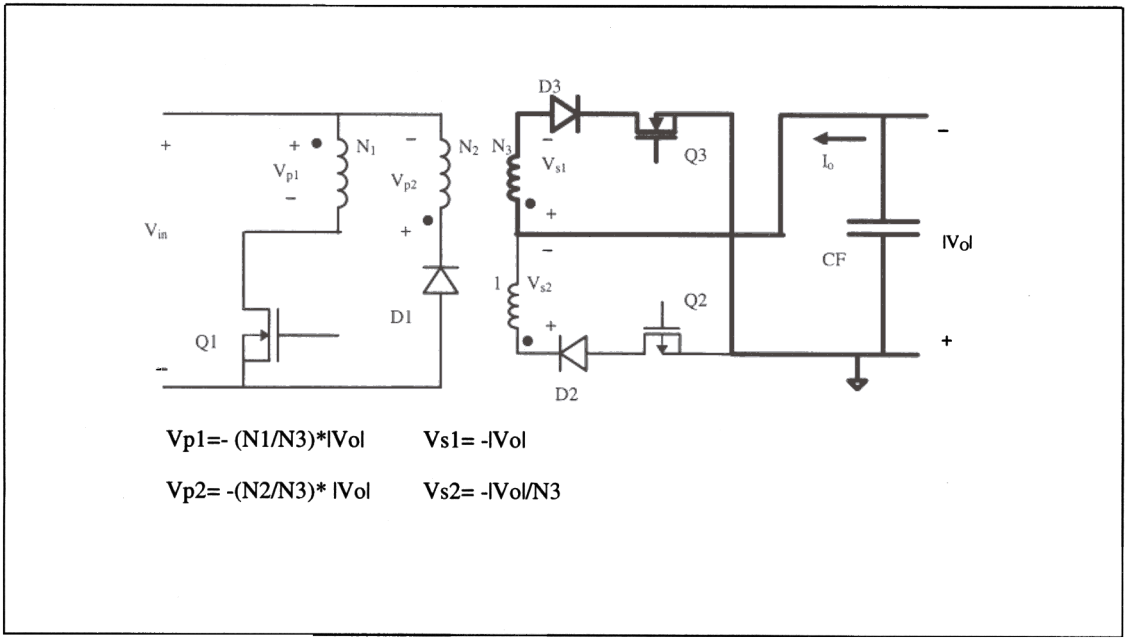


Figure 3f. Mode 3B - Forward Power Transfer (Negative Vo) -Rectifying Interval

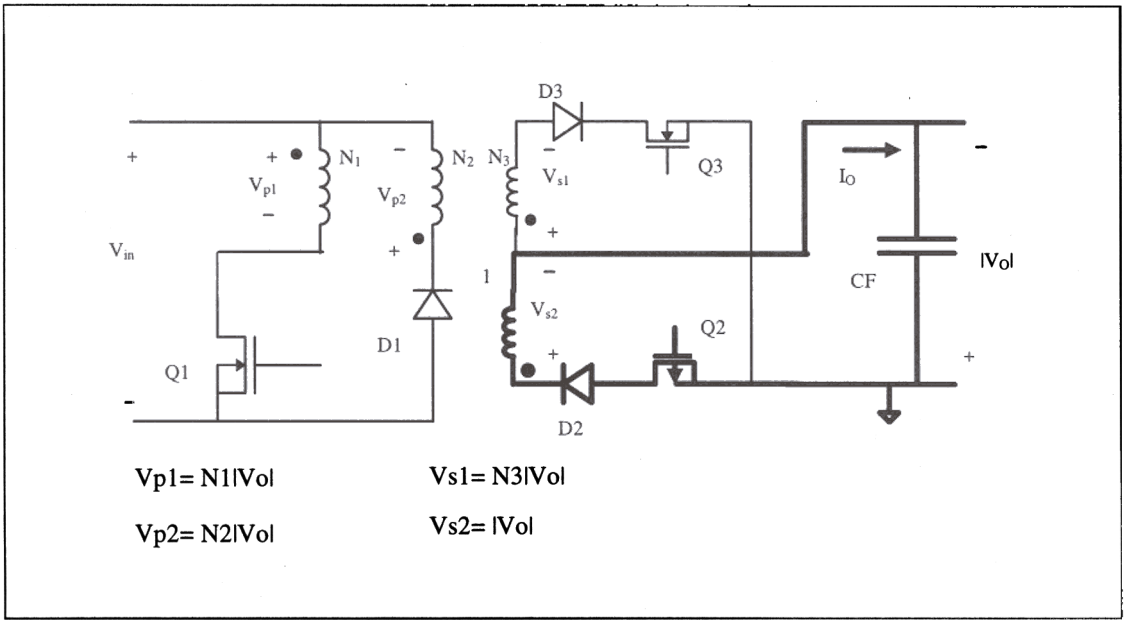


Figure 3g. Mode 4A - Reverse Power Transfer (Negative Vo) - PWM Interval

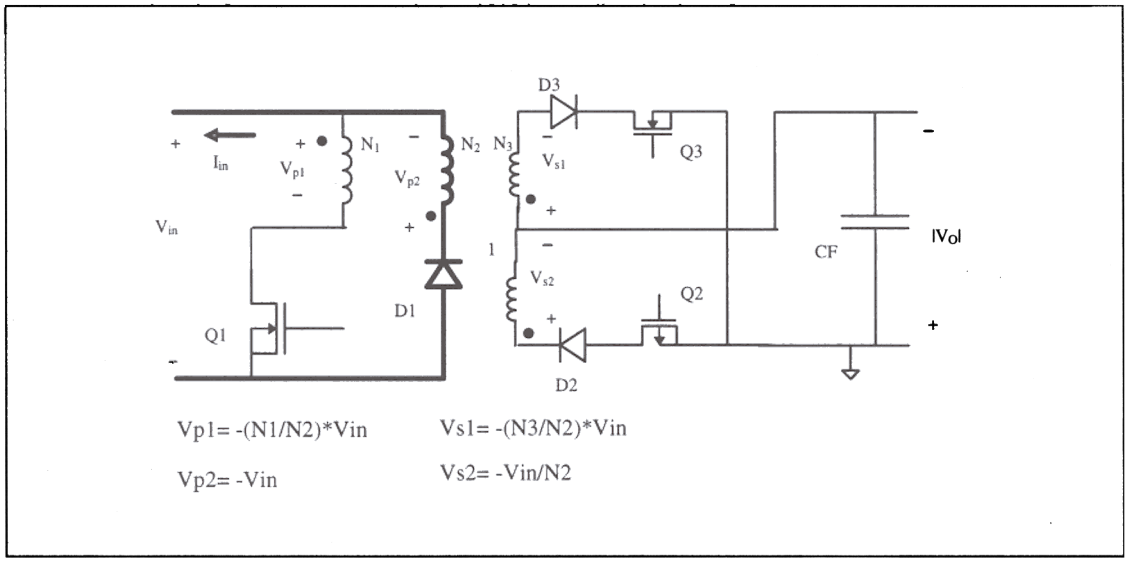


Figure 3h. Mode 4B - Reserve Power Transfer (Negative (VO) - Rectification Interval

generator and demand for higher efficiencies and cost effectiveness. In considering these requirements, the four quadrant flyback topology provides a very good solution.

The equivalent impedance of a single mechanical bell is 6930 ohms in series with 8 uF. This impedance is considered 1 Ringer Equivalent Number (REN). For a ring generator designed to ring n phones simultaneously, the equivalent load is given by n REN (6930/n ohms in series with 8n uF). In addition to this load, equivalent values of parasitic resistance and parasitic inductance of the distribution path have to be considered. For a 85V ring signal, the power equivalent of 1 REN is 1W. In the central office ring generators, a relatively lower power capacity ring generator could be designed to support many phones due to the statistical improbability of ringing all the phones simultaneously. On the other hand, the ringing voltage needs to be higher due to longer distances and higher drops along the distribution network. For the distributed approach of ring generation, the issues are different. With fewer phone lines per ring generator, statistical averaging to lower the peak power capability is no longer possible. However, the distribution drops are lower and hence a lower amplitude ring signal from the ring generator is acceptable.

The high voltage ring signal is usually superimposed on a DC pedestal voltage when applied to the phone. In some applications, the ring generator output is a floating AC waveform that is stacked on the DC output. In many other instances, the ring generator output has both the AC and the DC signals combined and it is directly connected to the phone that needs ringing. The ring generator has to be designed with these variations in mind. In addition to providing the high amplitude ring signal, the ring generator has to provide interfacing signals so that the ringing signal can be correctly applied to the desired phone line(s). The zero crossing signal allows an external relay to be switched without any voltage across it when the phone goes off hook. Before the relay switches, the ring generator has to support a significantly higher current presented by the off-hook condition of the phone. This condition could last for up to 200 ms. In some systems, this condition is handled by attenuating the AC signal. The converter also has to provide protection against a short circuit condition.

FOUR QUADRANT FLYBACK DESIGN CONSIDERATIONS

The modifications applied to the flyback converter to make it operational for four quadrants impose certain design restrictions which are discussed here.

The presence of Q2 and Q3 implies that the output rectifier conduction is not automatic when the primary switch is turned off. Either Q2 or Q3 (depending on the output polarity) is required to be turned on in the rectifier mode as soon as Q1 is turned off for the energy to transfer to the output. If this is not done, the power is returned to the input through D1. One option is to keep the appropriate switch (Q2 or Q3) continuously on in modes 1 and 3. The switch will conduct only when its associated series rectifier (D2 or D3) is forward biased by turn-off of Q1. While this is feasible with the circuit shown in Figure 1, it is impractical in many applications, where an n-channel MOSFET is used for Q2 instead of the p-channel device shown in Figure 1. Functionally, the n-channel device gives lower Rds-on performance over the p-channel counterpart for the same voltage rating and die size. The availability of n-channel devices is also much wider, especially at the high voltage ratings typically required for ring generator applications. The only drawback of using the n-channel device for Q2 is that it requires a floating drive circuit since its source will not be ground referenced, as illustrated in Figure 4. This drive can be designed using gate drive circuits commonly used for bridge type switching applications. However, it is not possible to keep Q2 continuously on because it may lead to saturation of the gate drive transformer. The choice of using an n-channel or p-channel device for Q2 will vary depending on the application requirements. For the purpose of this paper, a p-channel device is used in order to maintain simple drive circuit.

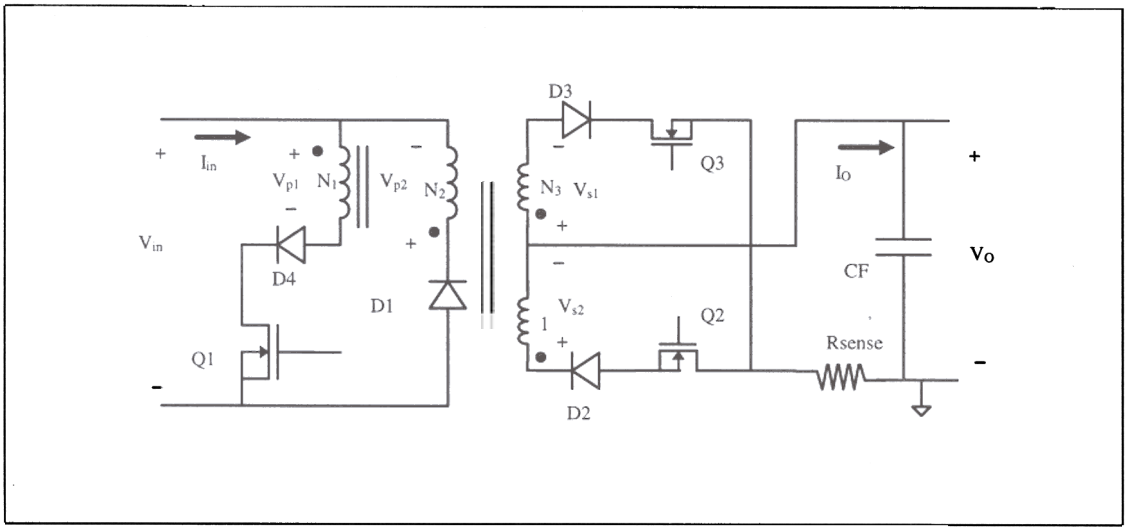


Figure 4. Four Quadrant Flyback Converter Topology - Possible Modifications (Q2, DR4)

A more appropriate way to ensure that the appropriate rectifying switch turns on is to use leading edge modulation with Q1. With this method, the drive signal for the modulating switch is always turned off with the clock pulse and the turn-on of the rectifying switch can be easily synchronized to the clock pulse. Figure 5 shows the typical timing waveforms illustrating the leading edge modulation and synchronized rectification scheme. As shown in Figure 5, a triangular ramp can be used to ensure that the maximum duty cycle is limited to 50% and a full 50% of the switching period is available for resetting the core. This is critical when the output voltage is near zero as the reset interval needs to be much longer than the on period of the primary switch.

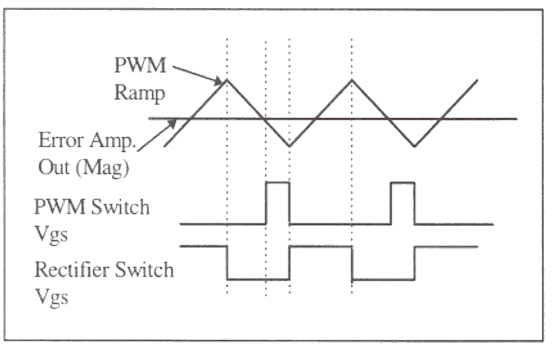


Figure 5. PWM Timing Waveforms

Transformer Design

The design of the four quadrant flyback transformer is much more involved due to the presence of additional windings and the required trade-offs for different operating modes. A good transformer design can help minimize voltage stresses, ensure DCM operation under all conditions and limit distortion in the output waveform under the severest of load conditions.

If the output voltage of the inverter is symmetrical (AC only), the two secondary windings should have identical turns. On the other hand, if the output voltage has a DC offset (typically -48V), the maximum output voltage will be much higher in one direction (negative) compared to the other. In this case, the turns ratio of the secondary windings should reflect the asymmetry in the output. The turns ratio N3 should be selected so that:

$$N_3 = \frac{V_o(pk-)}{V_o(pk+)} \qquad (2)$$

The primary to secondary turns ratios are constrained by two factors. The ratio N2 from auxiliary primary winding to the secondary S2 should be such that D1 does not conduct before D2 and D3 are forward biased in modes 1 and 3 respectively (Figures 3b, 3f). This constraint (shown in equation 3) places an upper bound on N2. N2 should be chosen to be as

high as possible within this constraint. A lower value of N2 will lead to higher voltage stress on Q1, Q2 and Q3, while reducing the stress on D1.

$$N_2 \le \frac{V_{in}(\min)}{V_o(pk+)} \tag{3}$$

When Q3 and Q2 are being PWMed, in modes 2 and 4 respectively, the voltage across drain-to-source of Q1 can go negative (Figures 3c, 3g) and force the body diode of Q1 to turn on. This undesirable situation can be prevented if N1 meets the following conditions:

$$N_1 \le \frac{V_{in}(\min)}{V_o(pk-)} \tag{4a}$$

and

$$N_1 \le N_3 * \frac{V_{in}(\min)}{V_o(pk+)} \tag{4b}$$

Depending on the value of N3, only one of the conditions (4a) and (4b) has to be met and the other condition is automatically satisfied. If N3 is greater than 1, indicating negative offset, (4a) is the dominating constraint. The value of N1 should be chosen as high as possible within this constraint. A lower value of N1 will lead to higher voltage stress on D1-D3 while reducing the stress on Q1.

As an alternative to meeting the constraints imposed by (4), a series diode D4 can be inserted in series with Q1(as shown in Figure 4) to prevent the body diode of Q1 from conducting in modes 2 and 4. In this case, there is no upper limit on N1. A higher value of N1 also helps core reset at lower output voltages.

The voltage stresses on the switching devices vary depending on the mode of operation and the output and input voltage levels. It is a simple exercise to identify voltage stress across each device in each mode and from there, the worst case voltage stresses can be extracted. These values are listed in Table II.

The other critical transformer design parameter is the magnetizing inductance. The maximum inductance for the conventional flyback converter to ensure DCM operation can be derived using equation (1). However, there are additional constraints for the four quadrant flyback converter. The first constraint is based on the core reset requirement. With the reset interval limited to 50% of the switching period as shown in Figure 5, the reset has to be completed in this interval for all output voltage levels.

The positive flux swing during modes 1 and 3 (Figures 3a, 3e) is given by:

$$\Delta\phi(+) = \frac{V_{in} * D * T_s}{N_1} \tag{5}$$

Substituting from equation (1), the flux swing becomes:

$$\Delta\phi(+) = \frac{V_o}{N_1} * \sqrt{\frac{2 * L_p * T_s}{R_o}} \tag{6}$$

The maximum possible negative flux swing is given by equations (7a) and (7b) for modes 1 and 3 respectively.

$$\Delta\phi(-)[\max] = V_o * 0.5 * T_s$$

or

$$\Delta\phi(-)[\max] = \frac{V_o * 0.5 * T_s}{N_3}$$

To ensure core reset every cycle, the positive

Device	Voltage Stress	Device	Voltage Stress
Q1	$(1+N_1/N_2)V_{in}(\max)$	D1	$(1+N_2/N_1)V_{in}(\max)$
Q2	$-V_o(pk-) - V_{in}(\max)/N_2$	D2	$V_o(pk+) + V_{in}(\max)/N_1$
Q3	$V_o(pk+) + N_3/N_2 * V_{in}(\max)$	D3	$\lvert V_o\rvert(pk-) + N_3/N_1 * V_{in}(\max)$

Table II. Voltage Stresses on Switching Devices

flux swing should always be lower than the maximum available negative flux swing. For N3 ≥ 1, equation 7(b) results in lower maximum negative flux swing. Thus,

$$\frac{V_o * 0.5 * T_s}{N_3} \geq \frac{V_o}{N_1} * \sqrt{\frac{2 * L_p * T_s}{R_o}} \quad (8)$$

Simplifying this results in:

$$L_p \leq (\frac{N_1}{N_3})^2 * \frac{R_o * T_s}{8} \quad (9)$$

The primary magnetizing inductance must meet this condition to ensure proper operation in modes 1 and 3. If the condition in equation (9) is not met, the converter may transition to CCM operation and eventually saturate the core if the condition persists for a number of switching cycles. The peak primary current is given by:

$$I_p(pk) = V_o(pk) * \sqrt{\frac{2 * T_s}{R_o * L_p}} \quad (10)$$

The rest of the transformer design can be completed using conventional methods for selecting core size, number of primary turns, flux excursion etc. The peak primary current determines the wire size in the main primary winding as well as the wire sizes of the 2 secondary windings. The wire size of the other primary winding can be much smaller and is determined by the peak reverse power being transferred. The peak and RMS current ratings of the switches can also be determined from (10) and the turns ratio information. These are used along with the voltage rating requirements from Table II to select the switching devices for the converter.

Reverse Power Transfer Modes (Modes 2 and 4)

The flyback converter operation in reverse modes, when either Q2 or Q3 is being pulse width modulated, is somewhat different from the operation in forward power transfer modes. In these modes, Vo acts as the input voltage to the converter and determines the amount of energy stored in the flyback inductor during the switch on time. Since this energy is transferred every switching cycle to the input, Vo sets the limit on the rate of energy transfer or power that can be transferred back during these modes. The peak current during modes 2 and 4 is given by:

$$I_s = \frac{|V_o| * D * T_s}{L_s} \quad (11)$$

where D is the duty cycle for Q2 or Q3, |Vo| is the magnitude of instantaneous output voltage and Ls is the magnetizing inductance of the associated secondary winding. Equating the rate of energy storage to the required rate of transfer, we get -

$$0.5 * L_s * I_s^2 = |P_o| * T_s = |V_o| * |I_o| * T_s \quad (12)$$

Substituting from (11) and simplifying results in

$$D^2 = \frac{2 * L_s}{T_s} * \frac{|I_o|}{|V_o|} \quad (13)$$

With the reactive load present in many switching amplifiers (including the ring generator), the ratio of |Io| to |Vo| is a time varying quantity and can vary over a wide range. When this ratio is very high, e.g. when |Vo| is close to zero and |Io| is near its peak, the flyback converter duty cycle may not be able to meet the condition in (13). As a result, there may be some distortion in the output voltage waveform. In order to minimize this limit situation, the secondary magnetizing inductance, Ls, should be minimized. Since Ls and Lp are related by turns ratio, the conditions imposed by (9) and (13) will significantly influence the required primary and secondary inductances and the turns ratios.

CONTROL CIRCUIT CONSIDERATIONS

The control circuit required for the four quadrant flyback converter has to support all four modes of operation and has to be able to handle transitions from one mode to the other smoothly. While a discrete implementation is possible, the complexity of such an approach can be overwhelming due to the precision timing requirements and multiple functionalities required. The converter implementation can be greatly simplified by using Unitrode's source ringer controller IC - the UCC3750.

Figure 6 shows the internal block diagram of the UCC3750. As shown in Figure 6, the UCC3750 contains all the functional blocks required to control the four quadrant flyback converter. It is referenced to the secondary side of the converter to ease output current sensing and driving of switches Q2 and Q3. It operates from a 5V bias supply referenced to the secondary side that is normally available. The IC generates a higher (~13V) voltage at pin Vcp for driving the MOSFET gates using a charge pump. If the system has the higher voltage supply available also, it can be applied to Vcp and the charge pump can be disabled. Note that the 5V supply at the VDD input is still required. From VDD and VCP, the IC generates two reference voltages - an internal reference of 3V which serves as virtual ground for all the AC signal processing and a reference voltage of 7.5V which drives most of the internal circuitry. The 7.5V is brought out to a pin (REF) for bypassing.

The UCC3750 has a crystal derived low frequency sine-wave reference which is programmable and has low Total Harmonic Distortion(THD). With a 32kHz crystal, available sine-wave frequencies are 20Hz, 25Hz and 50Hz and can be selected with frequency select pins. With other crystals or with a square-wave clock signal applied across the XTAL1 and XTAL2 inputs, other frequencies can be derived. These frequencies are a fixed ratio of the applied frequency. The sine-wave reference output can also be tri-stated and an externally generated AC reference can be applied to the IC. With a filtering capacitor on the SINREF pin, the discrete steps in the sine-wave can be smoothed. The value of the capacitance on pin 9 should be less than 0.1 uF to prevent attenuation of the sine-wave signal. The amplitude of the sine-wave reference generated by UCC3750 is 1V p-p (riding on the internal 3V reference).

The sine-wave reference is buffered and applied to the error amplifier inputs for error voltage generation. The buffer stage can attenuate the AC signal if the AC current limit is indicated. The first amplifier functions as a summing amplifier for adding the reference and the required DC offset voltage. The output of this amplifier forms the actual reference against which the output voltage is compared. The amplifier output also serves as an input to the internal circuit, indicating when the output voltage polarity changes and the operating mode needs to be changed. The second amplifier functions as the voltage error amplifier, where the scaled output voltage is compared against the reference voltage and an

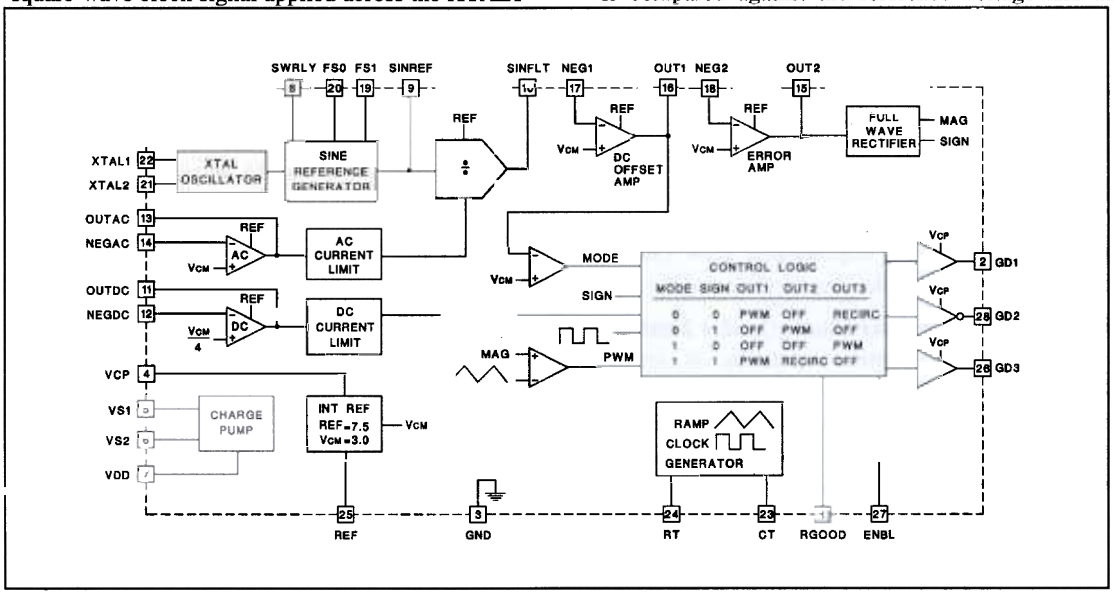


Figure 6. Block Diagram of the UCC3750

error signal is generated. The feedback compensation for loop stability is also applied in this stage. The error signal is further processed to separate its polarity and magnitude. An absolute value circuit (precision full-wave rectifier) is used to get the magnitude information. The error signal polarity and the reference signal polarity determine the operating mode of the circuit. The absolute value circuit provides phase inversion for modes 2 and 3 in order to maintain the correct polarity for loop gain. The output of the absolute value circuit is compared to the oscillator ramp for generation of the PWM output. The PWM output is directed to the appropriate output gate driver based on the mode determining circuit.

More details regarding the UCC3750 and its application are available from the datasheet of the IC [3].

CIRCUIT PERFORMANCE

A four quadrant flyback converter was designed using the UCC3750, applying the design considerations highlighted in this paper. It was designed for a 15 REN ring generator application with selectable ring frequency and programmable output voltage offset. The nominal output voltage is set at 85V RMS with no DC offset. The detailed circuit diagram is shown in Figure 7.

While most of the circuit elements shown in Figure 7 are self-explanatory, some circuit blocks need elaboration. One such circuit block is the configuration consisting of Q4-Q6 [4]. This block protects the switch Q1 from turning on inadvertently when it is meant to be off for modes 2 and 4. The UCC3750 outputs are controlled in such a manner that only one switch is commanded on at a time. However, based on the resonance between magnetizing inductance of the gate drive transformer (T2) and the coupling capacitance in the gate drive circuit, there may be a tendency to turn Q1 on even when GD1 output is low. This secondary side resonance can be damped by higher coupling capacitance. The resonance frequency can also be reduced by increasing the magnetizing inductance. However,

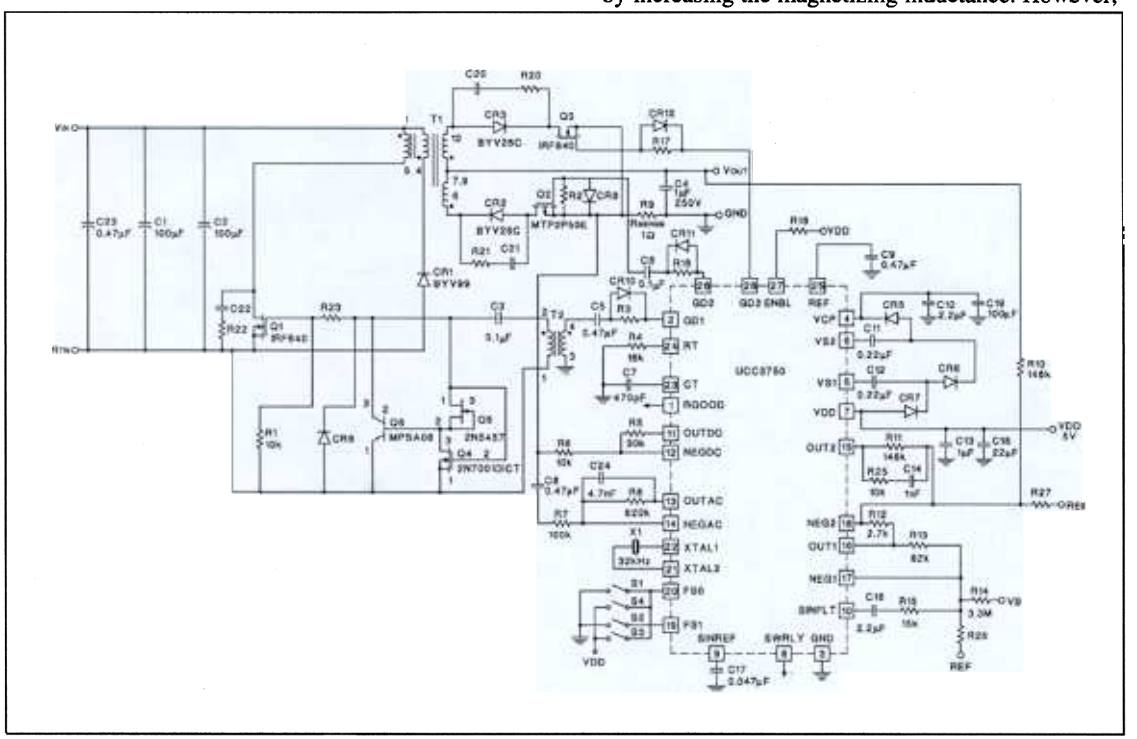


Figure 7. 15 REN Ring Generator using UCC3750

the circuit block shown in Figure 7 provides a reliable alternative method of clamping the resonance. If the resonance begins to take shape, the current source formed by Q5 turns Q6 on and prevents the untimely turn on of Q1. During normal operation, the pulse output of GD1 is fast enough to turn Q4 on and prevent turn-on of Q6.

Another circuit block that requires explanation is the AC current limiting block. C8 provides AC coupling of the sensed current into the AC limit amplifier. Using the AC limit amplifier, the sine-wave amplitude (coming out of SINFLT, pin 10) can be attenuated. This feature can be used to attain the output voltage attenuation when ringing multiple phones, allowing the ring generator to ride through off-hook conditions without causing excessive power to be delivered. However, with coupling capacitor C16, the attenuation of SINFLT amplitude causes temporary saturation of the error amplifier outputs and can cause excessive transient currents. Depending on the application requirements, it may be more appropriate to disable the AC limit functioning by setting R8 to zero ohms and using the DC limiting as the overall power limiting function of the ring generator.

The performance of the circuit in Figure 7 has been evaluated over different line and load conditions. The overall conversion efficiency is above 80% for full load operation. The measured THD of the output voltage under nominal load conditions is 4.25%. The output voltage and current waveforms for different load conditions are shown in Figures 8-11. As shown in Figure 8, the no load waveform is distortion free. With an equivalent of a 10 REN load (700 ohms, 70 uF), the output waveform (Figure 9) is still distortion free. With a more reactive load (33 uF, 700 ohms), the waveform gets some distortion in modes 2 and 4 due to inadequate duty cycle (failure to satisfy (13))(Figure 10). With the capacitance set to even a lower value (16.5 uF) the distortion increases as the circuit operates for a longer period in modes 2 and 4 (Figure 11).

Other Applications and Modifications

The discussion of the four quadrant flyback converter has been limited to the application of ring generators for the purpose of this paper. As mentioned before, the topology is also suitable for various other applications which require high efficiency DC-AC inversion. The major factors which influence the design of this form of switching inverters are the load characteristics for the application. These include output power level, voltage level, frequency, required response time and reactance. Each of these factors has an impact on applicability and effectiveness of the four quadrant flyback converter for that application.

For example, for audio amplifier applications, the output bandwidth has to be much higher to support higher signal frequencies. It may necessitate using a higher switching frequency and more involved loop compensation design than presented here. On the other hand, higher power applications (such as low power UPS), could benefit from a continuous conduction mode (CCM) operation of the flyback converter. Other possible modifications to the flyback converter are also feasible including a different control method such as average current control or minor topological modifications. These changes can help optimize the performance of the converter for a particular application, but need a more detailed evaluation than presented in this paper.

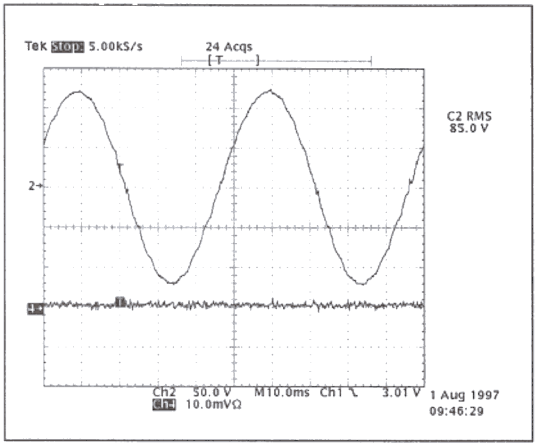


Figure 8. Output Waveforms with no load [Upper trace - Vo (50 V/div), Lower trace - Io (100 mA/div);

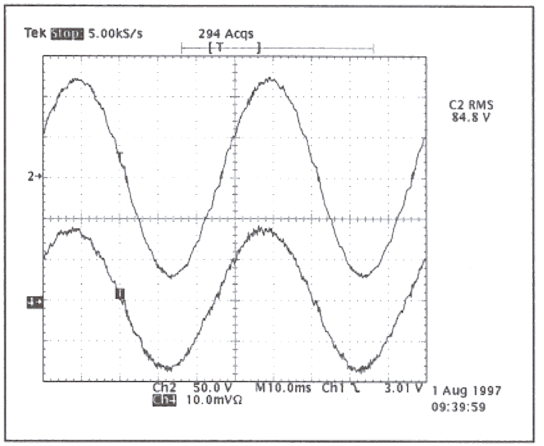


Figure 9. Output waveforms for 700Ω, 70uF load. [Upper trace - Vo (50 V/div), Lower trace - Io (100mA/div)]

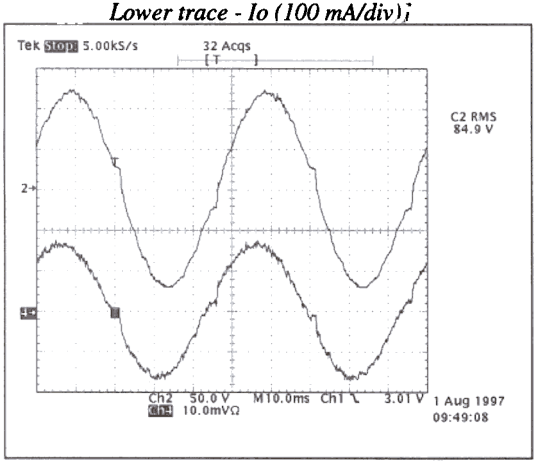


Figure 10. Output waveforms for 700Ω, 33uF load. [Upper trace - Vo (50V/div), Lower trace - Io (100 mA/div)]

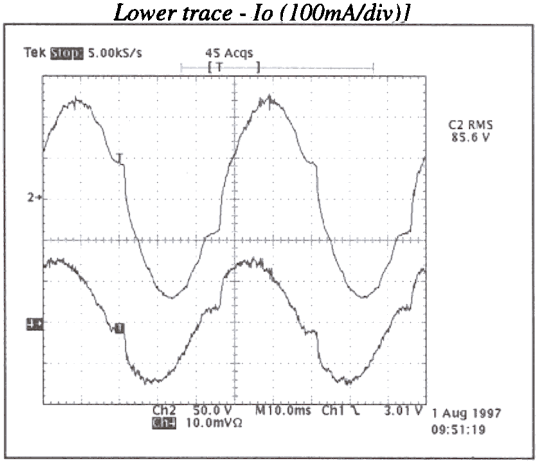


Figure 11. *Output waveforms for 700Ω, 16.5uF load. [Upper trace - Vo (50 V/div), Lower trace - Io (100mA/div)]*

CONCLUSIONS

The characteristics of a four quadrant flyback converter have been highlighted in this paper. The design criteria for meeting the operating requirements have been presented in detail. A switching inverter designed using these criteria for ring generator applications has been presented. Based on the results and operating requirements, the four quadrant flyback is shown to be a viable solution for low to medium power switching amplifier applications such as ring generators, UPS, audio amplifiers etc.

REFERENCES

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[2] L. H. Dixon, "*Switching Power Supply Topology Review*", Unitrode Seminar SEM 200 (Reprinted in many recent seminar books)

[3] UCC3750 Datasheet, Unitrode Product Data Handbook, 1997.

[4] Suggested by John Fletcher, Nortel.

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