The Effects of Leakage Inductance on Multi-Output Flyback Circuits

by Lloyd Dixon

TOPIC 2

THE EFFECTS OF LEAKAGE INDUCTANCE ON MULTI-OUTPUT FLYBACK CIRCUITS

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A similar topic dealing with buck-derived regulators was presented at previous Unitrode seminars (see Section P2). Leakage inductance is also the major cause of poor cross-regulation in flyback circuits, but the circuit analysis is quite different. This topic shows how to predict and minimize the effects of leakage inductance and wiring inductance in continuous and discontinuous mode flyback regulators.

Introduction: A typical flyback regulator circuit with two outputs is shown in Figure 1. The flyback "transformer" is actually an inductor with multiple windings. While the transistor switch is ON, the inductor draws increasing current from the input and stores this energy. During the ON time, the output rectifiers are reverse biased (note the polarity dots). When the transistor turns OFF, the inductor ampere-turns cannot instantaneously change. The voltages across all inductor windings reverse or "fly back" forcing the ampere-turns that were flowing in the primary to transfer to the secondary windings. The previously stored energy is then delivered to the outputs.

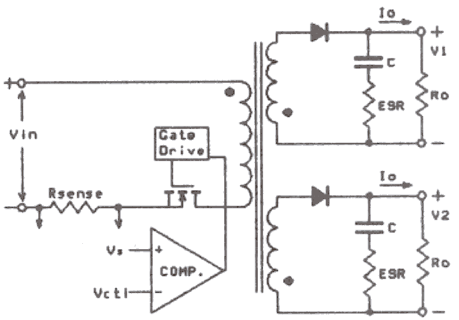

Figure 1 - FLYBACK CONVERTER

A flyback regulator may be operated in the continuous or discontinuous inductor current modes. Idealized current waveforms for the discontinuous mode (at full load) are shown in Figure 2a, which assumes a 1:1 turns ratio. By definition, the inductor current starts at zero at the beginning of each switching period. All of the energy stored during the ON time is delivered to the outputs and the current is back to zero before the end of each period. In the continuous mode shown in Figure 2b, the inductor current is never zero during normal operation, and the inductor holds much more energy than is taken from the input and delivered to the output each switching cycle.

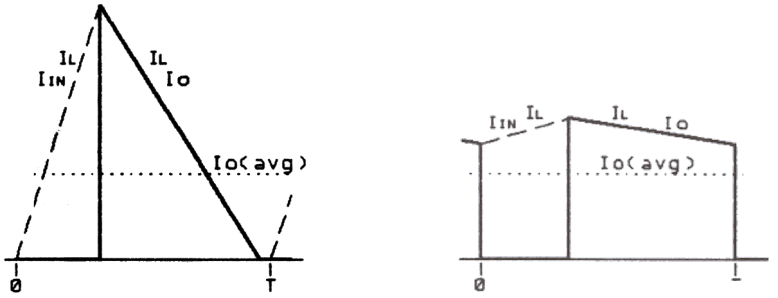

Figure 2 - Inductor Current Modes

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These two inductor current operating modes have radically different operating characteristics, with divergent opinions by experienced designers as to which mode is better. Note that for the same average output current (same power output), the discontinuous mode reaches nearly twice the peak current required in the continuous mode. However, as indicated by the relative inductor current slopes, the continuous mode typically employs 10 times the inductance value and requires $10/1.8^2 = 3$ times the inductor energy storage capability as the discontinuous mode.

Non-Ideal Aspects: All flyback circuits depend upon inductive energy storage. This is usually accomplished by introducing a small non-magnetic gap in series with the inductor core. Unfortunately, the inductor windings cannot all be equally well coupled to the energy storage gap because of the physical separation between the windings. Additional amounts of magnetic energy are also stored between and within the windings. These amounts of energy are represented in the circuit as leakage inductances.

When the transistor turns off, leakage inductance between transformer primary and secondaries will fight the transfer of current to the secondaries, causing a large voltage spike to occur across the transistor. This inductive spike must be clamped to a voltage level less than the transistor rating or the transistor will be destroyed. (Figure 1 does not show this necessary clamp.) There are many possible clamping methods -- with some, the energy put into the clamp is lost, hurting circuit efficiency, with other methods the clamp energy is conserved. The two-transistor 150 Watt Flyback Regulator Design Review (Section A3) saves this energy by returning it to the input.

Leakage inductance between secondaries, together with wiring inductances from each secondary to its respective filter capacitor, are the main cause of poor cross-regulation between the outputs.

Circuit diagrams such as Figure 1 seldom show these many parasitic inductive elements which play such an important role in flyback circuit performance. Circuit analysis becomes complex and confusing when all these elements are included, compounded by the differing turns ratios between the windings.

The Normalized Equivalent Circuit: Considerable simplification is possible as shown in the normalized equivalent circuit of Figure 3. In the normalized circuit, the actual circuit values associated with each winding have been translated according to the actual turns ratios into equivalent circuit values with 1:1 turns ratios. Since input-output isolation is not relevant to this analysis, the ideal 1:1 transformer may then be discarded and the windings directly interconnected. When the analysis is completed, the resulting values may be "de-normalized" to their actual values according to the turns ratios.

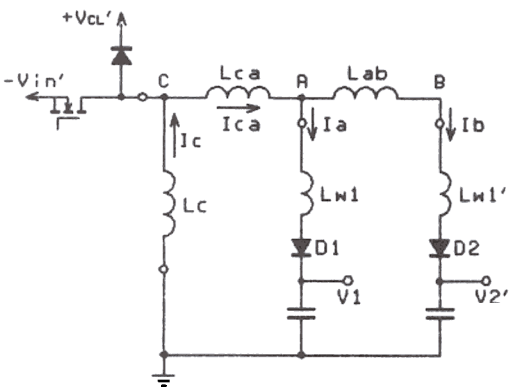

Figure 3 - Normalized Circuit

For example, assume an off-line regulator with a 30:1 turns ratio between primary and 5V secondary, and a 3:1 turns ratio between 15V secondary and the 5V secondary. Normalization may be with respect to any winding. In this case, all windings are normalized to the 5V winding by dividing each voltage and multiplying current by the actual turns ratio. Inductance and resistance are divided and capacitance multiplied by the turns ratio squared. Referred to the 5V secondary, a V_{in} of 300V divided by the turns ratio of 30 translates to V_{in}' of 10V. Primary inductance of 450µH divided by 30^2 becomes 0.5µH. The V2 of 15V at 4A secondary becomes V2' of 5V at 12A, etc.

The normalized circuit of Figure 3, mutual inductance L_C represents energy stored in the gap, L_{ca} represents leakage inductance between primary and secondary A, and L_{ab} is the leakage inductance between secondaries A and B. Mutual inductance L_C is connected directly to V_{in}' through the transistor or to V_{CL}' through the clamp diode, whereas outputs V1 and V2' are coupled to L_C through leakage inductances and secondary wiring inductances L_{w1} and L_{w2}. Primary wiring inductance is negligible because it is divided by 30^2. This Figure 3 configuration applies when the primary winding is closest to the gap -- either inside the secondaries with the centerleg gapped or outside the secondaries with the outer leg gapped. If the primary were on the other side of the secondaries opposite the gap, the equivalent circuit would have L_C connected to point B instead of point C.

To further simplify the analysis, output ripple voltages are assumed to be zero. The error caused by this assumption is small in a practical power supply and its effect nearly averages out over a complete switching period.

Energy Lost to the Clamp: The continuous mode waveforms of Figure 4 show two non-ideal occurrences, both caused by leakage and wiring inductances which fight the transfer of current from primary to secondary when the transistor switches on and off. The leakage inductances plus wiring inductances are normally a small fraction of the primary inductance L_C. Assuming V1 and V2' are substantially equal, the leakage and wiring inductances may be combined:

$$L_{ps} = L_{ca} + \frac{L_{w1}(L_{ab}+L_{w2}')}{L_{w1}+L_{ab}+L_{w2}'}$$

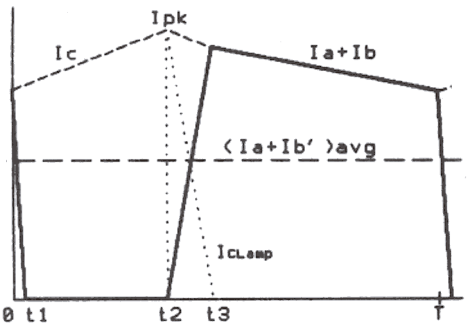

Figure 4 - Current Transfer

Immediately before the transistor turns on at t_0, inductor current I_C equals I_{ca} and flows through L_{ps} to the outputs. At t_0, the transistor pulls point C down to $-V_{in}'$. However, I_{ca} cannot instantaneously decrease, which prevents I_C from immediately transferring to the input. The time required for I_{ca} to reach zero and I_C transfer to be completed is (neglecting diode drops):

$$t_1 = (V_{in}'+V_1)/L_{ps}$$

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Some of the energy in L_{ps} when the transistor turns on transfers to L_c, the rest goes to the output - none is lost.

This turn-on transfer problem cannot occur in the discontinuous inductor current mode because I_{ca} is always zero before the transistor switches on.

A much more serious transfer delay occurs when the transistor switches off at time t_2. At t_2, inductor current Ic is at its maximum peak value, but current I_{ca} through L_{ps} is zero. The voltage across L_c reverses in an attempt to force I_c through L_{ps}. I_{ca} cannot change instantaneously, so L_c forces its current into the clamp. I_{ca} rises according to the voltage V_{CL}'-Vl across L_{ps}, and I_{CL}' decreases in a complementary manner as shown in Figure 4. The transfer time is:

$$t_3-t_2 = I_{c(pk)}\frac{L_{ps}}{V_{CL}'(1+L_{ps}/L_c)-V_1} \qquad (2)$$

With Vl = V2' = Vout, the energy transferred into the clamp is:

$$W_{clamp} = \frac{L_{ps}I_{pk}^2}{2} \cdot \frac{1}{1+L_{ps}/L_c-V1/V_{CL}'} \qquad (3)$$

This equation also applies to the discontinuous inductor current mode. It also may be used (with a small error) when the primary winding is opposite the gap, or when the primary is split and interleaved on both sides of the secondaries. (Interleaving will reduce L_{ca} by a factor of 3 and accordingly reduce the energy lost to the clamp.)

The energy diverted from the output to the clamp hurts open loop load regulation, but this is not very significant because the closed loop feedback easily corrects for this. But in order to maintain reasonable efficiency in flyback supplies of more than a few Watts output this energy must be recovered in some way rather than allow it to be dissipated. The two-transistor circuit shown in Section A3 accomplishes this quite easily with a pair of cross-connected diodes which return the energy to the Vin source. Single transistor flyback circuits usually employ a single diode with an added winding bifilar with the primary. Even when the clamp energy is conserved, it should be minimized because it increases the current in the transistor and the energy storage requirement of the flyback transformer.

As equation (3) reveals, the energy delivered to the clamp equals the energy stored in the primary-secondary leakage inductance, L_{ps}, <u>increased</u> by the fraction on the right whose denominator is usually considerably less than 1. The L_{ps}/L_c term is almost negligible, but $V1/V_{CL}'$ is 0.5 when the clamp voltage is twice Vl (as in the example used). In this case, the energy sent to the clamp is <u>twice</u> the energy stored in L_{ps}. In order to minimize the energy diverted to the clamp, it is important to (1) minimize L_{ps} which consists of leakage inductances and wiring inductances, (2) make the clamp voltage V_{CL}' as large as possible compared to Vl (but this will increase the transistor V_{CE} requirements).

Table I shows that in the same application -- 100 W, 100 kHz -- the continuous mode circuit puts only 8.48 Watts into the clamp vs. 15.99 Watts

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for the continuous mode. Even though Ipk in the discontinuous mode is almost twice as large, primary-secondary inductance L_{ps} is 6 times smaller which gives the advantage to the discontinuous mode. The L_{ps} would be even smaller fovoring the discontinuous mode even more but the wiring inductance which is the same in both circuits is a much more significant portion of the discontinuous mode L_{ps}.

Cross-Regulation in the Continuous Mode:

Figure 5 shows the secondary current waveforms of the two-output flyback circuit of Fig. 3 operated in the continuous inductor current mode and with equal normalized output voltages (V1 = V2'). L_c+L_{ca} together force current I_c into both outputs. The division of this current between the two outputs is determined by the inductances L_{w1} and L_{ab}+L_{w2}'in series with the outputs.

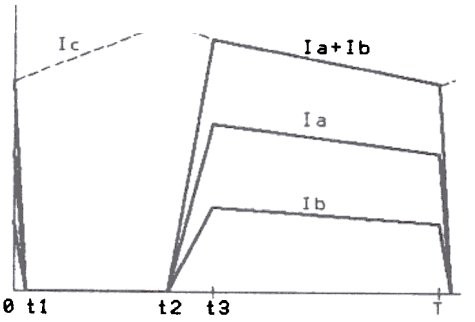

Figure 5 - Two Outputs, V1 = V2'

Let output #1 inductance L1 = L_{w1}, and output #2 inductance L2 = L_{ab}+L_{w2}'.
At the beginning of the off time, point C is at Vclamp. The voltages across L1 and L2 are equal. At the beginning of the OFF time (t_3), peak I_c divides into I_a and I_b:

$$I_a = \frac{I_c \cdot L2}{L1+L2} \; ; \qquad I_b = \frac{I_c \cdot L1}{L1+L2} \tag{4}$$

Let L_t = L_c+L_{ca}. After current transfer to the secondaries is completed at t_3, L_t freewheels across V1 (=V2'), forcing current I_c into the parallel combination of L1 and L2. The downslope of Ic and the average I_c (=I_a+I_b) is determined by Vout across L_t. L1 and L2 have almost no effect on the total output current because L_t is very much larger than L1 and L2 in parallel. The total output current I_c (I_a+I_b) is maintained by the control loop at the level required to keep the output voltages in regulation.

With V1 = V2', the voltages across L1 and L2 are equal during the entire OFF time, so that not only are the peak I_a and I_b values proportioned to peak I_c according to the inductor ratios of equation 4, but their current slopes and average output currents have the same proportional relationships.

So with zero output voltage differential, the average currents I_a and I_b are apportioned strictly by L1 and L2 as per equation 3 and their ratio is inversely proportional to the inductances:

$$I_a/I_b = L2/L1$$

However, the actual load currents cannot be expected to observe the ratio established above. To change the I_a/I_b ratio consistent with actual load current requirements requires a small differential voltage, ΔV_{12}, between output voltages V1 and V2. This differential is so small compared to V1 and V2 that it has negligible effect on the total current I_a and I_b, but it will cause the current slopes in L1 and L2 to diverge, changing the apportionment of average current between I_a and I_b.

Figure 6 shows what happens when I_b is reduced by 25% below the value set by the inductor ratio. The dash line shows the current waveforms when V1 = V2', as in Figure 5. Suppose I_b=6A, I_a=12A so that I_c=18A. If the load on output #2 changes causing I_b to drop 25% to 6A but I_a stays at 12A, then I_c must drop by the same 2A to 16A. The control loop will make this happen. However, if V1 remains equal to V2' I_a and I_b will drop proportionately, by 1.333A and .667A respectively, as shown by the dotted lines. In order to reduce I_b by 2A and keep I_a at the original level, a small differential voltage ΔV_{12} will appear between V1 and V2. V2 will become more positive than V1, increasing the I_b downslope and in this case causing I_a to slope upwards. The solid lines in Figure 5 show the resulting waveforms. Note that the slopes change but not the initial peak values.

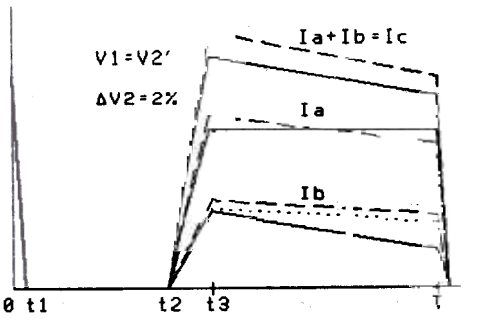

Figure 6 - Two Outouts, ΔV2 = 2%

The voltage differential ΔV_{12} is the output voltage cross-regulation error accompanying the change in load current on one output. The error will appear in whichever output is <u>not</u> sensed and regulated by the control circuit, regardless of which output experiences the load change. The magnitude of the cross-regulation error is:

$$\Delta V_{12} = \frac{2\Delta I_b \cdot L2}{T(1-D)^2} = -\frac{2\Delta I_a \cdot L1}{T(1-D)^2} \qquad (1\text{-}D) = Vin/(Vo+Vin) \qquad (5)$$

Where D is the duty cycle and T the switching period = $1/f_s$. In the continuous mode example given in Table I, L1 is .02 µH while L2 is .07+.012 = .082 µH. With ΔV_{12} = 0, I_a/I_b = .082/.02 = 4/1. Having I_a 4 times greater than I_b with ΔV_{12} = 0 is probably acceptable if output #1 has most of the load power requirement of the supply, because a relatively small ΔV_{12} can make the necessary adjustment. (Normalized load currents are proportional to load power because the normalized voltages are the same.)

With D=.36 and T=10µsec, equation 5 predicts ΔV_{12} of .01V for a 1A change in I_a (10 mΩ). This is a 0.2% change in voltage for an 8.33% change in current. For a 1A change in I_b the voltage differential is -.04V (40 mΩ). This is a .8% change in voltage for a 16.7% change in current. If the #1 output is actually 15V with a 3:1 turns ratio, the latter translates to an actual .12V differential for a 1/3 A change, or 0.36Ω.

Note that equation 5 shows a linear relationship between current and voltage changes. But be careful. If ΔV_{12} becomes too large, the I1 or I2 downslope may reach zero current before the end of the switching period. The output reaching zero becomes discontinuous and the cross-regulation becomes much worse. Equation 5 no longer applies. If the output that becomes discontinuous is sensed for closed loop control, the loop gain characteristics probably change (this has not been evaluated).

Equation 5 also shows that cross-regulation improves when duty cycle D smaller, which occurs with high Vin.

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Cross-regulation in the Discontinuous Mode:
The waveforms of Figure 7 show the secondary currents of the Figure 3 flyback circuit operated in the discontinuous mode with V1 = V2' ($\Delta V_{12} = 0$). The peak values, the downslope and the average current values are all proportioned the same as determined by L1 and L2, just as with the continuous mode. Equation 4 applies to the discontinuous mode, as well. However, in the discontinuous mode, all the inductor values are much smaller (except for wiring inductance) so that the slopes are much steeper, and the peak current is nearly twice the discontinuous mode. Transfer time t_3-t_2 is much shorter and less energy goes to the clamp.

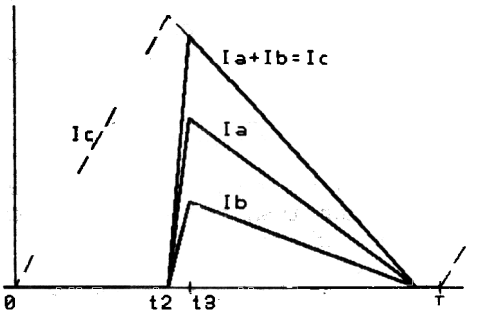

Figure 7 - Two Outputs, V1

In the discontinuous mode example given in Table I, L1 and L2 are both .02μH, dominated by winding inductances. This means that with V1=V2, I_a and I_b are equal (not as shown in Figure 7). If ΔV_{12} is changed to decrease I_a and increase I_b, the current waveforms in an actual flyback circuit will look like Figure 8. The current in one secondary looks like a spike, while the other secondary has a rounded waveform. The curvature is because of small voltage changes across the output capacitors and their ESRs. In spite of the strange shape, the normalized currents add up to the expected triangular waveform.

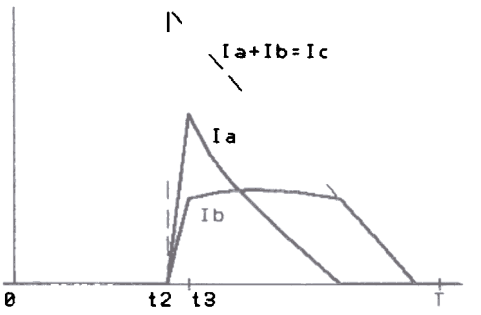

Figure 8

Figure 9 shows the situation of Figure 7 with I_b reduced in current and I_a constant. The explanation of its behavior is similar to the continuous mode example of Figure 6. If I_b is decreased by 2A and I_a stays the same, then the control circuit must reduce I_c by 2A. But this will cause the average I_b and I_a to decrease proportionately by .667A and 1.33A respectively as shown by the dotted lines. So an output voltage differential ΔV_{12} is necessary in order to decrease the downslope of I_a to maintain its original average value, and increase the downslope of I_b to reduce its average value by the desired 2A.

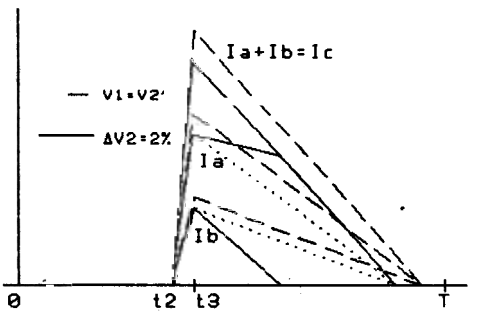

Figure 9 - Two Outputs ΔV2' = 2%

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Compared to the continuous mode, there is one big difference: In the discontinuous mode, one triangle becomes a trapezoid (I_a), while the other triangle gets a smaller base. The relationship between voltage changes and current changes is much more complex and non-linear:

$$\Delta I_a = \frac{I_{a0}}{(Vl \cdot Lp/(\Delta V_{12} L_t) + 1)} \quad , \qquad \Delta I_b = \frac{I_{b0}}{(Vl \cdot Lp/(\Delta V_{12} L_t) + 1)} \qquad (6)$$

Where Lp is the parallel combination of L1 and L2. ΔI is solved in terms of ΔV rather than the other way around because the equation is much simpler. Because of the non-linearity of the ΔV-ΔI relationship, the changes must all be calculated from a specific starting condition, which is with V1 = V2 (ΔV=0), as depicted in Figure 7. I_{a0} and I_{b0} are the average values under this condition, which must be predefined.

For the example given in Table I, I_{a0}/I_{b0} = L2/L1 = .02/.02. Therefore I_{a0} equals I_{b0}. Taking an arbitrary starting point of 9A total normalized output current, I_{a0} and I_{b0} will both equal 4.5A. Using equation 6, ΔV_{12} calculates to be .019V (.019mΩ). Note from the form of equation 6 that ΔI_a changes proportional to the starting value of I_{a0} with ΔV_{12} fixed. Thus a ΔV_{12} of .019V will support a 2A ΔV_{12} if I_{a0} and I_{b0} are raised to 9A (.0095mΩ).

TABLE I -- DISCONTINUOUS VS. CONTINUOUS MODE EXAMPLE

Input: 100 W , f_S: 100 kHz Refer to Figure 3

	Continuous Mode		Discontinuous Mode	
	Actual	Normalized	Actual	Normalized
Core Type, (Area Product	EC35 (AP=.94)		LP22/13 (AP=.33)	
Primary: Turns	180	6	60	2
V_{in}	-300	-10	-300	-10
$I_{in(pk)}$	1.1	33	2.0	60
V_{CL} (clamp)	300	10	300	10
Output 1: Turns	6	6	2	2
V1	5	5	5	
I1	12	12	12	
Output 2: Turns	18	6	6	
V2	15	5	15	
I2	2	6	2	
Windings are not interleaved				
L_c		5 µH		0.5 µH
L_{ca}		.14 µH		.016µH
L_{w1}	.02	.02	.02	.02
L_{ab}		.07		.008
L_{w2}	11	.012	.11	.012
L_{ps}		.156		.026
L_{12}		.1		.04
Watts into clamp:	15.99	15.99	8.48	8.48 W

How to Calculate the Amount of Leakage Inductance: Leakage inductance represents the energy storage between two windings. It may be roughly calculated from the winding geometry, using the inductance formula:

$$L = N^2 \mu_o \mu_r \cdot \text{Area/Length} \times 10^{-2}$$

In the S.I. system of units, $\mu_o = 4\pi \cdot 10^{-7}$. For the non-magnetic materials between and within the windings, $\mu_r = 1$. For concentric coils, "Area" is the cross-section in cm^2 of the hollow cylindrical shape between the windings (the distance from the middle of one winding to the middle of the other, multiplied by the average length of one turn). "Length" is the length of the cylindrical shape -- the length of the winding in cm^2, or the breadth of the winding window. N is the number of turns in the whichever winding the leakage inductance will be referenced to. With the windings normalized, it doesn't make any difference.

How to Minimize Leakage Inductance:

1. Windings must be long and thin (few layers) for intimate coupling. Pot cores have very poor window form factor - windings are short and thick. Ferrite ETD and LP cores are good. Mo-Permalloy powder toriods provide the best winding form factor but they are probably too lossy for use in discontinuous mode applications because of the large flux swings involved.

2. Secondaries must be tightly coupled to get good cross-regulation. Wind multifilar, otherwise as close together as possible. Don't sandwich the primary between two secondaries. This reduces eddy current losses but hurts cross-regulation.

3. Primary to secondary leakage inductance does not hurt cross-regulation, but it does divert much of the inductor energy into the clamp. In off-line applications, insulation requirements force significant area between primary and secondary windings which cam make the leakage inductance quite large. If necessary, interleave the primary and secondaries by putting on half the primary turns, then all the secondaries, then the other half of the primary turns outside the secondaries. The primary halves must be series connected. (Never parallel windings that are at different levels in the winding structure or large circulating current will result.) Interleaving will reduce primary-secondary leakage inductance by a factor of three, but it reduces the leakage inductance between secondaries very little and therefore has little effect on cross-regulation.

How to Minimize Wiring Inductance: Wiring inductance is especially critical in low voltage, high current outputs.

1. Minimize the area enclosed by the loop from the transformer secondary through the rectifier to the filter capacitor and back to the secondary. Keep the distances as short as possible and keep the outward and return conductors very close to each other. A ground plane is no good for the return path unless the outward conductor is held very close to it.

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2. Don't use round wire, use flat strip or braid with their breadths facing each other as closely as possible. Two copper strips 1 cm wide and 10 cm long spaced 0.3 cm apart have a total inductance of 20 nH. Spread apart, the inductance will rise to 100 nH.

What Sequence for the Secondaries: Referring to Figure 3, with zero differential between the normalized output voltages, the output currents will divide according to the ratio of inductances L_{w1} vs. $L_{ab}+L_{w2}'$. A high voltage output will usually have much lower normalized wiring inductance (because it is reduced by N^2). If the high voltage output is in position 1 with the closest coupling to the primary, it will take most of the normalized current (and power output). A large differential offset will be required to force power to output #2 to achieve a better balance.

Because the low voltage output has higher normalized wiring inductance, it usually makes sense to put it in the #1 position closest to the primary, where its wiring inductance helps to balance out leakage inductance L_{ab}. This will provide better distribution of power without requiring as much output voltage offset. Better balance can be achieved by deliberately increasing wiring inductance selectively, but this will hurt cross-regulation.

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