Elimination of the Positive Zero in Fixed Frequency Boost and Flyback Converters

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It is shown how a fixed-frequency, leading-edge modulated PWM can eliminate the undesirable positive zero in practical boost and flyback converters. This allows a substantial improvement in the closed-loop characteristics. Several techniques are employed to predict this result. The design procedure for elimination of the positive zero is presented. Experimental verification is provided.

I. INTRODUCTION

A. Background

State-space averaging [1] predicts a positive zero in the control-to-output transfer function of boost and flyback converters operating in the continuous mode. The 90 degree phase lag severely constrains the loop gain crossover to a frequency much lower than the right-half-plane zero. This limits the dynamic performance of the converter.

The PWM Switch Model [2] is an alternative average modelling technique that is easier to implement in circuit analysis programs such as SPICE. The small-signal characteristics of the PWM switch model are identical to state-space averaging in the continuous conduction mode. It is used throughout this paper.

Average models, however, do not accurately predict the behavior of power converters under all circumstances. It has been shown [3] that when the error compensation signal is pulsating due to the ESR of the output capacitance, that the Discrete-Average Model has better accuracy. The Discrete-Average Model employs the identical averaging of the state variables. The only difference is that the output equation is not averaged. The output equation of the converter power state depends on the type of modulation that is performed in the pulse-width-modulator. This is described later in detail.

Conventional PWM converters are designed with trailing-edge modulation. In trailing-edge modulation, the PWM signal is turned on at the clock signal and turned off when the error signal intersects the ramp waveform. Almost all commercially available PWM integrated circuits operate on this principle. However, it is just as easy to implement leading-edge modulation. In leading-edge modulation, the PWM signal is turned off at the clock signal and turned on when the error signal crosses the ramp waveform.

It is shown that the positive zero can be eliminated from the power stage transfer function of boost and flyback regulators under suitable conditions. These conditions are as follows:

1) Leading-edge modulation must be employed in the pulse-width-modulator.
2) The feedback compensation must not average the ESR-generated output voltage switching ripple.
3) Appropriate power stage parameter values are necessary.

B. Motivation

The motivation behind this study originated after a stability analysis of a spacecraft battery discharger employing a boost topology could not predict the converters' excellent performance and stability. The converter, which was designed in the early 1970's, has been operating in space, flawlessly, for about 15 years. The stability analysis, however, which employed the state-space averaging technique, indicated that the converter should be unstable.

II. MODELLING TECHNIQUES

A. Waveform Analysis

Systems that contain a right-half-plane zero, often referred to as nonminimum phase systems, have a unique step input response shown in Fig. 1. The output will initially drop prior to rising and reaching steady state.

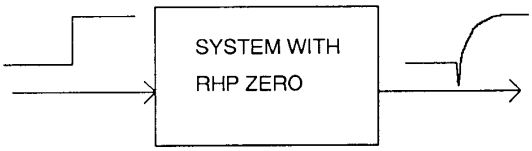

Fig. 1. Nonminimum-Phase-Zero Characteristic Step Response. *The step input response of a system containing a positive zero will initially decrease prior to rising and reaching steady state.*

In boost and buck-boost derived converters, an incremental step increase in duty cycle translates to increased capacitor hold-up time for the output voltage. This will cause the *average* output voltage to initially drop until the inductor current builds up to recharge the capacitor. The lag time from the initial drop until the voltage returns to the initial value is inversely proportional to the positive zero.

However, depending on the dynamics of the feedback compensation network, the PWM error processor may respond to the *instantaneous* output voltage. When conventional trailing-edge modulation is employed, the PWM responds to the instantaneous voltage prior to the switch turning off. When leading-edge modulation is employed, the PWM responds to the instantaneous voltage prior to the switch turning on.

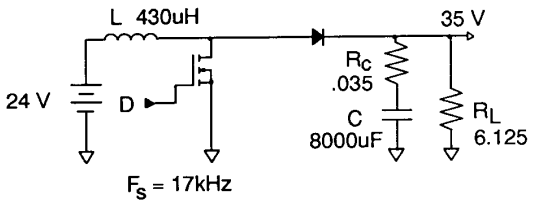

Fig. 2a. Simulated Boost Converter

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Fig. 2a shows a boost regulator schematic that was simulated in SPICE. Fig. 2b shows the switch current waveform. At t = 3 ms, a step increase in duty cycle occurs. The inductor current increases immediately (labeled point A on the figure). The control-to-inductor current transfer function does not contain a positive zero. Fig. 2c shows the voltage waveform directly across the output capacitor. At the step increase in duty cycle, the capacitor voltage waveform initially drops before recovering. This is true for the average capacitor voltage, as well as the instantaneous voltage after the switch turns off (labeled point B on the figure) and the instantaneous voltage after the switch turns on again (labeled point C on the figure). The positive zero cannot be eliminated from the control-to-capacitor voltage transfer function. The capacitor voltage is the same as the average output voltage. Fig. 2d shows the output voltage waveform. At the instant that the switch turns off or on, there is a discontinuous jump in the output voltage due to the voltage drop across the capacitor ESR. At the step increase in duty cycle, the instantanous output voltage, prior to switch turn-off, (labeled point D on the figure) initially drops, as in the capacitor voltage. Thus, when employing trailing-edge modulation, the positive zero cannot be eliminated. The instantanous output voltage prior to switch turn on, (labeled point E on the figure) however, increases. It is a necessary condition for elimination of the positive zero that the instantaneous output voltage, prior to switch turn on, increase in response to an incremental increase in duty cycle. This is dependent on the power inductance, capacitance, load resistance, capacitor ESR, and operating duty cycle.

This condition for elimination of the positive zero can be approximately derived by viewing the steady stage waveforms shown in Fig. 3. The output voltage, v_{o1}, at the instant prior to the switch turning on is the sum of the instantaneous capacitor and ESR voltages:

$$v_{o1} = v_{c1} + v_{rc1} \tag{1}$$

The instantaneous capacitor voltage prior to the switch turning on is equal to the average output voltage plus the change in capacitor voltage due to the average charging current.

$$v_{c1} = V_o(1 + \frac{dT_s}{2R_LC}) \tag{2}$$

The intantaneous ESR voltage prior to the switch turning on is given by:

$$v_{rc1} = V_o(\frac{R_c}{R_L(1-d)} - \frac{(1-d)dT_sR_c}{2L}) \tag{3}$$

Let d = D + $\hat{d}$. The new value of the output voltage at the instant prior to the switch turning on, v_{o1}', is derived in terms of the old value, v_{o1}, plus a function of the incremental duty cycle.

$$v_{o1}' = v_{o1} + \hat{d}T_sV_o(\frac{R_c}{L} - \frac{1}{R_LC(1-D)}) \tag{4}$$

To eliminate the positive zero, the new value of the output voltage at the instant prior to the switch turning on must be greater that the old value. This condition is given by:

$$R_cC > \frac{L}{R_LD'} \tag{5}$$

B. Discrete-Average Model Mathematical Derivation

State-space averaging is implemented by writing the state equations and output equation for the linear networks corresponding the switch-on and switch-off conditions. The equations are then weighted according to the switch-on and switch-off periods.

$$\dot{x} = (dA_1 + d'A_2)x + (dB_1 + d'B_2)u \tag{6}$$

$$v_o = (dC_1 + d'C_2)x \tag{7}$$

These equations are then linearized in order to obtain the equivalent small signal circuit and the resulting transfer functions. The Discrete-Average Model is similar to the average model in that the average of the state variables is used. However, the output voltage is determined by discrete samples. The sample point is dependent on whether

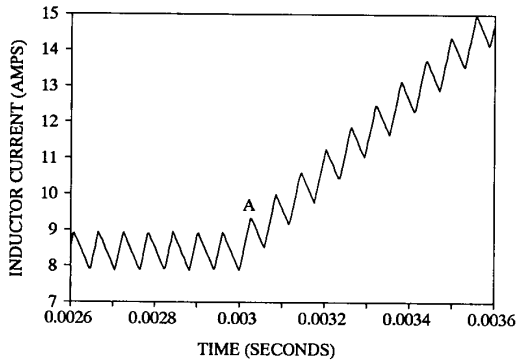

Fig. 2b. Inductor Current Time Waveform. *At the step increase in duty cycle at t = 3ms, the inductor current immediately rises indicating no positive zero in the duty cycle to inductor current transfer function.*

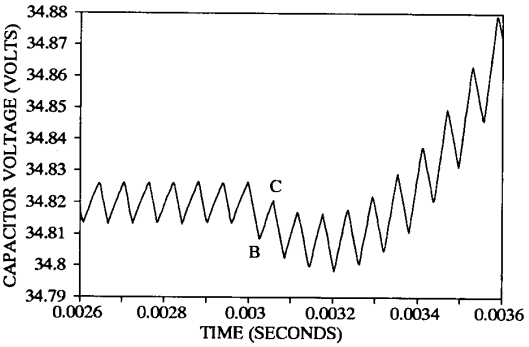

Fig. 2c. Capacitor Voltage Time Waveform. *At the step increase in duty cycle, the capacitor voltage waveform decreases prior to increasing. This indicates that the duty cycle to capacitor voltage transfer function contains a positive zero.*

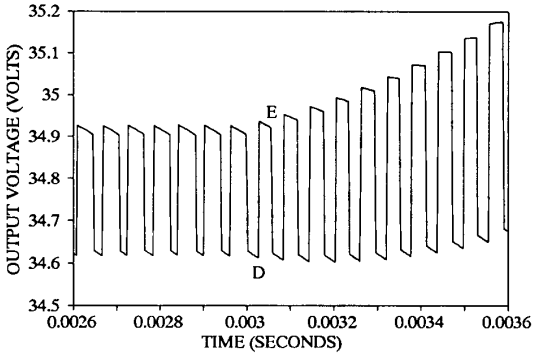

Fig. 2d. Output Voltage Time Waveform. *At the step increase in duty cycle, the valley of the output voltage waveform (D) initially decreases prior to increasing. The peak of the output voltage waveform (E) increases immediately.*

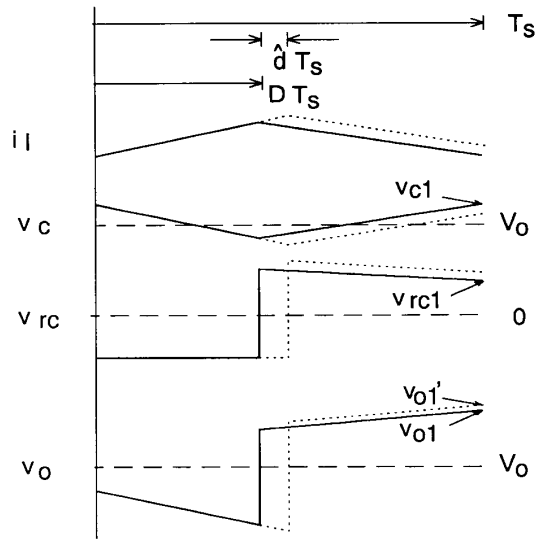

Fig. 3. Steady State Waveforms.

trailing-edge or leading-edge modulation is employed. When conventional trailing-edge modulation is employed, the PWM responds to the instantaneous output voltage while the switch is on in order to determine the termination point of the on time.

$$v_o = C_1 x \tag{8}$$

When leading-edge modulation is employed, the PWM responds to the instantaneous output voltage while the switch is off in order to determine the termination point of the off time.

$$v_o = C_2 x \tag{9}$$

This leads to some subtle differences in the control-to-output transfer function of the three models. The control-to-output transfer function of the Average model is given by:

$$\frac{\hat{v}_o}{\hat{d}} = \frac{V_i}{D'^2} \frac{(1 + s/\omega_z)(1 - s/\omega_a)}{(1 + s/\omega_o Q + s^2/\omega_o^2)} \tag{10}$$

where

$$\omega_z = \frac{1}{R_c C}, \quad \omega_a = \frac{D'^2 R_L}{L} \tag{11}$$

$$\omega_o = \frac{D'}{\sqrt{LC}}, \quad Q = \frac{D'}{\omega_o} \frac{1}{\frac{L}{D'R_L} + R_c C} \tag{12}$$

The control-to-output transfer function of the Discrete-Average model for trailing-edge modulation is given by:

$$\frac{\hat{v}_o}{\hat{d}} = \frac{V_i}{D'^2} \frac{(1 - s/\omega_a)}{(1 + s/\omega_o Q + s^2/\omega_o^2)} \tag{13}$$

The control-to-output transfer function of the Discrete-Average model for leading-edge modulation is given by:

$$\frac{\hat{v}_o}{\hat{d}} = \frac{V_i}{D'^2} \frac{(1 + s/\omega_{a1})}{(1 + s/\omega_o Q + s^2/\omega_o^2)} \tag{14}$$

where

$$\omega_{a1} = \frac{1}{\frac{R_c C}{D'} - \frac{L}{D'^2 R_L}} \tag{15}$$

This model predicts that the positive zero can be eliminated with leading-edge modulation provided that the following condition is held:

$$R_c C > \frac{L}{D' R_L} \tag{16}$$

C. SPICE Implementation of Discrete-Average Model

The Discrete-Average Model can be easily implemented in SPICE using a minor modification to the PWM switch model. For trailing-edge modulation, the output equation is given by:

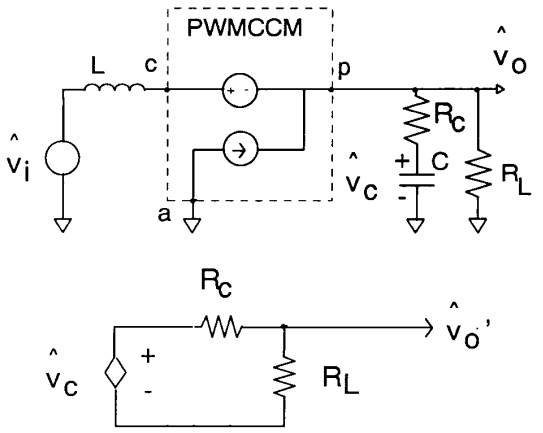

Fig. 4a. SPICE Implementation of Discrete-Average Model with Trailing-Edge Modulation. *The voltage v_o' corresponds to the output voltage that the control loop will respond to while v_o is the average output voltage.*

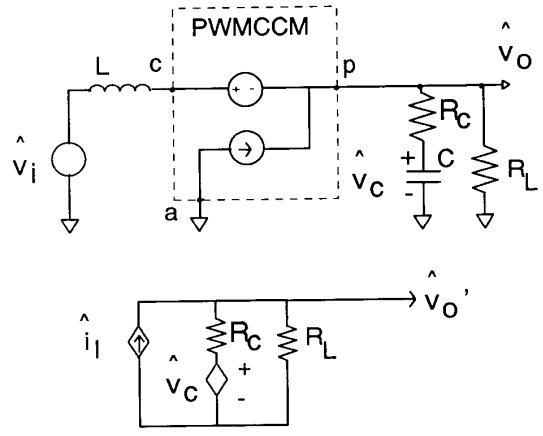

Fig. 4b. SPICE Implementation of Discrete-Average Model with Leading-Edge Modulation

$$v_o = C_1 x = \frac{v_c R_L}{R_L + R_c} \cong v_c \tag{17}$$

This SPICE implementation is shown in Fig. 4a. The feature in SPICE known as dynamic multiplication of variables [4] is employed for easy modelling of the PWM block. For leading-edge modulation, the output equation is given by:

$$v_o = C_2 x = \frac{i_l R_L R_c}{R_L + R_c} + \frac{v_c R_L}{R_L + R_c} \cong R_c i_l + v_c \tag{18}$$

This SPICE implementation is shown in Fig. 4b.

Once the feedback loop is closed, proper implementation of the Discrete-Average Model also includes the sampling of the compensation network output. This is described in section III.

D. Model Comparison

The boost regulator power stage of Fig. 2a is modeled in SPICE with 3 techniques, averaging, discrete-averaging with leading-edge modulation, and discrete-averaging with trailing-edge modulation. Fig. 5 shows the control-to-output transfer functions that result from the three models. There are significant differences, especially with regard to the phase. The positive zero is apparent in the average model and the trailing-edge discrete-average model, by viewing the asymptotic phase response. It is absent from the leading-edge discrete-average model. This boost regulator can, in fact, behave like any one of these three results, depending on the type of modulation and feedback compensation.

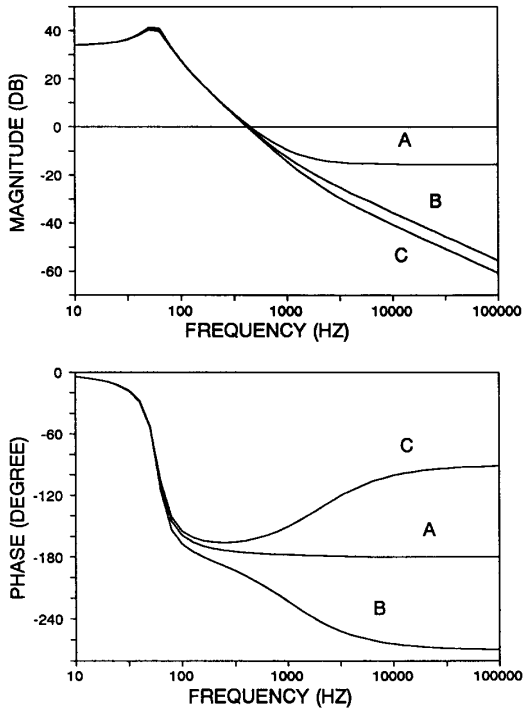

Fig. 5. Control-to-Ouput Transfer Function of Average Model (A), Discrete-Average Model with Trailing-Edge Modulation (B), and Discrete-Average Model with Leading-Edge Modulation (C).

III. COMPARISON WITH CURRENT-MODE CONTROL

A single-loop, leading-edge modulated boost converter has many similarities to a current-mode controlled boost converter. The PWM samples the error signal when the power switch is off. At this time the inductor current is charging the capacitor and feeding the load. The voltage across the capacitor ESR is thus proportional to inductor current. The compensation network amplifies this signal to produce a current sense ramped waveform. This is then compared with the external ramp in the pulse-width-modulator. Recent analysis of current-mode control [5] provides an accurate model of the modulator gain characteristic. Fig. 6 is a block diagram of the system. The gain of the modulator is given by:

$$F_m = \frac{1}{(S_n + S_e)T_s} \tag{19}$$

where S_n is the slope of the error signal, and S_e is the slope of the external ramp. The current feedback loop in a current-mode controlled regulator also has a frequency dependent element due to the sampling nature of the system. This is given by:

$$H_e(s) \cong 1 + \frac{s}{\omega_n Q_z} + \frac{s^2}{\omega_n^2} \tag{20}$$

where

$$Q_z = \frac{-2}{\pi}, \omega_n = \frac{\pi}{T_s} \tag{21}$$

Hence, although the boost regulator positive zero is eliminated from the power stage, two additional positive zeroes located at one half the switching frequency are introduced due to the sampling nature of the system. These two positive zeros limit the crossover frequency of the loop gain to below approximately one-fifth of the switching frequency. This is much less constraining, however, than the power stage positive zero which can often limit crossover to below $F_s/30$.

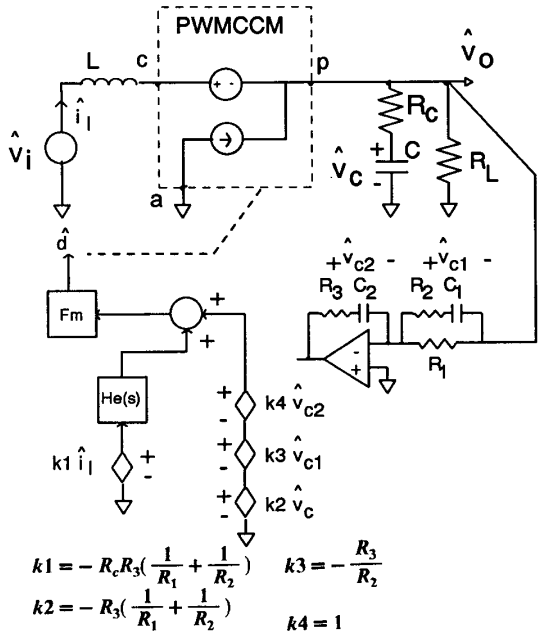

Fig. 6. System Block Diagram. *This representation of the power converter and control loop averages all four of the system state variables yet samples the error signal while the switch is off.*

Proper implementation of the Discrete-Average Model also includes the sampling of the compensation network output. In Fig. 6 the compensation network has two additional state variables, v_{c1} and v_{c2} The output equation of this network is given by:

$$v_e = \frac{-R_3}{R_2} v_{c1} + v_{c2} - \left(\frac{R_3}{R_1} + \frac{R_3}{R_2}\right) v_o \qquad (22)$$

where

$$v_o = R_c i_l + v_c \qquad (23)$$

This output equation is implemented with the controlled sources and summing network shown in Fig. 6.

The dependence of the modulator gain on the slope of the error signal acts to mitigate the effects of varying compensator gain or ESR. For example, a decrease in ESR will reduce the gain of the power stage by moving the zero to a higher frequency. However, it will increase the modulator gain by reducing the ripple on the error signal.

IV. PRACTICAL CIRCUIT DESIGN

A. Power Component Selection

A boost converter is designed to the following specifications:

$$V_i = 20 - 25V$$
$$V_o = 30V \pm .3Vp - p$$
$$F_s = 25kHz$$
$$P_o = 0 - 50W$$

An inductor value of $350\mu H$ is chosen to allow for a $\pm$ 15% current ripple at the low line, high load condition. $660\mu F$ of capacitance with an ESR of $0.075m\Omega$ is used to filter the ripple to the specified value. The condition for elimination of the positive zero is met.

B. Leading-Edge PWM

Most PWM IC's employ trailing-edge modulation. By simply inverting the output pulse, the leading-edge is modulated. To retain negative feedback in the control loop, the error signal is also inverted. Most PWM IC's allow for an adjustable duty cycle maximum limit, a necessity for boost regulators. However, the duty cycle maximum limit becomes a duty cycle minimum once the output is inverted. The duty cycle limit can be externally contolled in several ways. In this implementation, a synchronized signal containing a 50% maximum duty cycle was ANDed with the PWM output.

C. Control Loop Design

A two-pole and two-zero compensator is used in the control loop. The first pole is placed at the origin for DC regulation. The two zeroes are placed to obtain the maximum midband gain and a good phase margin in the loop gain while minimizing the system transient response settling time. The first zero was placed just after the resonant frequency to avoid a conditionally stable system. The second zero was placed at approximately twice the frequency of the first zero. The second pole was placed to cancel the zero in the power stage that has now been moved to the left-half-plane. A wide bandwidth operational amplifier (LM318) was employed to provide the necessary gain at the switching frequency.

Fig. 7 is a schematic diagram of the entire power converter circuit including power stage, PWM and control.

V. SYSTEM MEASUREMENTS

A. Loop Gain Measurement

Fig. 8 is a photograph of the steady-state gate drive signal, error signal and output voltage. There is a large discontinuity in the error signal. Conventional loop gain measurement using analog injection techniques will not yield correct results under these circumstances [6]. When an AC signal is injected into the feedback loop, the output voltage and error signal will be both amplitude modulated and duty cycle modulated. The amplitude modulation contains an upper side, corresponding to when the switch is on, and a lower side corresponding to when the switch is off. The crucial gain and phase information is contained in the upper side of the amplitude modulation component. However, the network analyzer tracks all components. The gate drive signal, however, is only duty cycle modulated. This is the only signal in the loop which contains only one modulation component. In order to properly measure the loop gain, digital modulation and measurement must be employed [6]. Fig. 9 shows the theoretical and experimental loop gain taken at the minimum line and maximum load condition. The theoretical and experimental results are in excellent agreement up to one-half of the switching frequency. The crossover frequency is about 5 kHz, which is one-fifth of the switching frequency. The phase margin is over 60 degrees. Had this been a conventional trailing-edge modulated boost converter, the system would have been unstable. The positive zero would have been at about 3 kHz, causing an additional 45 degrees of phase lag at this frequency. Loop gain crossover would have been constrained to be at about 1 kHz to maintain 60 degrees of phase margin.

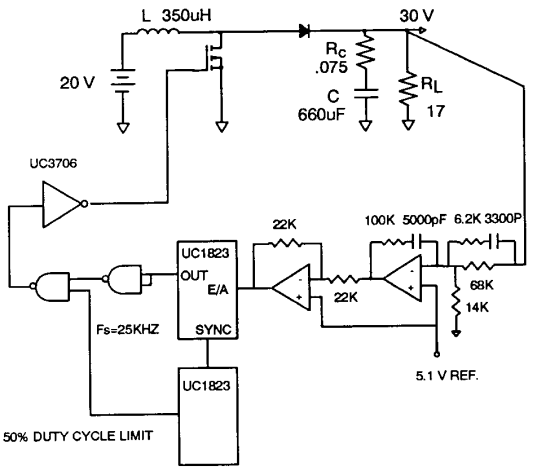

Fig. 7. Schematic Diagram of Entire Power Converter Circuit

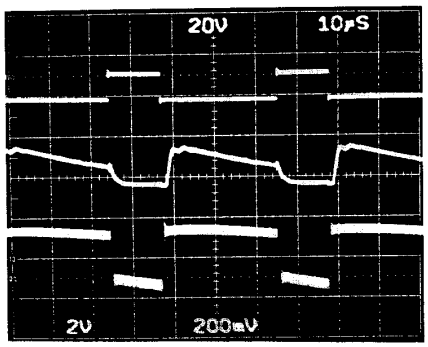

Fig. 8. Photograph of Steady State Gate Drive Signal (20 V/Div.), Error Signal (2 V/Div.), and Output Voltage Waveform (0.2 V/Div. AC). *The slope of the error signal while the switch is off partially determines the gain of the modulator.*

B. Measurement of the Control-to-Output Transfer Function

Fig. 10 is a photograph of the error signal and output voltage in the

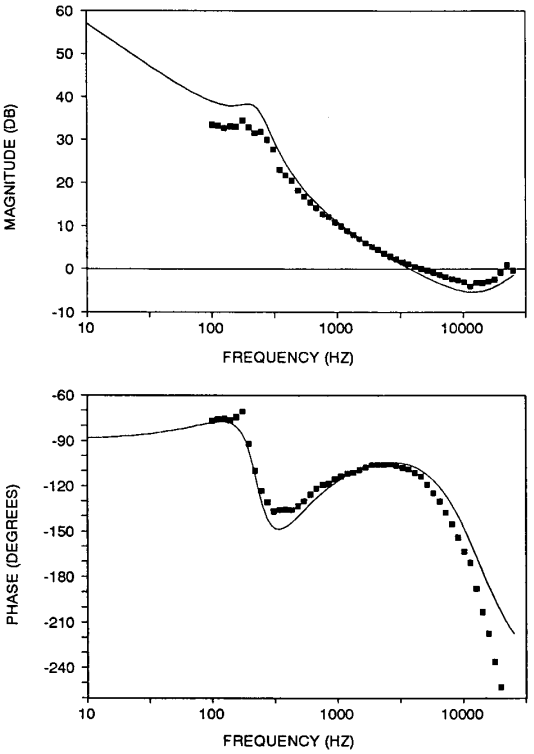

Fig. 9. Theoretical (solid line) and Experimental Loop Gain

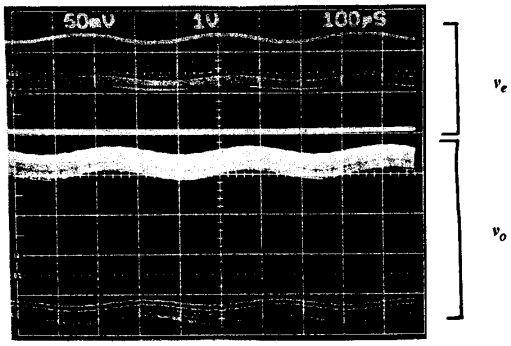

Fig. 10. Photograph of Error Signal (1 V/Div.) and Output Voltage (50 mV/Div. AC) with 3 kHz Modulation. *Both the error signal and output voltage waveform appear to be two separate signals due to their discontinuity. The modulation on the upper half of the error signal corresponds to the modulation on the upper half of the output voltage. The lower half of error signal is clipped by the feedback amplifier. The phase lag of of the bottom half of the output voltage is significantly greater than the top half.*

presence of an external 3 kHz disturbance. The double-sided amplitude modulation of the output voltage is clearly visible. There is a significant phase difference between the top and bottom halves. The top half does not contain the positive zero while the bottom half does.

One would like to measure the control-to-output transfer function prior to closing the loop. However, this is not practical in this circumstance. If the error signal and output voltage are placed into the reference and test inputs of a network analyzer, the results will agree with the average model. The network analyzer averages all the components of the output voltage switching ripple. This system is unique in that the open loop plant characteristic in fact depends on the feedback control dynamic characteristics. Once the loop is closed, the control-to-output transfer function can be indirectly measured by subtracting the compensator transfer function from the loop gain. This measurement requires care as well, since the compensator input and output are both discontinuous. One possibility, is to employ a sample-and-hold circuit. However, this will introduce phase errors that must be accounted for. The lack of a good measurement procedure for the control-to-output transfer function is one drawback for this technique.

VI. CONCLUSIONS

It has been shown how the right-half-plane zero can be eliminated from practical boost converter circuits. The right-half-plane zero is eliminated under the following conditions:

1) Leading-edge modulation must be employed in the pulse-width-modulator.
2) Proper power stage parameter values are necessary.

$$R_c C > \frac{L}{D' R_L}$$

3) The switching ripple must not be integrated by the control loop.

The Discrete Average Model is used to predict this result. It is shown how the Discrete Average Model can be implemented in SPICE using a slight variation of the PWM switch model. This same criterion holds for flyback converter circuits. For flyback converters, the inductance L, is the secondary inductance of the flyback transformer.

Conventional analog loop gain measurement is inaccurate due to the pulsating nature of the waveforms. In order to measure the loop gain, digital modulation must be employed.

The theoretical and experimental results indicate high stability margin and wide bandwidth. Loop gain crossover is shown to be much higher than one could ordinarily expect with a conventional trailing-edge modulated boost regulator.

It is shown that leading-edge modulation is very similar to current-mode control in this case. By modulating the leading-edge, the output capacitor current is sampled by sensing the voltage across the ESR. Capacitor current when the switch is off is equal to inductor current minus the load current. By providing an effective feedforward of the load current, this technique ensures excellent load transient response and low output impedance.

There are several disadvantages of this technique. Measurement of the control-to-output transfer function cannot easily be performed. Also, the positive zero elimination is dependent on the capacitor ESR value. Capacitor ESR can often change substantially over temperature. Small changes in the ESR value will not effect the stability margin. This is due to the dependence of the modulator gain on the error signal ripple. However, reduction of the ESR well below the criterion for positive zero elimination will effect system stability. Finally, this technique can be susceptible to noise since the output voltage switching ripple is not filtered in the compensation network.

ACKNOWLEDGEMENTS

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