

June 2008

FSEZ1016A Primary-Side-Regulation PWM Integrated Power MOSFET

Features

- Constant-voltage (CV) and Constant-current (CC)
 Control Without Secondary-feedback Circuitry
- Green-mode Function: PWM Frequency Linearly Decreasing
- Fixed PWM Frequency at 42kHz with Frequency Hopping to Solve EMI Problem
- Cable Compensation in CV mode
- Low Start-up Current 10µA
- Low Operating Current 3.5mA
- Peak-current-mode Control in CV mode
- Cycle-by-cycle Current Limiting
- VDD Over-voltage Protection with Auto-Restart
- VDD Under-voltage Lockout (UVLO)
- Gate Output Maximum Voltage Clamped at 18V
- Fixed Over-temperature Protection with Latch
- DIP-7 and SOP-7 Package Available

Applications

- Battery chargers for cellular phones, cordless phones, PDA, digital cameras, power tools
- Best choice to replace linear transformer and RCC SMPS

Description

This highly integrated PWM controller, FSEZ1016A, provides several features to enhance the performance of low-power flyback converters. The patented topology of FSEZ1016A enables most simplified circuit design especially for battery charger applications. A low-cost, smaller and lighter charger is thus resulted when compared to a conventional design or a linear transformer. The start-up current is only 10uA, which allows use of large start-up resistance for further power saving.

To minimize the standby power consumption, the proprietary green-mode function provides off-time modulation to linearly decrease PWM frequency under light-load conditions. This green-mode function assists the power supply to easily meet the power conservation requirement.

By using FSEZ1016A, a charger can be implemented with fewest external components and minimized cost. A typical output CV/CC characteristic envelope is shown in Figure 1.

FSEZ1016A series controller are available in 7-pin DIP and 7-pin SOP packages.

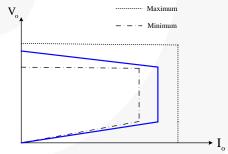


Figure 1. Typical output V-I characteristic

Ordering Information

| Part Number | Operating Junction Temperature | © Eco Status | Package | Packing Method |
|-------------|-----------------------------------|--------------|--|----------------|
| FSEZ1016ANY | -40°C to +125°C | Green | 7-Lead, Dual Inline Package(DIP-7) | Tube |
| FSEZ1016AMY | -40°C to +125°C | Green | 7-Lead, Small Outline Package (SOP-7) | Tape & Reel |

Por Fairchild's definition of "green" Eco Status, please visit: http://www.fairchildsemi.com/company/green/rohs_green.html.

Application Diagram

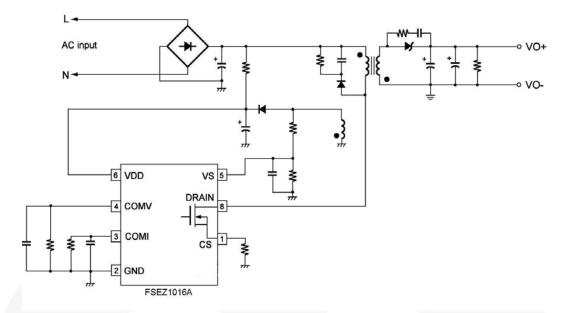


Figure 1. Typical Application

Internal Block Diagram

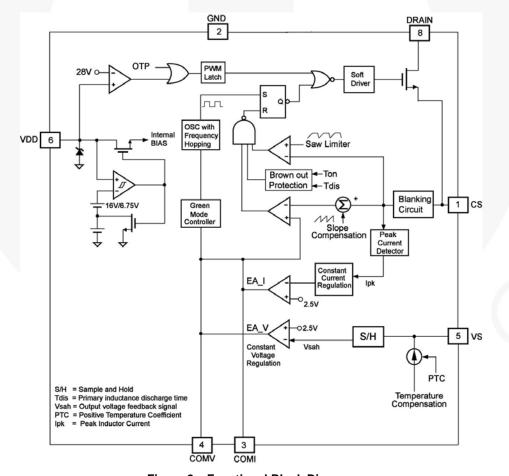
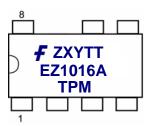


Figure 2. Functional Block Diagram

Marking Information



F- Fairchild logo

Z- Plant Code

X- 1 digit year code

Y- 1 digit week code

TT: 2 digits die run code

T: Package type (N=DIP, M=SOP)
P: Z: Pb free, Y: Green package

M: Manufacture flow code

Figure 3. Top Mark

Pin Configuration

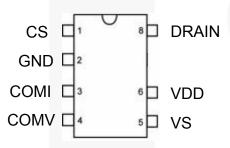


Figure 4. Pin Configuration

Pin Definitions

| Pin# | Name | Description | | | | |
|------|-------|--|--|--|--|--|
| 1 | CS | Analog input, Current sense. Connected to a current-sense resistor for peak-current-mode control in CV mode. The current-sense signal is also provided for output-current regulation in CC mode. | | | | |
| 2 | GND | oltage Reference, Ground. | | | | |
| 3 | COMI | Analog output, Current compensation. Output of the current error amplifier. Connecting a capacitor between COMI pin and GND for frequency compensation. | | | | |
| 4 | COMV | Analog output, Voltage compensation. Output of the voltage error amplifier. Connecting a capacitor between COMV pin and GND for frequency compensation. | | | | |
| 5 | vs | Analog input, Voltage sense. Output-voltage-sense input for output-voltage regulation. | | | | |
| 6 | VDD | Power Supply. | | | | |
| 7 | N.C | | | | | |
| 8 | DRAIN | Power MOSFET Drain. This pin is the high voltage power MOSFET drain | | | | |

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

| Symbol | Parameter | | Min. | Max. | Unit | |
|-------------------|--|-----------------------|------|------|-------|--|
| V_{VDD} | DC Supply Voltage ^(1, 2) | | 30 | V | | |
| V _{VS} | VS Pin input voltage | | -0.3 | 7 | V | |
| V _{CS} | CS Pin input voltage | | -0.3 | 7 | V | |
| V_{COMV} | Voltage Error amplifier output voltage | | -0.3 | 7 | V | |
| V _{СОМІ} | Voltage Error amplifier output voltage | | -0.3 | 7 | V | |
| V _{DS} | Drain-Source Voltage | | | 600 | V | |
| | Continuous Drain Current | T _C =25°C | | 1 | Α | |
| I _D | Continuous Drain Current | T _C =100°C | | 0.6 | Α | |
| I _{DM} | Pulsed Drain Current | | | 4 | Α | |
| E _{AS} | Single Pulse Avalanche Energy | | | 33 | mJ | |
| I _{AR} | Avalanche Current | | 1 | Α | | |
| A 5 | Power Dissipation (T _A <50°C) | DIP-7 | | 800 | mW | |
| P_D | | SOP-7 | 7 | 660 | | |
| Б | Thermal Resistance (Junction to Air) | DIP-7 | | 113 | °C /W | |
| $R_{	heta JA}$ | | SOP-7 | | 153 | | |
| D | The second Designation of County | DIP-7 | | 67 | 90 AM | |
| $R_{	heta JC}$ | Thermal Resistance (Junction to Case) | SOP-7 | | 39 | °C /W | |
| TJ | Operating Junction Temperature | | | 150 | °C | |
| T _{STG} | Storage Temperature Range | | -55 | 150 | °C | |
| TL | Lead Temperature (Wave soldering or IF | R, 10 seconds) | | 260 | °C | |
| ECD | ESD Capability, Human Body Model | | | 2.5 | KV | |
| ESD | ESD Capability, Machine Model | | 200 | V | | |

Notes:

- 1. Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device.
- 2. All voltage values, except differential voltages, are given with respect to GND pin.

Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to Absolute Maximum Ratings.

| Symbol | Parameter | Conditions | Min. | Тур. | Max. | Unit |
|--------|--------------------------------|------------|------|------|------|------|
| TJ | Operating Junction Temperature | | -40 | | 125 | °C |

Electrical Characteristics

 V_{DD} =15V, T_A =25°C, unless otherwise specified.

| Symbol | Parame | ter | Conditions | Min. | Тур. | Max. | Units |
|-------------------------|---|-------------------------------|--|------|------|------|-------|
| VDD SECT | ION | | 1 | | | | • |
| V _{OP} | Continuously Operating Voltage | | | | | 25 | V |
| V _{DD-ON} | Turn-on Threshold | Voltage | | 15 | 16 | 17 | V |
| V_{DD-OFF} | Turn-Off Threshold Voltage | | | 4.5 | 5 | 5.5 | V |
| I _{DD-ST} | Startup current | | 0< V _{DD} < V _{DD-ON} - 0.16V | | 10 | 20 | μA |
| I _{DD-OP} | Operating Current | | V_{DD} =20V, Fs= F_{OSC} , V_{VS} =2V, V_{CS} =3V, C_L =1nF | | 3.5 | 5 | mA |
| I _{DD-GREEN} | Green-mode Operating Supply Current | | V_{DD} =20V, V_{VS} =2.7V $Fs=F_{OSC-N-MIN}$, V_{CS} =0V C_L =1nF, V_{COMV} = 0V | | 1 | 2 | mA |
| $V_{\text{DD-OVP}}$ | VDD Over-voltage-protection level | | V _{CS} =3V, V _{VS} =2.3V V _{DD} =20V → OVP | 27 | 28 | 29 | V |
| t _{D-VDDOVP} | VDD Over-voltage-protection Debounce Time | | V_{CS} =5V, Fs= F_{OSC} , V_{VS} =2.3V, | 100 | 250 | 400 | μs |
| OSCILLAT | OR SECTION | | | | | | |
| | FSEZ1016A Frequency | Center Frequency | T _A = 25°C V _{VS} =2.3V, V _{CS} =5V | 39 | 42 | 45 | |
| Fosc | | Frequency Hopping Range | V _{CS} =1.5V, V _{VS} =2V; | ±1.8 | ±2.6 | ±3.6 | KHz |
| t _{FHR} | Frequency Hopping | Period | V _{CS} =1.5V, V _{VS} =2V; | | 3 | | ms |
| F _{OSC-N-MIN} | Min. frequency at N | lo-Load | V _{VS} =2.7V, V _{COMV} = 0V | | 550 | | Hz |
| F _{OSC-CM-MIN} | Min. Frequency at 0 | CCM | V _{VS} =2.3V, V _{CS} =0.5V | | 20 | | KHz |
| F_{DV} | Frequency Variation Deviation | n Versus V _{DD} | V _{DD} = 10V to 25V | | | 5 | % |
| F _{DT} | Frequency Variation Temp. Deviation | n Versus | T _A = -40°C to 85°C | | | 15 | % |
| VOLTAGE- | SENSE SECTION | | | | | | |
| I _{VS-UVP} | Sink current for Bro | wnout | R _{VS} =20KΩ | | 125 | | μA |
| Itc | IC Compensation B | ias Current | | | 9.5 | | μA |
| V _{BIAS-COMV} | Adaptive Bias volta dominated by V _{COM} | ge v | V_{COMV} =0V, T_A = 25°C, V_{CS} =5V, R_{VS} =20K Ω | | 1.4 | | V |

Electrical Characteristics

 V_{DD} =15V, T_A =25°C, unless otherwise specified.

| Symbol | Parameter | Conditions | Min. | Тур. | Max. | Units |
|-----------------------|---|--|-------|------|-------|-------|
| CURRENT | SENSE SECTION | , | • | | • | |
| t _{PD} | Propagation Delay to GATE Output | | | 100 | 200 | ns |
| t _{MIN-N} | Min. On Time at No-Load | V_{VS} = -0.8V, Rs=2K Ω , V_{COMV} =1V | | 1100 | | ns |
| t _{MINCC} | Min. On Time in CC mode | V _{CS} =5V V _{VS} =0V, V _{COMV} =2V | | 400 | | ns |
| D _{SAW} | Duty Cycle of SAW Limiter | | | 40 | | % |
| V_{TH} | Threshold Voltage for Current Limit | | | 1.3 | | V |
| OLTAGE- | ERROR-AMPLIFIER SECTION | İ | | | | |
| V_{VR} | Reference Voltage | V _{CS} =5V | 2.475 | 2.5 | 2.525 | V |
| V _N | Green-Mode Starting Voltage on COMV pin | V _{CS} =5V, F _S =F _{OSC} - 2KHz V _{VS} =2.3V | | 2.8 | | ٧ |
| V_{G} | Green-Mode Ending Voltage on COMV pin | V _{CS} =5V, F _S =1KHz | | 0.8 | | V |
| I _{V-SINK} | Output Sink Current | V _{VS} =3V, V _{COMV} =2.5V | | 90 | | μA |
| I _{V-SOURCE} | Output Source Current | V _{VS} =2V, V _{COMV} =2.5V | | 90 | | μA |
| V_{V-HGH} | Output High Voltage | V _{VS} =2.3V | 4.5 | \ \ | | V |
| CURRENT | ERROR-AMPLIFIER SECTION | | | | | |
| V_{IR} | Reference Voltage | V _{CS} =5V | 2.475 | 2.5 | 2.525 | V |
| I _{I-SINK} | Output Sink Current | V _{CS} =3V, V _{COMI} =2.5V | | 55 | | μΑ |
| I _{I-SOURCE} | Output Source Current | V _{CS} =0V, V _{COMI} =2.5V | | 55 | | μΑ |
| V_{I-HGH} | Output High Voltage | V _{CS} =0V | 4.5 | | | V |

PRELIMINARY DATASHEET

Electrical Characteristics

V_{DD}=15V, T_A=25°C, unless otherwise specified.

| Symbol | Parameter | Conditions | Min. | Тур. | Max. | Units |
|----------------------------------|---|---|------|------|------|-------|
| INTERNAL | MOSFET SECTION | • | • | • | • | • |
| DCY_{MAX} | Maximum Duty Cycle | | | 75 | | % |
| BV_{DSS} | Drain-Source Breakdown Voltage | I _D =250μA, V _{GS} =0V | 600 | | | V |
| $\Delta BV_{DSS} / \Delta T_{J}$ | Breakdown Voltage Temperature Coefficient | I _D =250μA, Referenced to 25 °C | | 0.6 | | V/°C |
| Is | Maximum Continuous Drain- Source Diode Forward Current | | | | 1 | Α |
| I _{SM} | Maximum Pulsed Drain-Source Diode Forward Current | | | | 4 | Α |
| R _{DS(ON)} | Static Drain-Source On- Resistance | I _D =0.5A, V _{GS} =10V | | 9.3 | 11.5 | Ω |
| | Drain-Source Leakage Current | V _{DS} =600V, V _{GS} =0V, T _C =25 °C | | | 1 | μA |
| I _{DSS} | | V _{DS} =480V, V _{GS} =0V, T _C =100 °C | | | 10 | μA |
| t _{D-ON} | Turn-on Delay Time | $V_{DS}{=}300V, \\ I_{D}{=}1.1A, \\ R_{G}{=}25\Omega_{(1)(2)}$ | | 7 | 24 | ns |
| tr | Rise Time | | | 21 | 52 | ns |
| t _{D-OFF} | Turn-off Delay Time | | | 13 | 36 | ns |
| tf | Fall Time | | | 27 | 64 | ns |
| C _{ISS} | Input Capacitance | V_{GS} =0V, V_{DS} =25V, F_S =1MHz | | 130 | 170 | pF |
| Coss | Output Capacitance | | | 19 | 25 | pF |
| OVER-TEM | PERATURE-PROTECTION SE | ECTION | | | | |
| T _{OTP} | Threshold Temperature for OTP ⁽³⁾ | | | 150 | | °C |

Note:

- 1. Pulse Test : Pulse width \leq 300us, Duty cycle \leq 2%
- 2. Essentially independent of operating temperature
- When the Over-temperature protection is activated, the power system will enter latch mode and output is disabled.

Functional Description

The patented topology of FSEZ1016A enables most simplified circuit design especially for battery charger applications. Without secondary feedback circuitry, the CV and CC control can still be achieved accurately. As shown in Figure 4, with the frequency-hopping, PWM operation, EMI problem can be solved by using minimized filter components. FSEZ1016A also provides many protection functions. VDD pin is equipped with over-voltage protection, also with under-voltage lockout. Pulse-by-pulse current limiting and CC control ensure over-current protection at heavy loads. The GATE output is clamped at 15V to protect the external MOSFET from over-voltage damage. Also, the internal over-temperature-protection function shuts down the controller with latch when over heated.

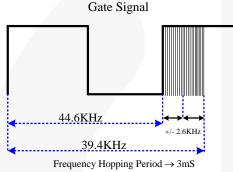


Figure 5. Frequency Hopping

Start-Up Current

The start-up current is only 10uA. Low start-up current allows a start-up resistor with a high resistance and a low-wattage to supply the start-up power for the controller. A 1.5M Ω , 0.25W, start-up resistor and a 10uF/25V V_{DD} hold-up capacitor would be sufficient for an AC-to-DC power adapter with a wide input range (100V_{AC} to 240V_{AC})

Operating Current

The operating current has been reduced to 3.5mA. The low operating current results in higher efficiency and reduces the V_{DD} hold-up capacitance requirement. Once FSEZ1016A enter deep-green-mode, the operating current will be reduced to 1.2mA, thus that can assist the power supply to easily meet the power conservation requirement.

Green-Mode Operation

Figure 5 shows the characteristics of the PWM frequency vs. the output voltage of the error amplifier (V_{COMV}). The FSEZ1016A uses the positive, proportional, output load parameter (V_{COMV}) as an indication of the output load for modulating the PWM frequency. In heavy load conditions, the PWM

frequency is fixed at 42KHz. Once V_{COMV} is lower than V_N , the PWM frequency starts to linearly decrease from 42KHz to 500Hz. Thus providing further power savings and easily meeting international power conservation requirements.

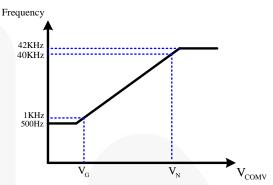


Figure 6. Green-Mode operation Frequency vs V_{COMV}

Constant Voltage(CV) and Constant Current(CC) Operation

An innovative technique of the FSEZ1016A can accurately achieve CV/CC characteristic output without secondary side voltage or current feedback circuitry. There has a feedback signal for CV/CC operation that is from the reflected voltage across the primary auxiliary winding, this voltage signal is proportional to secondary winding, so it provides controller the feedback signal from secondary side and achieve constant voltage output property. In constant current output operation, this voltage signal will be detected and examined by the precise constant current regulation controller, then determined the on-time of the MOSFET to control input power and provide constant current output property. With feedback voltage Vcs across current sense resistor, the controller can obtain input power of power supply. Therefore, the region of constant current output operation can be adjusted by current sense resistor.

Temperature Compensation

The FSEZ1016A has a built in temperature compensation, in order to get better constant voltage regulation at different ambient temperature. This internal compensation current is a positive temperature coefficient (PTC) current that can compensate the forward-voltage drop of the secondary diode of varying with temperature. This variation caused output voltage rising at high temperature.

Leading-Edge Blanking

Each time the power MOSFET is switched on, a turn-on spike will inevitable occur at the sense-resistor. To avoid premature termination of the switching pulse, a leading-edge blanking time is built in. Conventional RC filtering can therefore be omitted. During this blanking period, the current-limit comparator is disabled and it cannot switch off gate driver.

Under Voltage Lockout (UVLO)

The turn-on and turn-off thresholds of the FSEZ1016A are fixed internally at 16V/5V. During start-up, the hold-up capacitor must be charged to 16V through the start-up resistor, so that the FSEZ1016A will be enabled. The hold-up capacitor will continue to supply V_{DD} until power can be delivered from the auxiliary winding of the main transformer. V_{DD} must not drop below 5V during this start-up process. This UVLO hysteresis window ensures that hold-up capacitor will be adequate to supply V_{DD} during start-up.

VDD Over-Voltage Protection

VDD over-voltage protection has been built in to prevent damage due to over voltage conditions. When the voltage VDD exceeds 28V due to abnormal conditions, PWM pulses will be disabled until the VDD voltage drops below the UVLO and then start-up again. Over-voltage conditions are usually caused by open feedback loops.

Over Temperature Protection (OTP)

The FSEZ1016A has a built-in temperature sensing circuit to shut down PWM output once the junction temperature exceeds 150°C. While PWM output is shut down, the V_{DD} voltage will gradually drop to the UVLO voltage. Some of the FSEZ1016A's internal circuits will be shut down, and V_{DD} will gradually start increasing again. When V_{DD} reaches 16V, all the internal circuits including the temperature sensing circuit will start operating normally. If the junction temperature is still higher than 150°C, the PWM controller will be shut down immediately. This situation will continue until the temperature drop below 120°C.

Gate Output

The FSEZ1016A BiCMOS output stage is a fast totem pole gate driver. Cross conduction has been avoided to minimize heat dissipation, increase efficiency, and enhance reliability. The output driver is clamped by an internal 15V Zener diode in order to protect power MOSFET transistors against undesired over-voltage gate signals.

Built-in Slope Compensation

The sensed voltage across the current sense resistor is used for current mode control and pulse-by-pulse current limiting. Built-in slope compensation will improve stability and prevent sub-harmonic oscillations due to peak-current mode control. The FSEZ1016A has a synchronized, positively-sloped ramp built-in at each switching cycle.

Noise Immunity

Noise from the current sense or the control signal can cause significant pulse width jitter, particularly in continuous-conduction mode. While slope compensation helps alleviate these problems, further precautions should still be taken. Good placement and layout practices should be followed. Avoiding long PCB traces and component leads, locating compensation and filter components near the FSEZ1016A, and increasing the power MOS gate resistance is advised.

Applications Information

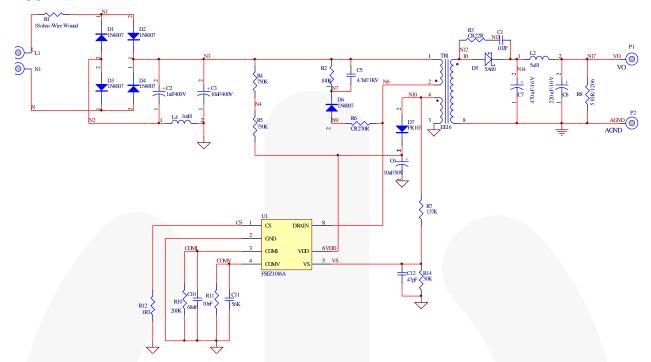


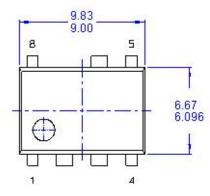
Figure 7. 5W (5V/1A) Application Circuit

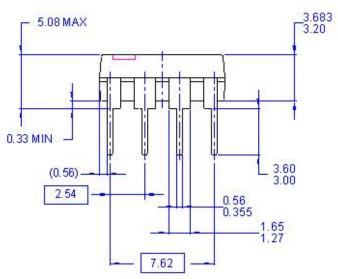
BOM

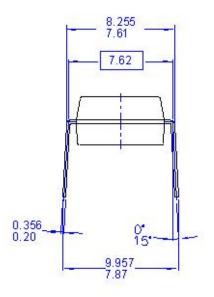
| Designator | Part Type | Designator | Part Type | |
|--------------------|--------------|------------|--------------|--|
| D1, D2, D3, D4, D6 | 1N4007 | R2 | R 100 KΩ | |
| D5 | SB560 | R3 | R 22 Ω | |
| D7 | FR103 | R4, R5 | R 750 KΩ | |
| C1 | 1nF | R6 | R 270 Ω | |
| C2 | EC 1µF/400V | R7 | R 137 KΩ | |
| C3 | EC 10µF/400V | R8 | R 510 Ω | |
| C5 | 4.7nF/1KV | R10 | R 200 KΩ | |
| C6 | EC 10µF/50V | R11 | R 56ΚΩ | |
| C7 | EC 470µF/16V | R12 | R 1.3 Ω | |
| C8 | EC 220µF/10 | R14 | R 30 Ω | |
| C10 | 68nF | L2 | 5uH | |
| C11 | 10nF | L4 | 1mH | |
| C12 | 47pF | T1 | EE16 (1.5mH) | |
| R1 | R 18 Ω | U1 | IC FSEZ1016A | |

Physical Dimensions

7PINS-DIP(N)







NOTES: UNLESS OTHERWISE SPECIFIED

- A) THIS PACKAGE CONFORMS TO JEDEC MS-001 VARIATION BA
- B) ALL DIMENSIONS ARE IN MILLIMETERS.
- C) DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.
- D) DIMENSIONS AND TOLERANCES PER ASME Y14.5M-1994
- E) DRAWING FILENAME AND REVSION: MKT-N08FREV2.

Figure 8. Official FSC Drawings only - ALWAYS include DWG number & revision

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Figure 9. Official FSC Drawings only - ALWAYS include DWG number & revision

E) DRAWING FILENAME: MOSAREV13

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SuperSOTTM-8
SuperSOTTM-8
SuperSOTTM-8
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PRODUCT STATUS DEFINITIONS

Definition of Terms

| Datasheet Identification Product Status | | Definition | | | | |
|---|-----------------------|---|--|--|--|--|
| Advance Information | Formative / In Design | Datasheet contains the design specifications for product development. Specifications may change in any manner without notice. | | | | |
| Preliminary | First Production | Datasheet contains preliminary data; supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design. | | | | |
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