BJ8P153C

8-Bit Microcontroller with OTP ROM

Product Specification

Doc. Version 1.6

BJX MICROELECTRONICS CORP.

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APPENDIX

Specification Revision History

Doc. Version	Revision Description	Date
1.0	Initial version	2008.12.31

1 General Description

The BJ8P153C is an 8-bit microprocessor designed and developed with low-power and high-speed CMOS technology. It has an on-chip 1024 - 13-bit Electrical One Time Programmable Read Only Memory (OTP-ROM). It provides a protection bit to prevent intrusion of user's OTP memory code. Fifteen Code option bits are also available to meet user's requirements.

With its enhanced OTP-ROM feature, theBJ8P153C provides a convenient way of developing and verifying user's programs. Moreover, this OTP device offers the advantages of easy and effective program updates, using development and programming tools. User can avail of the ELAN Writer to easily program his development code.

2 Features

- CPU configuration
  - 1K - 13 bits on chip ROM
  - 32 - 8 bits on-chip registers (SRAM, general purpose)
  - 5 level stacks for subroutine nesting
  - Less than 1.5 mA at 5V/4MHz
  - Typically 15 ∝A, at 3V/32kHz
  - Typically 1 ∝A, during Sleep mode
- I/O port configuration
  - 2 bidirectional I/O ports : P5, P6
  - 12 I/O pins
  - Wake-up port : P6
  - 6 Programmable pull-down I/O pins
  - 7 programmable pull-high I/O pins
  - 7 programmable open-drain I/O pins
  - External interrupt : P60
- Operating voltage range:
  - OTP version:

  Operating voltage range: 2.3V~5.5V
- Operating temperature range: 0~70°C
- Operating frequency range (base on 2 clocks):
  - Crystal mode:

    DC~20MHz/2clks @ 5V; DC~100ns inst. cycle @ 5V
    DC~8MHz/2clks @ 3V; DC~250ns inst. cycle @ 3V
    DC~4MHz/2clks @ 2.3V; DC~500ns inst. cycle @ 2.3V
  - ERC mode:

    DC~4MHz/2clks @ 5V; DC~500ns inst. cycle @ 5V
    DC~4MHz/2clks @ 3V; DC~500ns inst. cycle @ 3V
    DC~4MHz/2clks @ 2.3V; DC~500ns inst. cycle @ 2.3V
  - IRC mode:

    Oscillation mode : 4MHz, 8MHz, 1MHz, 455kHz
    Process deviation : Typ ± 5.5%, Max ± 6%
    Temperature deviation : ±10% (0°C~70°C)

  The transient point of system frequency between HXT and LXT is 400kHz.
- Peripheral configuration
  - 8-bit real time clock/counter (TCC) with selective signal sources, trigger edges, and overflow interrupt
- Three available interrupts:
  - TCC overflow interrupt
  - Input-port status changed interrupt (wake-up from sleep mode)
  - External interrupt
- Special features
  - Programmable free running watchdog timer
  - Power saving Sleep mode
  - Selectable Oscillation mode
- Other features
  - Programmable prescaler of oscillator set-up time
  - One security register to prevent intrusion of user's OTP memory code
  - One configuration register to match user's requirement
  - Two clocks per instruction cycle
- Package type:
  - 14-pin DIP 300mil : BJ8P153C
  - 14-pin SOP 150mil : BJ8P153C

Note: Green products do not contain hazardous substances.

3 Pin Assignment

(1) 14-Pin
DIP/SOP

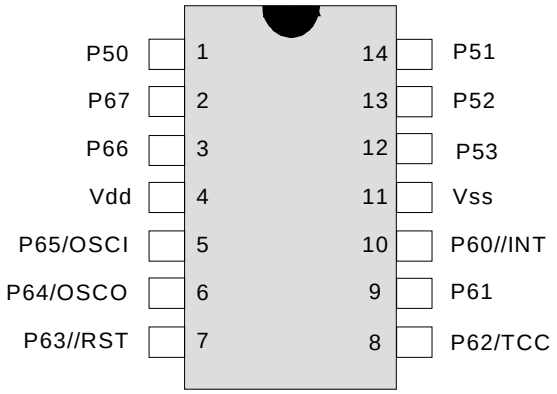


Fig. 3-1 BJ8P153C

4 Pin Description

BJ8P153C

Symbol	Pin No.	Type	Function
P66, P67	2, 3	I/O	General purpose input/output pin Pull-high open-drain Wake up from sleep mode when the status of the pin changes
P65/OSCI	5	I/O	General purpose input/output pin External clock signal input Input pin of XT oscillator Pull-high open-drain Wake up from sleep mode when the status of the pin changes
P64/OSCO	6	I/O	General purpose input/output pin External clock signal input Input pin of XT oscillator Pull-high open-drain Wake up from sleep mode when the status of the pin changes
P63//RESET	7	I	P63 is input pin only Internal Pull-high is on if defined as /RESET. If set as /RESET and remains at logic low, the device will be reset Wake-up from sleep mode when pin status changes Voltage on /RESET must not exceed Vdd during normal mode
P62/TCC	8	I/O	General purpose input/output pin External Timer/Counter input Pull-high/Pull-down open-drain Wake up from sleep mode when the status of the pin changes
P61	9	I/O	General purpose input/output pin Pull-high/Pull-down open-drain Wake up from sleep mode when the status of the pin changes Schmitt Trigger input during the programming mode
P60/INT	10	I/O	General purpose input/output pin Pull-high/Pull-down open-drain Wake up from sleep mode when the status of the pin changes Schmitt Trigger input during the programming mode External interrupt pin triggered by a falling edge
P50, P51~P52	1, 13~14	I/O	General purpose input/output pin Pull-down
P53	12	I/O	General purpose input/output pin
VDD	4	–	Power supply
VSS	11	–	Ground

5 Function Description

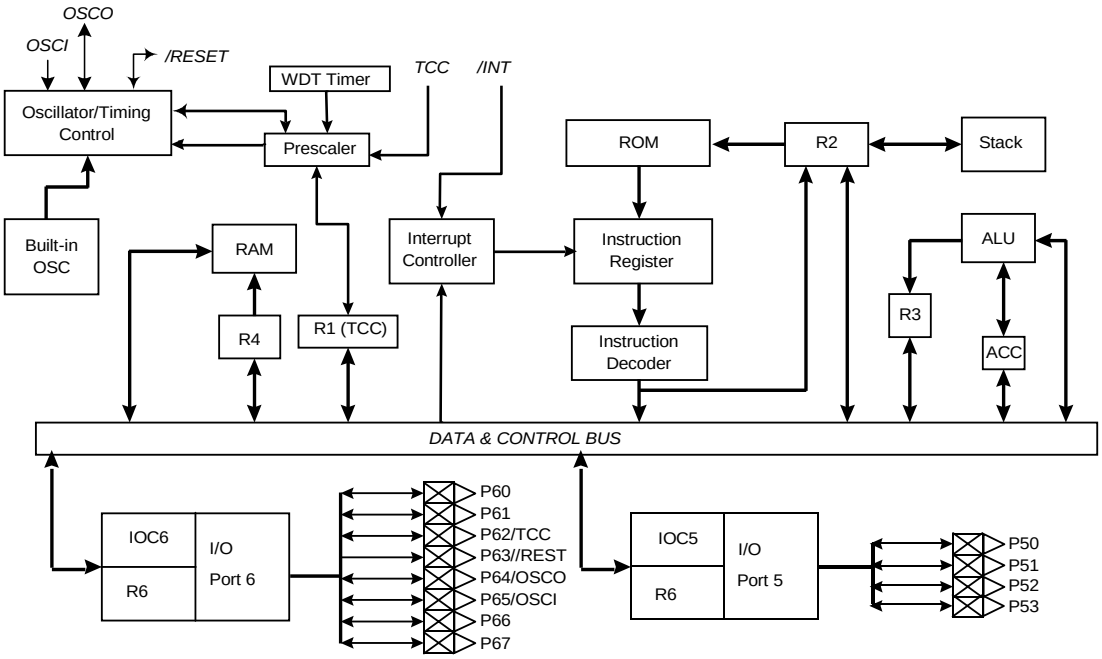


Fig. 5-1 BJ8P153C Functional Block Diagram

5.1 Operational Registers

5.1.1 R0 (Indirect Addressing Register)

R0 is not a physically implemented register. It is used as an indirect addressing pointer. Any instruction using R0 as a pointer actually accesses data pointed by the RAM Select Register (R4).

5.1.2 R1 (Timer Clock /Counter)

- Incremented by an external signal edge, which is defined by TE bit (CONT-4) through the TCC pin, or by the instruction cycle clock.
- Writable and readable as any other registers.
- Defined by resetting PAB (CONT-3).
- The prescaler is assigned to TCC, if the PAB bit (CONT-3) is reset.
- The contents of the prescaler counter will be cleared only when TCC register is written with a value.

5.1.3 R2 (Program Counter) & Stack

- Depending on the device type, R2 and hardware stack are 10-bit wide. The structure is depicted in the following figure.

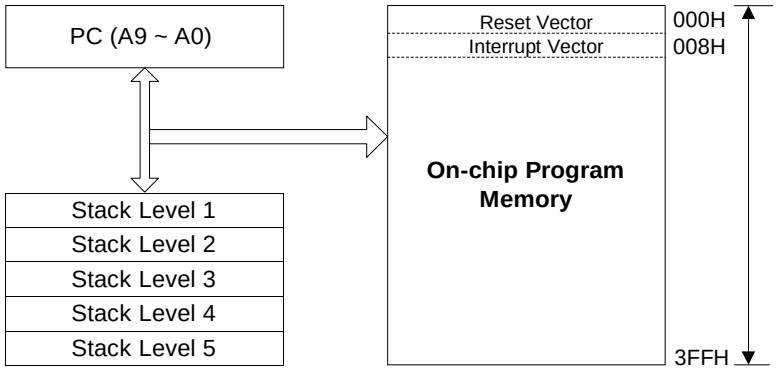


Fig 5-2 Program Counter Organization

- The configuration structure generates 1024*13 bits on-chip OTP ROM addresses to the relative programming instruction codes. One program page is 1024 words long.
- R2 is set as all "0" when under RESET condition.
- "JMP" instruction allows direct loading of the lower 10 program counter bits. Thus, "JMP" allows PC to go to any location within a page.
- "CALL" instruction loads the lower 10 bits of the PC, and then PC+1 is pushed into the stack. Thus, the subroutine entry address can be located anywhere within a page.
- "RET" ("RETLk", "RETI") instruction loads the program counter with the contents of the top-level stack.
- "ADD R2, A" allows a relative address to be added to the current PC, and the ninth and succeeding bits of the PC will increase progressively.
- "MOV R2, A" allows loading of an address from the "A" register to the lower 8 bits of the PC, and the ninth and tenth bits (A8 ~ A9) of the PC will remain unchanged.
- Any instruction written to R2 (e.g. “ADD R2,A”, "MOV R2, A", "BC R2, 6",[illegible]) will cause the ninth bit and the tenth bit (A8 ~ A9) of the PC to be cleared. Hence, the computed jump is limited to the first 256 locations of a page.
- All instructions are single instruction cycle (fclk/2 or fclk/4) except for instructions that would change the contents of R2. Such instructions will need one more instruction cycle.

■ The Data Memory Configuration is as follows:

Address	R PAGE Registers	IOC PAGE Registers
00	R0 (IAR)	Reserve
01	R1 (TCC)	CONT (Control Register)
02	R2 (PC)	Reserve
03	R3 (Status)	Reserve
04	R4 (RSR)	Reserve
05	R5 (Port 5)	IOC5 (I/O Port Control Register)
06	R6 (Port 6)	IOC6 (I/O Port Control Register)
07	Reserve	Reserve
08	Reserve	Reserve
09	Reserve	Reserve
0A	Reserve	Reserve
0B	Reserve	IOCB (Pull-down Register)
0C	Reserve	IOCC (Open-drain Control)
0D	Reserve	IOCD (Pull-high Control Register)
0E	Reserve	IOCE (WDT Control Register)
0F	RF (Interrupt Status)	IOCF (Interrupt Mask Register)
10 : 2F	General Registers	

Fig. 5-3 Data Memory Configuration

5.1.4 R3 (Status Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RST	GP1	GP0	T	P	Z	DC	C

Bit 0 (C): Carry flag

Bit 1 (DC): Auxiliary carry flag

Bit 2 (Z): Zero flag

Set to "1" if the result of an arithmetic or logic operation is zero.

Bit 3 (P): Power down bit

Set to “1” during power on or by a "WDTC" command; and reset to “0” by a "SLEP" command.

Bit 4 (T): Time-out bit

Set to “1” with the "SLEP" and "WDTC" commands, or during power up; and reset to “0” by WDT time-out.

Bits 5 ~6 (GP0 ~ GP1): General-purpose read/write bits

Bit 7 (RST): Bit for reset type

0 : Set to 0 if the device wakes up from other reset type

1 : Set to 1 if the device wakes up from sleep mode on a pin change

5.1.5 R4 (RAM Select Register)

Bits 7 ~ 6 are general-purpose read/write bits.

See the Data Memory Configuration in Fig. 5-3.

5.1.6 R5 ~ R6 (Port 5 ~ Port 6)

R5 and **R6** are I/O registers.

Only the lower 4 bits of R5 are available.

The upper 4 bits of R5 are fixed to 0.

P63 is input only.

5.1.7 RF (Interrupt Status Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	-	-	-	-	EXIF	ICIF	TCIF

Note: **" 1 "** means with interrupt request **" 0 "** means no interrupt occurs

Bit 0 (TCIF): TCC Overflow Interrupt Flag. Set when TCC overflows, reset by software.

Bit 1 (ICIF): Port 6 input status changed interrupt flag. Set when Port 6 input changes, reset by software.

Bit 2 (EXIF): External Interrupt Flag. Set by a falling edge on /INT pin, reset by software.

Bits 3 ~ 7: Not used.

RF can be cleared by instruction but cannot be set.

IOCF is the interrupt mask register.

NOTE

The result of reading RF is the "logic AND" of RF and IOCF.

5.1.8 R10 ~ R2F

These are all 8-bit general-purpose registers.

5.2 Special Function Registers

5.2.1 A (Accumulator)

Internal data transfer operation, or instruction operand holding usually involves the temporary storage function of the Accumulator, which is not an addressable register.

5.2.2 CONT (Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	/INT	TS	TE	PAB	PSR2	PSR1	PSR0

Bit 0 (PSR0) ~ Bit 2 (PSR2): TCC/WDT prescaler bits

PSR2	PSR1	PSR0	TCC Rate	WDT Rate
0	0	0	1:2	1:1
0	0	1	1:4	1:2
0	1	0	1:8	1:4
0	1	1	1:16	1:8
1	0	0	1:32	1:16
1	0	1	1:64	1:32
1	1	0	1:128	1:64
1	1	1	1:256	1:128

Bit 3 (PAB): Prescaler Assigned Bit

0 = TCC

1 = WDT

Bit 4 (TE): TCC signal edge

0 = increment if the transition from low to high takes place on the TCC pin

1 = increment if the transition from high to low takes place on the TCC pin

Bit 5 (TS): TCC signal source

0 = internal instruction cycle clock, P62 is a bidirectional I/O pin

1 = transition on TCC pin

Bit 6 (/INT): Interrupt enable flag

0 = masked by DISI or hardware interrupt

1 = enabled by ENI/RETI instructions

Bit 7: Not used

The CONT register is both readable and writable.

5.2.3 IOC5 ~ IOC6 (I/O Port Control Register)

0 = defines the relative I/O pin as output

1 = puts the relative I/O pin into high impedance

Only the lower 4 bits of IOC5 are available to be defined.

IOC5 and IOC6 registers are both readable and writable.

5.2.4 IOCB (Pull-down Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	/PD6	/PD5	/PD4	-	/PD2	/PD1	/PD0

Bit 0 (/PD0): Control bit used to enable the P50 pull-down pin.

0 = Enable internal pull-down

1 = Disable internal pull-down

Bit 1 (/PD1): Control bit used to enable the P51 pull-down pin

Bit 2 (/PD2): Control bit used to enable the P52 pull-down pin

Bit 3: Not used

Bit 4 (/PD4): Control bit used to enable the P60 pull-down pin

Bit 5 (/PD5): Control bit used to enable the P61 pull-down pin

Bit 6 (/PD6): Control bit used to enable the P62 pull-down pin

Bit 7: Not used

The IOCB Register is both readable and writable.

5.2.5 IOCC (Open-drain Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
OD7	OD6	OD5	OD4	-	OD2	OD1	OD0

Bit 0 (OD0): Control bit used to enable the P60 open-drain pin

0 = Disable open-drain output

1 = Enable open-drain output

Bit 1 (OD1): Control bit used to enable the P61 open-drain pin

Bit 2 (OD2): Control bit used to enable the P61 open-drain pin

Bits 3: Not used

Bit 4 (OD4): Control bit used to enable the P61 open-drain pin

Bit 5 (OD5): Control bit used to enable the P61 open-drain pin

Bit 6 (OD6): Control bit used to enable the P66 open-drain pin

Bit 7 (OD7): Control bit used to enable the P67 open-drain pin

The IOCC Register is both readable and writable.

5.2.6 IOCD (Pull-high Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
/PH7	/PH6	/PH5	/PH4	-	/PH2	/PH1	/PH0

Bit 0 (/PH0): Control bit used to enable the P60 pull-high pin

0 = Enable internal pull-high

1 = Disable internal pull-high

Bit 1 (/PH1): Control bit used to enable the P61 pull-high pin

Bit 2 (/PH2): Control bit is used to enable the pull-high function of P62 pin.

Bits 3: Not used

Bit 4 (/PH4): Control bit is used to enable the pull-high function of P64 pin.

Bit 5 (/PH5): Control bit is used to enable the pull-high function of P65 pin.

Bit 6 (/PH6): Control bit is used to enable the pull-high function of P66 pin.

Bit 7 (/PH7): Control bit is used to enable the pull-high function of P67 pin.

The IOCD Register is both readable and writable.

5.2.7 IOCE (WDT Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
WDTE	EIS	-	-	-	-	-	-

Bits 0~ 5: Not used

Bit 6 (EIS): Control bit is used to define the function of P60 (/INT) pin.

0 = P60, bidirectional I/O pin.

1 = /INT, external interrupt pin. In this case, the I/O control bit of P60 (Bit 0 of IOC6) must be set to "1."

When EIS is "0," the path of /INT is masked. When EIS is "1," the status of /INT pin can also be read by way of reading Port 6 (R6). See Figure 5-6 under Section 5.4 for reference.

EIS is both readable and writable.

Bit 7 (WDTE): Control bit used to enable the Watchdog timer.

0 = Disable WDT

1 = Enable WDT

WDTE is both readable and writable.

5.2.8 IOCF (Interrupt Mask Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	-	-	-	-	EXIE	ICIE	TCIE

Bit 0 (TCIE): TCIF interrupt enable bit

0 = disable TCIF interrupt

1 = enable TCIF interrupt

Bit 1 (ICIE): ICIF interrupt enable bit

0 = disable ICIF interrupt

1 = enable ICIF interrupt

Bit 2 (EXIE): EXIF interrupt enable bit

0 = disable EXIF interrupt

1 = enable EXIF interrupt

Bits 3~7: Not used

The IOCF register is both readable and writable.

5.3 TCC/WDT & Prescaler

There is an 8-bit counter available as prescaler for the TCC or WDT. The prescaler is available for the TCC only or the WDT only at the same time and the PAB bit of the CONT register is used to determine the prescaler assignment. The PSR0~PSR2 bits determine the ratio. The prescaler is cleared each time the instruction is written to TCC under TCC mode. The WDT and prescaler, when assigned to WDT mode, are cleared by the "WDTC" or "SLEP" instructions. Fig. 5-4 depicts the circuit diagram of TCC/WDT.

- R1 (TCC) is an 8-bit timer/counter. The clock source of TCC can be internal or external clock input (edge selectable from TCC pin). If TCC signal source is from internal clock, TCC will increase by 1 at every instruction cycle (without prescaler). Referring to Fig. 5-4, CLK=Fosc/2 or CLK=Fosc/4, depends on the Code Option bit CLK. CLK=Fosc/2 is used if CLK bit is "0", and CLK=Fosc/4 is used if CLK bit is "1". If TCC signal source is from external clock input, TCC is incremented by 1 at every falling edge or rising edge of TCC pin.
- The watchdog timer is a free running on-chip RC oscillator. The WDT will keep running even when the oscillator driver has been turned off (i.e. in sleep mode). During normal operation or sleep mode, a WDT time-out (if enabled) will cause the device to reset. The WDT can be enabled or disabled any time during normal mode by software programming. Refer to WDTE bit of the IOCE register. Without prescaler, the WDT time-out period is approximately 18 ms[1] (default).

5.4 I/O Ports

The I/O registers, both Port 5 and Port 6, are bidirectional tri-state I/O ports. Port 6 can be pulled-high internally by software except P63. In addition, Port 6 can also have open-drain output by software except P63. Input status changed interrupt (or wake-up) function is available from Port 6. P50 ~ P52 and P60 ~ P62 pins can be pulled-down by software. Each I/O pin can be defined as "input" or "output" pin by the I/O control register (IOC5 ~ IOC6) except P63. The I/O registers and I/O control registers are both readable and writable. The I/O interface circuits for Port 5 and Port 6 are shown in Fig. 5-5, Fig. 5-6 and Fig. 5-7 respectively.

[1] **Note: Vdd = 5V, set up time period = 16.5ms ± 30%**
Vdd = 3V, set up time period = 18ms ± 30%

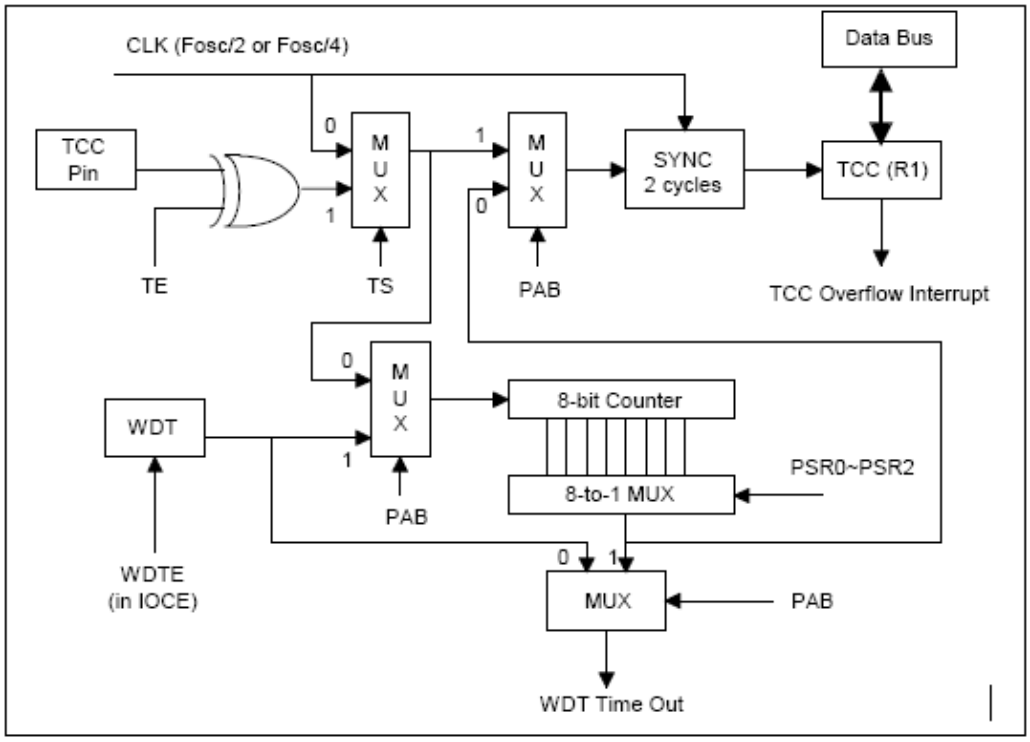
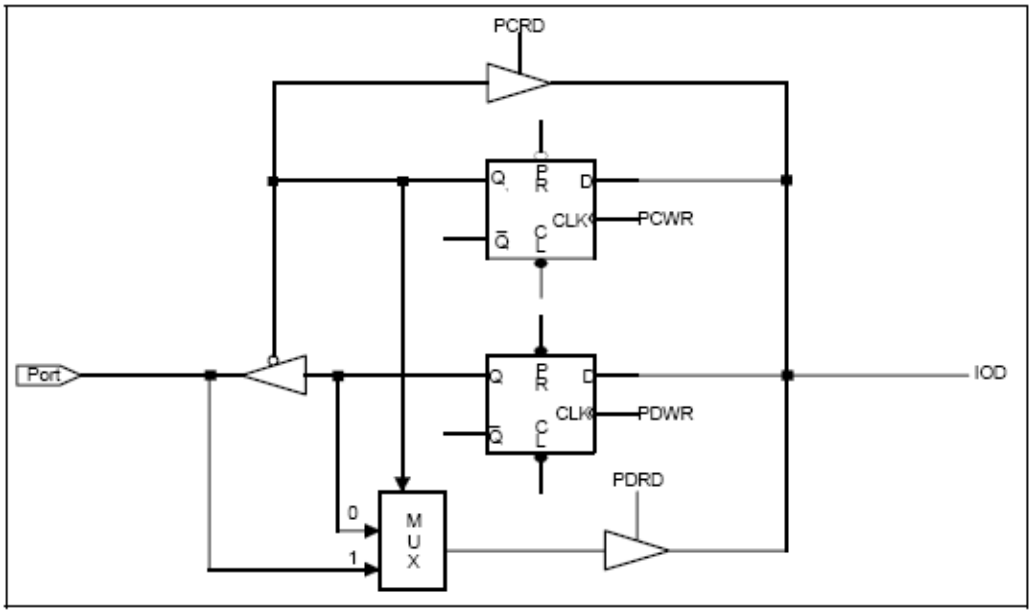
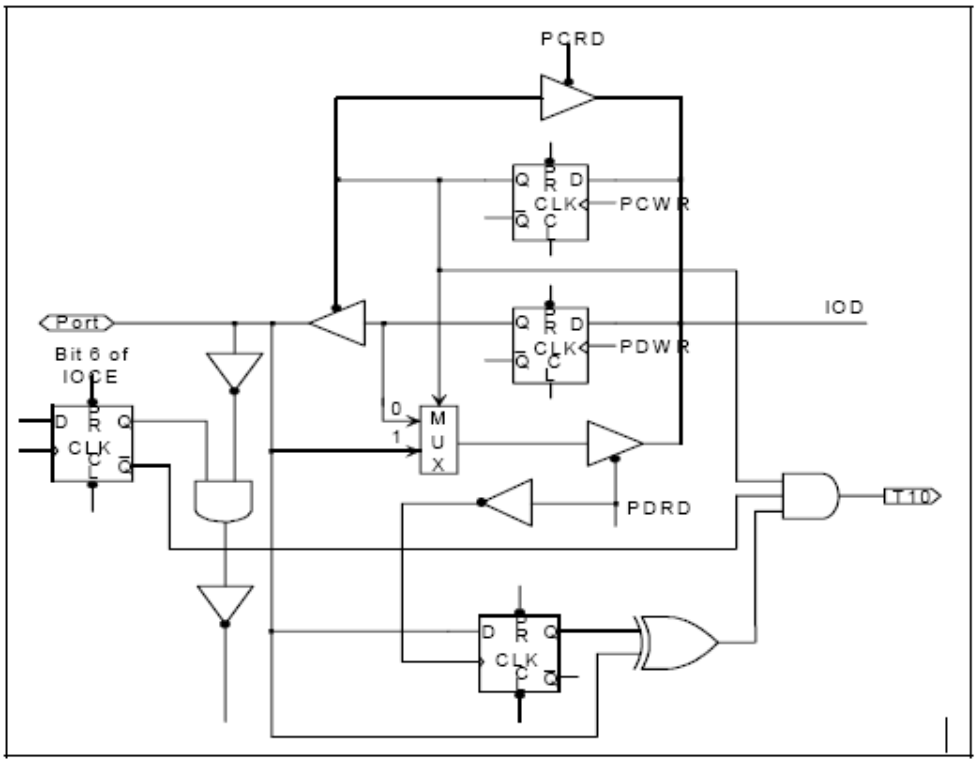


Fig. 5-4 TCC and WDT Block Diagram



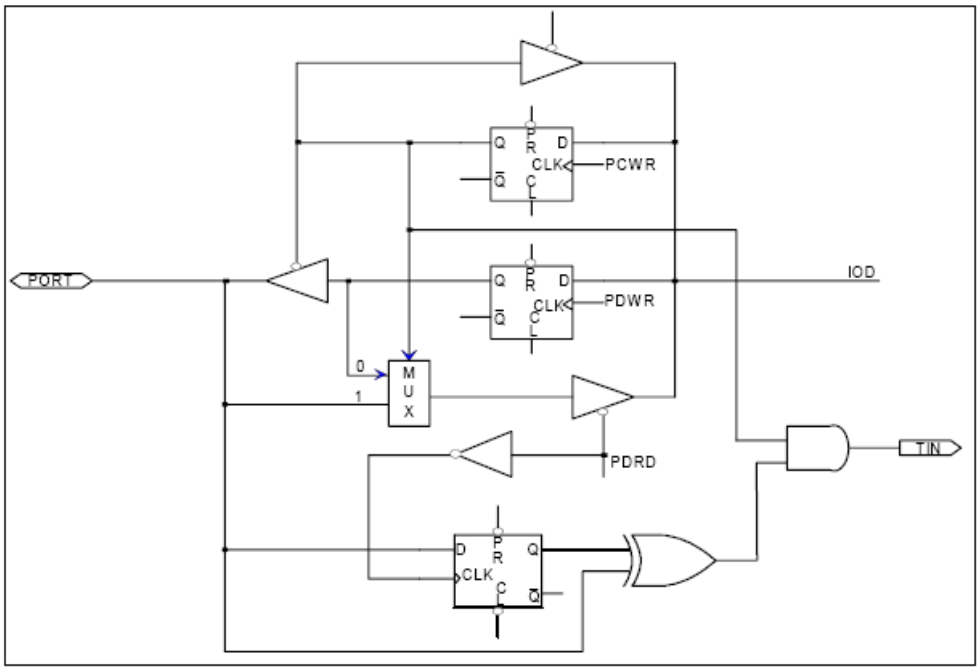
Note: Pull-down is not shown in the figure.

Fig. 5-5 I/O Port and I/O Control Register Circuit for Port 5



Note: Pull-high (down) and open-drain are not shown in the figure.

Fig 5-6 I/O Port and I/O Control Register Circuit for P60 (/INT)



Note: Pull-high (down) and open-drain are not shown in the figure.

Fig. 5-7 I/O Port and I/O Control Register Circuit for P61~P67

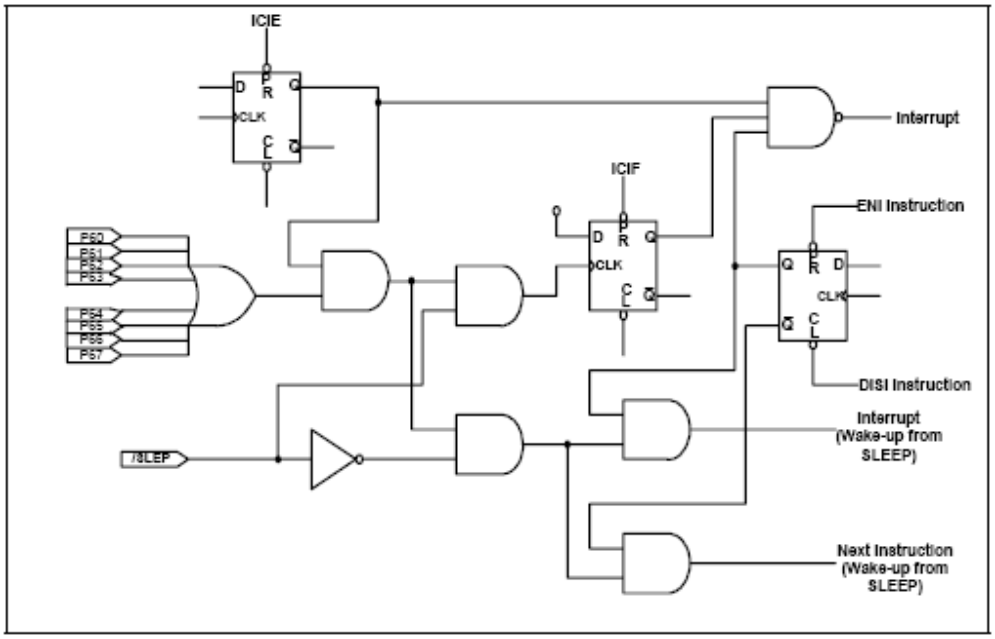


Fig. 5-8 Block Diagram of I/O Port 6 with input change interrupt/wake-up

Table 1 Usage of Port 6 Input Change Wake-up/Interrupt Function

Usage of Port 6 Input Status Change Wake-up/Interrupt	
(I) Wake-up from Port 6 Input Status Change (a) Before Sleep 1. Disable WDT 2. Read I/O Port 6 (MOV R6,R6) 3. Execute "ENI" or "DISI" 4. Enable interrupt (Set IOCF.1) 5. Execute "SLEP" instruction (b) After Wake-up 1. IF "ENI" → Interrupt vector (008H) 2. IF "DISI" → Next instruction	(II) Port 6 Input Status Change Interrupt 1. Read I/O Port 6 (MOV R6,R6) 2. Execute "ENI" 3. Enable interrupt (Set IOCF.1) 4. IF Port 6 change (interrupt) → Interrupt vector (008H)

5.5 Reset and Wake-up

5.5.1 Reset

A Reset is initiated by one of the following events:

1) Power on reset

2) /RESET pin input "low"

3) WDT time-out (if enabled)

The device is kept under reset condition for a period of approximately 18ms[2] (one oscillator start-up timer period) after a reset is detected. Once a Reset occurs, the following functions are performed**:**

- The oscillator is running, or will be started.
- The Program Counter (R2) is set to all "0."
- All I/O port pins are configured as input mode (high-impedance state)
- The Watchdog timer and prescaler are cleared.
- When power is switched on, the upper 3 bits of R3 are cleared.
- The bits of the CONT register are set to all "1" except for Bit 6 (INT flag).
- The bits of the IOCB register are set to all "1."
- The IOCC register is cleared.
- The bits of the IOCD register are set to all "1."
- Bit 7 of the IOCE register is set to "1," and Bits 4 and 6 are cleared.
- Bits 0 ~ 2 of RF and Bits 0 ~ 2 of IOCF registers are cleared.

The Sleep (power down) mode is asserted by executing the “SLEP” instruction. While entering Sleep mode, WDT (if enabled) is cleared but keeps on running. The controller can be awakened by-

1) External reset input on /RESET pin,

2) WDT time-out (if enabled)

3) Port 6 input status change (if enabled)

The first two cases will cause the BJ8P153C to reset. The T and P flags of R3 are used to determine the source of the reset (wake-up). The last case is considered the continuation of program execution and the global interrupt ("ENI" or "DISI" being executed) decides whether or not the controller branches to the interrupt vector

[2] **Vdd = 5V, set up time period = 16.8ms ± 30%**
Vdd = 3V, set up time period = 18ms ± 30%

following a wake-up. If ENI is executed before SLEP, the instruction will begin to execute from the address 008H after wake-up. If DISI is executed before SLEP, the operation will restart from the succeeding instruction right next to SLEP after a wake-up.

Only one of Cases 2 and 3 can be enabled before going into the Sleep mode. That is,

[a] if Port 6 Input Status Change Interrupt is enabled before SLEP, WDT must be disabled by software. However, the WDT bit in the option register remains enabled. Hence, the BJ8P153C can be awakened only by Case 1 or Case 3.

[b] if WDT is enabled before SLEP, Port 6 Input Status Change Interrupt must be disabled. Hence, the BJ8P153C can be awakened only by Case 1 or Case 2. Refer to Section 5.6, *Interrupt* for further details.

If Port 6 Input Status Change Interrupt is used to wake-up the BJ8P153C (Case [a] above), the following instructions must be executed before SLEP:

```
MOV A, @xxxx1110b     ; Select the WDT prescaler, it must be
                        set over 1:1
CONTW
WDTC                  ; Clear WDT and prescaler
MOV A, @0xxxxxxxb     ; Disable WDT
IOW RE
MOV R6, R6            ; Read Port 6
MOV A, @00000x1xb     ; Enable Port 6 input change interrupt
IOW RF
ENI (or DISI)        ; Enable (or disable) global interrupt
SLEP                  ; Sleep
```

NOTE

1. *After waking up from sleep mode, WDT is automatically enabled. The WDT enable/disable operation after waking up from sleep mode should be appropriately defined in the software.*
2. *To avoid a reset from occurring when the Port 6 Input Status Changed Interrupt enters into interrupt vector or is used to wake-up the MCU, the WDT prescaler must be set above the 1:1 ratio.*

5.5.2 Summary of Registers Initialized Values

Address	Name	Reset Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2		
N/A	IOC5	Bit Name	-	-	-	-	C53	C52	C51	C50
		Power-on	0	0	0	0	1	1	1	1
		/RESET and WDT	0	0	0	0	1	1	1	1
		Wake-up from Pin Change	0	0	0	0	P	P	P	P
N/A	IOC6	Bit Name	C67	C66	C65	C64	C63	C62	C61	C60
		Power-on	1	1	1	1	1	1	1	1
		/RESET and WDT	1	1	1	1	1	1	1	1
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0x05	P5	Bit Name	-	-	-	-	P53	P52	P51	P50
		Power-on	1	1	1	1	1	1	1	1
		/RESET and WDT	P	P	P	P	P	P	P	P
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0x06	P6	Bit Name	P67	P66	P65	P64	P63	P62	P61	P60
		Power-on	1	1	1	1	1	1	1	1
		/RESET and WDT	P	P	P	P	P	P	P	P
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
N/A	CONT	Bit Name	-	/INT	TS	TE	PAB	PSR2	PSR1	PSR0
		Power-on	1	0	1	1	1	1	1	1
		/RESET and WDT	1	0	1	1	1	1	1	1
		Wake-up from Pin Change	P	0	P	P	P	P	P	P
0x00	R0 (IAR)	Bit Name	-	-	-	-	-	-	-	-
		Power-on	U	U	U	U	U	U	U	U
		/RESET and WDT	P	P	P	P	P	P	P	P
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0x01	R1 (TCC)	Bit Name	-	-	-	-	-	-	-	-
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0x02	R2 (PC)	Bit Name	-	-	-	-	-	-	-	-
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	N	P	P	P
0x03	R3 (SR)	Bit Name	RST	GP1	GP0	T	P	Z	DC	C
		Power-on	0	0	0	1	1	U	U	U
		/RESET and WDT	0	0	0	*	*	P	P	P
		Wake-up from Pin Change	1	P	P	*	*	P	P	P
0x04	R4 (RSR)	Bit Name	GP1	GP0	-	-	-	-	-	-
		Power-on	U	U	U	U	U	U	U	U
		/RESET and WDT	P	P	P	P	P	P	P	P
		Wake-up from Pin Change	P	P	P	P	P	P	P	P

Address	Name	Reset Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1
0x0F	RF(ISR)	Bit Name	-	-	-	-	-	EXIF	ICIF	TCIF
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	0	0	0	0	0	P	N	P
0x0B	IOCB	Bit Name	-	/PD6	/PD5	/PD4	/PD3	/PD2	/PD1	/PD0
		Power-on	1	1	1	1	1	1	1	1
		/RESET and WDT	1	1	1	1	1	1	1	1
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0x0C	IOCC	Bit Name	OD7	OD6	OD5	OD4	-	OD2	OD1	OD0
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0x0D	IOCD	Bit Name	/PH7	/PH6	/PH5	/PH4	-	/PH2	/PH1	/PH0
		Power-on	1	1	1	1	1	1	1	1
		/RESET and WDT	1	1	1	1	1	1	1	1
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0x0E	IOCE	Bit Name	WDTE	EIS	-	-	-	-	-	-
		Power-on	1	0	1	1	1	1	1	1
		/RESET and WDT	1	0	1	1	1	1	1	1
		Wake-up from Pin Change	1	P	1	1	1	1	1	1
0x0F	IOCF	Bit Name	-	-	-	-	-	EXIE	ICIE	TCIE
		Power-on	1	1	1	1	1	0	0	0
		/RESET and WDT	1	1	1	1	1	0	0	0
		Wake-up from Pin Change	1	1	1	1	1	P	P	P
0x10~0x2F	R10~R2F	Bit Name	-	-	-	-	-	-	-	-
		Power-on	U	U	U	U	U	U	U	U
		/RESET and WDT	P	P	P	P	P	P	P	P
		Wake-up from Pin Change	P	P	P	P	P	P	P	P

Legend: **-:** Not used **U:** Unknown or don't care **P:** Previous value before reset

* Refer to tables provided in the next section (Section 5.5.3).

5.5.3 Status of RST, T, and P of the Status Register

A Reset condition is initiated by the following events

1) A power-on condition

2) A high-low-high pulse on /RESET pin

3) Watchdog timer time-out

The values of T and P listed in the table below are used to check how the processor wakes up.

Table 2 Values of RST, T, and P after a Reset

Reset Type	RST	T	P
Power on	0	1	1
/RESET during Operating mode	0	*P	*P
/RESET wake-up during Sleep mode	0	1	0
WDT during Operating mode	0	0	*P
WDT wake-up during Sleep mode	0	0	0
Wake-Up on pin change during Sleep mode	1	1	0

* ***P:*** *Previous status before reset*

The following table shows the events that may affect the status of T and P.

Table 3 Status of T and P Being Affected by Events

Event	RST	T	P
Power on	0	1	1
WDTC instruction	*P	1	1
WDT time-out	0	0	*P
SLEP instruction	*P	1	0
Wake-up on pin change during Sleep mode	1	1	0

* ***P:*** *Previous status before reset*

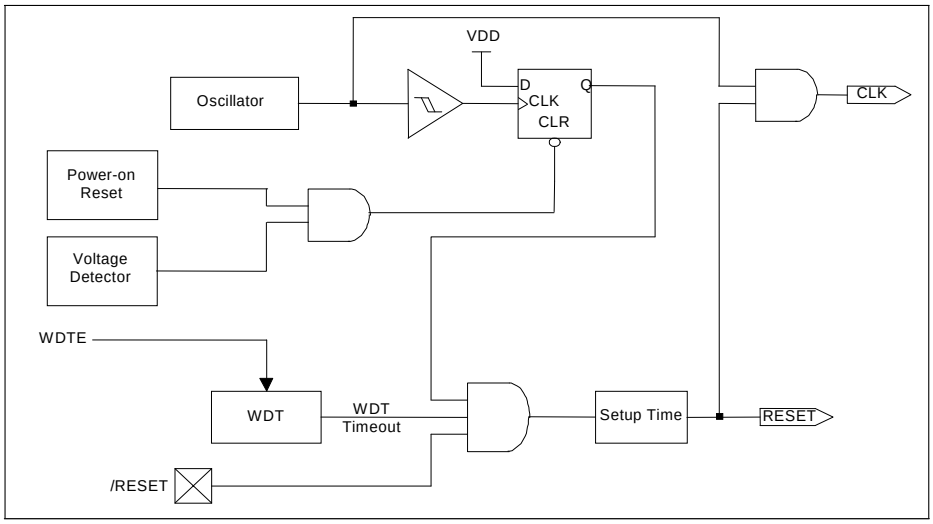


Figure 5-9 Controller Reset Block Diagram

5.6 Interrupt

The BJ8P153C has three falling-edge interrupts as listed herewith**:**

1) TCC overflow interrupt

2) Port 6 Input Status Change Interrupt

3) External interrupt [(P60, /INT) pin]

Before the Port 6 Input Status Changed Interrupt is enabled, reading Port 6 (e.g. "MOV R6,R6") is necessary. Each pin of Port 6 will have this feature if its status changes. Any pin configured as output or P60 pin configured as /INT, is excluded from this function. The Port 6 Input Status Changed Interrupt can wake up the BJ8P153C from Sleep mode if Port 6 is enabled prior to going into Sleep mode by executing SLEP instruction. When the chip wakes-up, the controller will continue to execute the program in-line if the global interrupt is disabled. If the global interrupt is enabled, it will branch to the interrupt vector 008H.

RF is the interrupt status register that records the interrupt requests in the relative flags/bits. IOCF is an interrupt mask register. The global interrupt is enabled by the ENI instruction and is disabled by the DISI instruction. When one of the interrupts (enabled) occurs, the next instruction will be fetched from address 008H. Once in the interrupt service routine, the source of an interrupt can be determined by polling the flag bits in RF. The interrupt flag bit must be cleared by instructions before leaving the interrupt service routine before interrupts are enabled to avoid recursive interrupts.

The flag (except ICIF bit) in the Interrupt Status Register (RF) is set regardless of the status of its mask bit or the execution of ENI. Note that the outcome of RF will be the logic AND of RF and IOCF (refer to Fig. 5-10). The RETI instruction ends the interrupt routine and enables the global interrupt (the execution of ENI).

When an interrupt is generated by the INT instruction (enabled), the next instruction will be fetched from address 001H.

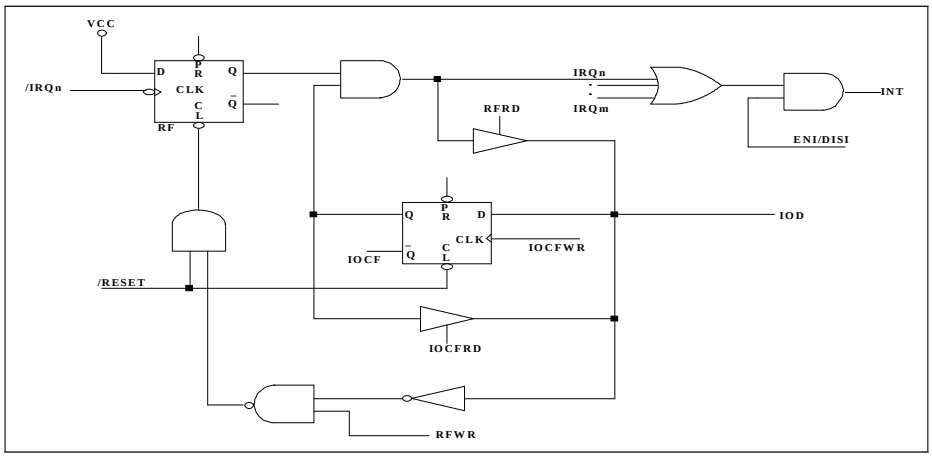


Figure 5-7 Interrupt Input Circuit

5.7 Oscillator

5.7.1 Oscillator Modes

The BJ8P153C can be operated in four different oscillator modes, such as External RC oscillator mode (ERC), Internal RC oscillator mode (IRC), High Crystal oscillator mode (HXT), and Low Crystal oscillator mode (LXT). The desired mode can be selected by programming OSC1 and OSC2 in the Code Option register. The Table below describes how these four oscillator modes are defined.

Table 4 Oscillator Modes Defined by OSC

Mode	OSC1	OSC2
IRC (Internal RC oscillator mode)	1	1
ERC (External RC oscillator mode)	1	0
HXT (High Crystal oscillator mode)	0	1
LXT(Low Crystal oscillator mode)	0	0

Note: The transient point of system frequency between HXT and LXY is 400kHz.

The maximum operational frequency of the crystal/resonator under different VDDs is as listed below.

Table 5 Summary of Maximum Operating Speeds

Conditions	VDD	Max Freq. (MHz)
Two cycles with two clocks	2.3	4.0
	3.0	8.0
	5.0	20.0

5.7.2 Crystal Oscillator/Ceramic Resonators (Crystal)

The BJ8P153C can be driven by an external clock signal through the OSCI pin as shown in the following figure.

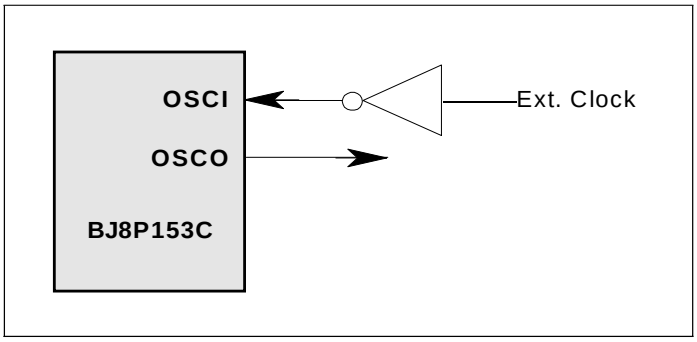


Fig. 5-11 Circuit for External Clock Input

In most applications, pin OSCI and pin OSCO can be connected with a crystal or ceramic resonator to generate oscillation. Fig. 5-12 depicts such circuit. The same thing applies whether it is in the HXT mode or in the LXT mode.

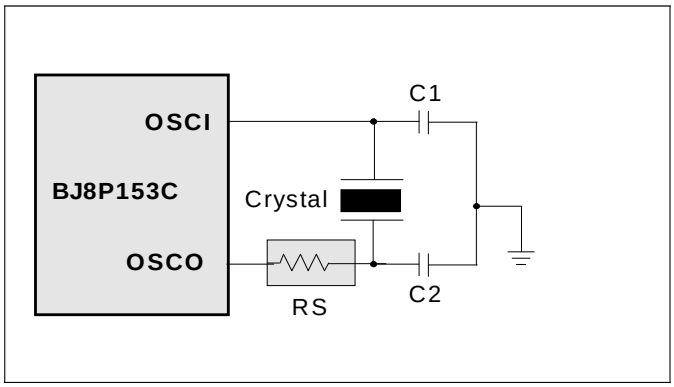


Fig. 5-12 Circuit for Crystal/Resonator

The following table provides the recommended values of C1 and C2. Since each resonator has its own attribute, refer to its specification for appropriate values of C1 and C2. RS, a serial resistor, may be necessary for AT strip cut crystal or low frequency mode.

Table 6 Capacitor Selection Guide for Crystal Oscillator or Ceramic Resonator

Oscillator Type	Frequency Mode	Frequency	C1 (pF)	C2 (pF)
Ceramic Resonators	HXT	455kHz	100~150	100~150
		2.0 MHz	20~40	20~40
		4.0 MHz	10~30	10~30
Crystal Oscillator	LXT	32.768kHz	25	15
		100kHz	25	25
		200kHz	25	25
	HXT	455kHz	20~40	20~150
		1.0MHz	15~30	15~30
		2.0MHz	15	15
		4.0MHz	15	15

Note: The values of capacitors C1 and C2 are for reference only

5.7.3 External RC Oscillator Mode

For some applications that do not require a very precise timing calculation, the RC oscillator (Fig 5-15) offers a cost-effective oscillator configuration. Nevertheless, it should be noted that the frequency of the RC oscillator is influenced by the supply voltage, the values of the resistor (Rext), the capacitor (Cext), and even by the
operation temperature. Moreover, the frequency also changes slightly from one chip to another due to manufacturing process variations.

In order to maintain a stable system frequency, the values of the Cext should not be less than 20pF, and that the value of Rext should not be greater than 1 M&. If they cannot be kept in this range, the frequency can be easily affected by noise, humidity, and leakage.

The smaller the Rext in the RC oscillator is, the faster its frequency will be. On the contrary, for very low Rext values, for instance, 1 K&, the oscillator becomes unstable because the NMOS cannot discharge the current of the capacitance correctly.

Based on the above reasons, it must be kept in mind that all of the supply voltage, the operation temperature, the components of the RC oscillator, the package types, the way the PCB is layout, will affect the system frequency.

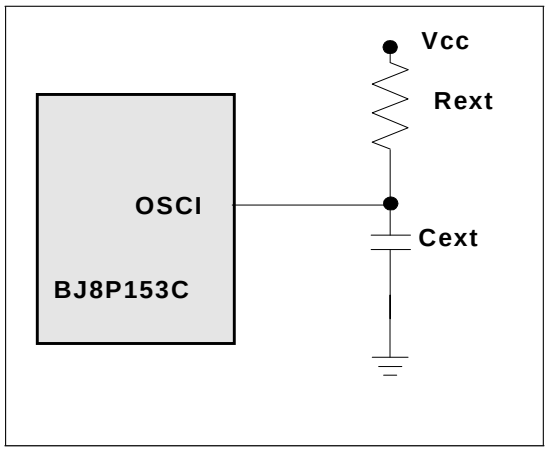


Figure 5-13 External RC Oscillator Mode Circuit

Table 7 RC Oscillator Frequencies

Cext	Rext	Average Fosc 5V, 25°C	Average Fosc 3V, 25°C
20 pF	3.3k	3.92 MHz	3.65 MHz
	5.1k	2.67 MHz	2.60 MHz
	10k	1.4MHz	1.40 MHz
	100k	150 kHz	156 kHz
100 pF	3.3k	1.4 MHz	1.33 MHz
	5.1k	940 kHz	917 kHz
	10k	476 kHz	480 kHz
	100k	50 kHz	52 kHz
300 pF	3.3k	595 kHz	570 kHz
	5.1k	400 kHz	384 kHz
	10k	200 kHz	203 kHz
	100k	20.9 kHz	20 kHz

Note: 1: Measured based on DIP packages.
2: The values are for design reference only.
3: The frequency drift is ± 30%.

5.7.4 Internal RC Oscillator Mode

BJ8P153C offers a versatile internal RC mode with default frequency value of 4MHz. The Internal RC oscillator mode has other frequencies (1MHz, 8MHz, & 455kHz) that can be set by Code Option (Word 1), RCM1, and RCM0. All these four main frequencies can be calibrated by programming the Option Bits CAL0 ~ CAL2. The table below describes the BJ8P153C internal RC drift with variation of voltage, temperature, and process.

Table 8 Internal RC Drift Rate (Ta=25°C, VDD=5VÔ5%, VSS=0V)

Internal RC	Drift Rate			
	Temperature (0°C~70°C)	Voltage (2.3V~5.5V)	Process	Total
8MHz	± 3%	± 5%	± 10%	± 18%
4MHz	± 3%	± 5%	± 5%	± 13%
1MHz	± 3%	± 5%	± 10%	± 18%
455kHz	± 3%	± 5%	± 10%	± 18%

Note: These are theoretical values provided for reference only. Actual values may vary depending on the actual process.

5.8 Code Option Register

The BJ8P153C has a Code Option word that is not a part of the normal program memory. The option bits cannot be accessed during normal program execution.

■ **Code Option Register and Customer ID Register Arrangement Distribution:**

Word 0	Word 1	Word 2
Bit 12 ~ Bit 0	Bit 12 ~ Bit 0	Bit 12 ~ Bit 0

5.8.1 Code Option Register (Word 0)

Word 0												
Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit
/RESET	/ENWDT	CLKS	OSC1	OCS0	CS	SUT1	SUT0	TYPE	RCOUT	C2	C1	C0

Bit 12 (/RESET): Define Pin 7 as a reset pin

0 : /RESET enable

1 : /RESET disable

Bit 11 (/ENWTD): Watchdog timer enable bit

0 : Enable

1 : Disable

Note

This bit must be enabled and the WDTE reg. (IOCE reg. Bit 6) must be disabled when Port 6 pin change wake-up function is used.

Bit 10 (CLKS): Instruction period option bit.

0 : two oscillator periods.

1 : four oscillator periods.

Refer to the Instruction Set section.

Bit 9 and Bit 8 (OSC1 and OSC0): Oscillator Modes Selection bits.

Table 9 Oscillator Modes defined by OSC1 and OSC0

Mode	OSC1	OSC0
IRC (Internal RC oscillator mode)	1	1
ERC (External RC oscillator mode)	1	0
HXT (High Crystal oscillator mode)	0	1
LXT (Low Crystal oscillator mode)	0	0

Note: The transient point of system frequency between HXT and LXY is 400kHz.

Bit 7 (CS): Code Security Bit

0 : Security On

1 : Security Off

Bit 6 and Bit 5 (SUT1 and SUT0): Set-up Time of device bits.

Table 10 Set-up Time of Device Programming

SUT1	SUT0	*Set-up Time
1	1	18 ms
1	0	4.5 ms
0	1	288 ms
0	0	72 ms

* Theoretical values, for reference only

Bit 4 (Type): Type selection for BJ8P153C

TYPE	Series
0	BJ8P153C
1	-

Bit 3 (RCOUT): Selection bit of Oscillator output or I/O port

RCOUT	Pin Function
0	P64
1	OSCO

Bits 2~ 0 (C2~C 0): Calibrator of internal RC mode Bit 3

C2, C1, C0 must be set to “1” only.

■Code Option Register (Word 1)

Word 1	
Bit 1	Bit 0
RCM1	RCM0

Bit 1 and Bit 0 (RCM1, RCM0): RC mode selection bits

RCM 1	RCM 0	*Frequency (MHz)
1	1	4
1	0	8
0	1	1
0	0	455kHz

■ Customer ID Register (Word 2)

Bit 12~Bit 0
XXXXXXXXXXXX

Bits 12~ 0: Customer’s ID code

5.9 Power-on Considerations

Any microcontroller is not guaranteed to start to operate properly before the power supply stabilizes at its steady state. Under customer application, when power is OFF, Vdd must drop to below 1.8V and remains OFF for 10μs before power can be switched ON again. This way, the BJ8P153C will reset and operates normally. The extra external reset circuit will work well if Vdd can rise at very fast speed (50 ms or less). However, under most cases where critical applications are involved, extra devices are required to assist in solving the power-up problems.

5.10 Programmable Oscillator Set-Up Time

The Option word contains SUT0 and SUT1 which can be used to define the oscillator set-up time. Theoretically, the range is from 4.5 ms to 72 ms. For most of crystal or ceramic resonators, the lower the operation frequency is, the longer the Set-up time may be required. Table 12 describes the values of the Oscillator Set-up Time.

5.11 External Power-on Reset Circuit

The circuit shown in the figure implements an external RC to produce the reset pulse. The pulse width (time constant) should be kept long enough for Vdd to reach minimum operation voltage. This circuit is used when the power supply has a slow rise time. Since the current leakage from the /RESET pin is about ±5∝A, it is recommended that R should not be greater than 40K. In this way, the /RESET pin voltage is held below 0.2V. The diode (D) acts as a short circuit at the moment of power down. The capacitor C will discharge rapidly and fully. Rin, the current-limited resistor, will prevent high current or ESD (electrostatic discharge) from flowing to pin /RESET.

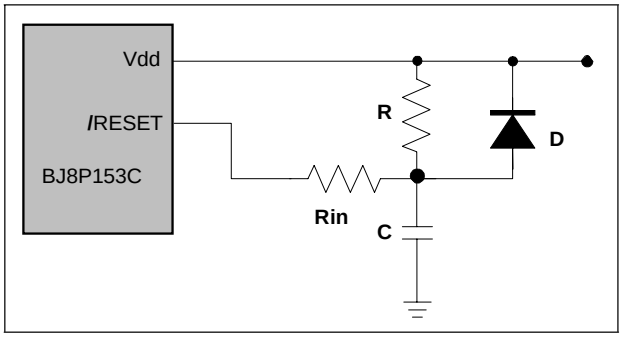


Fig 5-14 External Power-up Reset Circuit

5.12 Residue-Voltage Protection

When the battery is replaced, the device power (Vdd) is cut off but residue-voltage remains. The residue-voltage may trip below the minimum Vdd, but not to zero. This condition may cause a poor power-on reset. The following figures illustrate two recommended methods on how to build a residue-voltage protection circuit for BJ8P153C.

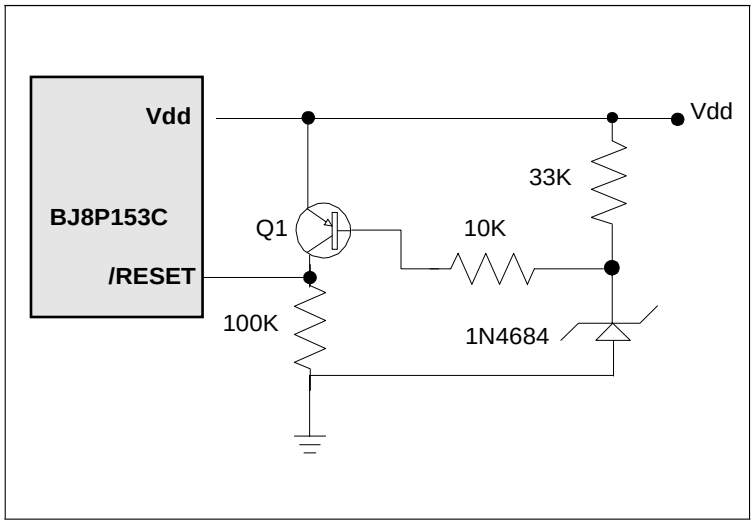


Fig. 5-15 Residue Voltage Protection Circuit 1

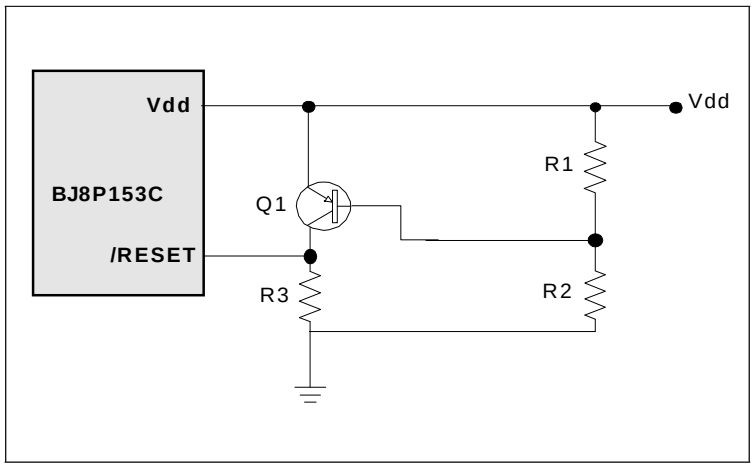


Fig.5-16 Residue Voltage Protection Circuit 2

5.13 Instruction Set

Each instruction in the instruction set is a 13-bit word divided into an OP code and one or more operands. Normally, all instructions are executed within one single instruction cycle (one instruction consists of two oscillator periods), unless the program counter is changed by instruction "MOV R2,A", "ADD R2,A", or by instructions of arithmetic or
logic operation on R2 (e.g., "SUB R2,A", "BS(C) R2,6", "CLR R2", ···). In this case, the execution takes two instruction cycles.

If for some reasons, the specification of the instruction cycle is not suitable for certain applications, try modifying the instruction as follows**:**

A) Modify one instruction cycle to consist of four oscillator periods.

B) "JMP," "CALL," "RET," "RETL," "RETI," or the conditional skip ("JBS," "JBC," "JZ," "JZA," "DJZ," "DJZA") commands which were tested to be true, are executed within two instruction cycles. The instructions that are written to the program counter also take two instruction cycles.

Case (A) is selected by the Code Option bit, called CLK. One instruction cycle consists of two oscillator clocks if CLK is low; and four oscillator clocks if CLK is high.

Note that once the four oscillator periods within one instruction cycle is selected as in Case (A), the internal clock source to TCC should be CLK=Fosc/4, instead of Fosc/2.

Moreover, the instruction set has the following features**:**

1) Every bit of any register can be set, cleared, or tested directly.

2) The I/O register can be regarded as general register. That is, the same instruction can operate on I/O register.

The following symbols are used in the Instruction Set table**:**

Convention:

R = Register designator that specifies which one of the registers (including operation and general purpose registers) is to be utilized by the instruction.
Bits 6 and 7 in R4 determine the selected register bank.

b = Bit field designator that selects the value for the bit located in the register R and which affects the operation.

k = 8 or 10-bit constant or literal value

Binary Instruction	Hex	Mnemonic	Operation	Status Affected
0 0000 0000 0000	0000	NOP	No Operation	None
0 0000 0000 0001	0001	DAA	Decimal Adjust A	C
0 0000 0000 0010	0002	CONTW	A→CONT	None
0 0000 0000 0011	0003	SLEP	0→WDT, Stop oscillator	T, P
0 0000 0000 0100	0004	WDTC	0→WDT	T, P
0 0000 0000 rrrr	000r	IOW R	A→IOCR	None [1]

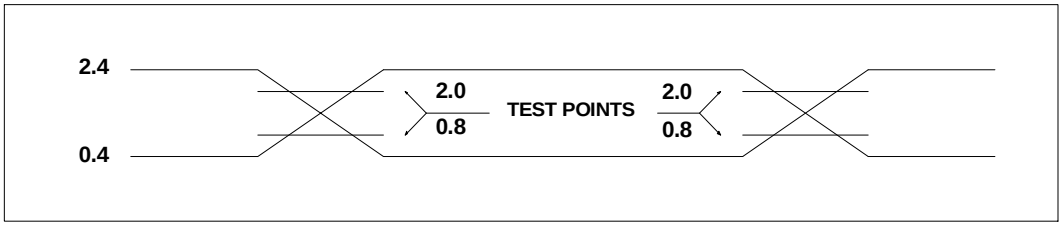
Binary Instruction	Hex	Mnemonic	Operation	Status Affected
0 0000 0001 0000	0010	ENI	Enable Interrupt	None
0 0000 0001 0001	0011	DISI	Disable Interrupt	None
0 0000 0001 0010	0012	RET	[Top of Stack] → PC	None
0 0000 0001 0011	0013	RETI	[Top of Stack] →PC, Enable Interrupt	None
0 0000 0001 0100	0014	CONTR	CONT → A	None
0 0000 0001 rrrr	001r	IOR R	IOCR → A	None [1]
0 0000 01rr rrrr	00rr	MOV R,A	A → R	None
0 0000 1000 0000	0080	CLRA	0 → A	Z
0 0000 11rr rrrr	00rr	CLR R	0 → R	Z
0 0001 00rr rrrr	01rr	SUB A,R	R-A → A	Z, C, DC
0 0001 01rr rrrr	01rr	SUB R,A	R-A → R	Z, C, DC
0 0001 10rr rrrr	01rr	DECA R	R-1 → A	Z
0 0001 11rr rrrr	01rr	DEC R	R-1 → R	Z
0 0010 00rr rrrr	02rr	OR A,R	A ∨ R → A	Z
0 0010 01rr rrrr	02rr	OR R,A	A ∨ R → R	Z
0 0010 10rr rrrr	02rr	AND A,R	A & R → A	Z
0 0010 11rr rrrr	02rr	AND R,A	A & R → R	Z
0 0011 00rr rrrr	03rr	XOR A,R	A ⊕ R → A	Z
0 0011 01rr rrrr	03rr	XOR R,A	A ⊕ R → R	Z
0 0011 10rr rrrr	03rr	ADD A,R	A + R → A	Z, C, DC
0 0011 11rr rrrr	03rr	ADD R,A	A + R → R	Z, C, DC
0 0100 00rr rrrr	04rr	MOV A,R	R → A	Z
0 0100 01rr rrrr	04rr	MOV R,R	R → R	Z
0 0100 10rr rrrr	04rr	COMA R	/R → A	Z
0 0100 11rr rrrr	04rr	COM R	/R → R	Z
0 0101 00rr rrrr	05rr	INCA R	R+1 → A	Z
0 0101 01rr rrrr	05rr	INC R	R+1 → R	Z
0 0101 10rr rrrr	05rr	DJZA R	R-1 → A, skip if zero	None
0 0101 11rr rrrr	05rr	DJZ R	R-1 → R, skip if zero	None
0 0110 00rr rrrr	06rr	RRCA R	R(n) → A(n-1), R(0) → C, C→ A(7)	C
0 0110 01rr rrrr	06rr	RRC R	R(n) → R(n-1), R(0) → C, C → R(7)	C
0 0110 10rr rrrr	06rr	RLCA R	R(n) → A(n+1), R(7) → C, C → A(0)	C
0 0110 11rr rrrr	06rr	RLC R	R(n) → R(n+1), R(7) → C, C → R(0)	C
0 0111 00rr rrrr	07rr	SWAPA R	R(0-3) → A(4-7), R(4-7) → A(0-3)	None
0 0111 01rr rrrr	07rr	SWAP R	R(0-3) → R(4-7)	None

Binary Instruction				Hex	Mnemonic	Operation	Status Affected
0	0111	10rr	rrrr	07rr	JZA R	R+1 → A, skip if zero	None
0	0111	11rr	rrrr	07rr	JZ R	R+1 → R, skip if zero	None
0	100b	bbrr	rrrr	0xxx	BC R,b	0 → R(b)	None [2]
0	101b	bbrr	rrrr	0xxx	BS R,b	1 → R(b)	None [3]
0	110b	bbrr	rrrr	0xxx	JBC R,b	if R(b)=0, skip	None
0	111b	bbrr	rrrr	0xxx	JBS R,b	if R(b)=1, skip	None
1	00kk	kkkk	kkkk	1kkk	CALL k	PC+1 → [SP], (Page, k) → PC	None
1	01kk	kkkk	kkkk	1kkk	JMP k	(Page, k) → PC	None
1	1000	kkkk	kkkk	18kk	MOV A,k	k → A	None
1	1001	kkkk	kkkk	19kk	OR A,k	A ∨ k → A	Z
1	1010	kkkk	kkkk	1Akk	AND A,k	A & k → A	Z
1	1011	kkkk	kkkk	1Bkk	XOR A,k	A ⊕ k → A	Z
1	1100	kkkk	kkkk	1Ckk	RETL k	k → A, [Top of Stack] → PC	None
1	1101	kkkk	kkkk	1Dkk	SUB A,k	k-A → A	Z, C,DC
1	1110	0000	0001	1E01	INT	PC+1 → [SP], 001H → PC	None
1	1111	kkkk	kkkk	1Fkk	ADD A,k	k+A → A	Z, C, DC

Note: 1.This instruction is applicable to IOC5~IOC6, IOCB ~ IOCF only.
2.This instruction is not recommended for RF operation.
3.THis instruction cannot operate under RF.

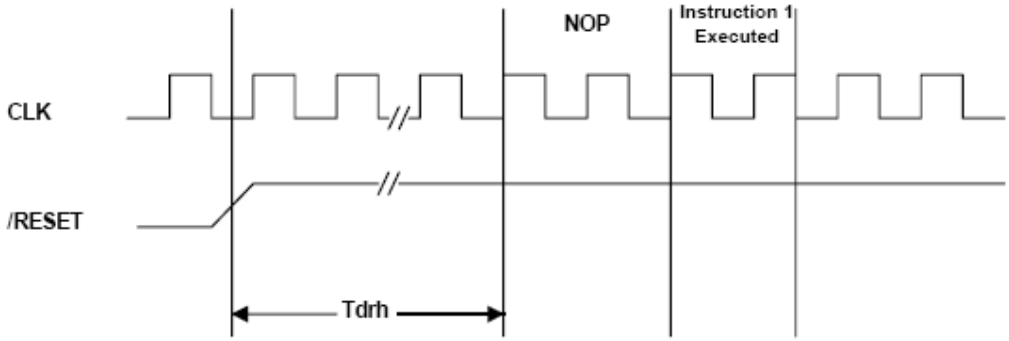
5.14 Timing Diagrams

AC Test Input/Output Waveform



AC Testing : Input is driven at 2.4V for logic "1",and 0.4V for logic "0".Timing measurements are made at 2.0V for logic "1",and 0.8V for logic "0".

RESET Timing (CLK="0")



TCC Input Timing (CLKS="0")

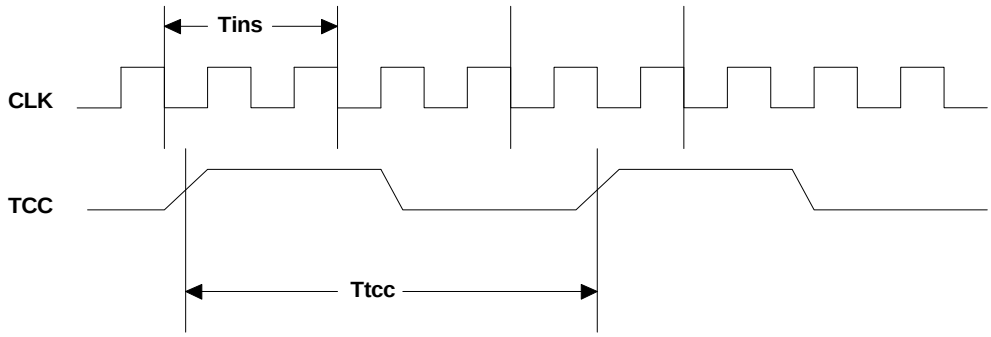


Figure 5-17 BJ8P153C Timing Diagrams

6 Absolute Maximum Ratings

■ **BJ8P153C**

Temperature under bias	0°C to 70°C
Storage temperature	-65°C to 150°C
Input voltage	-0.3V to +6.0V
Output voltage	-0.3V to +6.0V

Note: *These parameters are theoretical values and have not been tested.

7 Electrical Characteristics

7.1 DC Characteristic

Ta=25 °C, VDD=5V±5%, VSS=0V

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
FXT	Crystal: VDD to 2.3V	Two cycle with two clocks	DC		4.0	MHz
	Crystal: VDD to 3V	Two cycle with two clocks	DC		8.0	MHz
	Crystal: VDD to 5V	Two cycle with two clocks	DC		20.0	MHz
ERC	ERC: VDD to 5V	R: 5K&, C: 39 pF	F±30%	1500	F±30%	kHz
IIL	Input Leakage Current for input pins	VIN = VDD, VSS			±1	∝A
VIH1	Input High Voltage (VDD=5V)	Ports 5, 6	2.0			V
VIL1	Input Low Voltage (VDD=5V)	Ports 5, 6			0.8	V
VIHT1	Input High Threshold Voltage (VDD=5V)	/RESET, TCC (Schmitt trigger)	2.0			V
VILT1	Input Low Threshold Voltage (VDD=5V)	/RESET, TCC (Schmitt trigger)			0.8	V
VIHX1	Clock Input High Voltage (VDD=5V)	OSCI	2.5		Vdd+0.3	V
VILX1	Clock Input Low Voltage (VDD=5V)	OSCI			1.0	V
VIH2	Input High Voltage (VDD=3V)	Ports 5, 6	1.5			V
VIL2	Input Low Voltage (VDD=3V)	Ports 5, 6			0. 4	V
VIHT2	Input High Threshold Voltage (VDD=3V)	/RESET, TCC (Schmitt trigger)	1.5			V
VILT2	Input Low Threshold Voltage (VDD=3V)	/RESET, TCC (Schmitt trigger)			0.4	V
VIHX2	Clock Input High Voltage (VDD=3V)	OSCI	1.5			V
VILX2	Clock Input Low Voltage (VDD=3V)	OSCI			0.6	V
VOH1	Output High Voltage (Ports 6) (P60~P63, P66~P67 are Schmitt trigger)	IOH = -12 mA	2.4			V
VOL1	Output Low Voltage (P50~P53, P60~P63 P66~P67 are Schmitt trigger)	IOL = 12 mA			0.4	V
VOL2	Output Low Voltage (P64, P65)	IOL = 16.0 mA			0.4	V
IPH	Pull-high current	Pull-high active, input pin at VSS	–50	–100	–240	μA
IPD	Pull-down current	Pull-down active, input pin at VDD	20	50	120	μA

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
ISB1	Power down current	All input and I/O pins at VDD, Output pin floating, WDT disabled	-	-	1	μA
ISB2	Power down current	All input and I/O pins at VDD, Output pin floating, WDT enabled	-	-	10	μA
ICC1	Operating supply current at two clocks (VDD=3V)	/RESET= 'High', Fosc=32kHz (Crystal type, CLKS="0"), Output pin floating, WDT disabled	15	15	30	μA
ICC2	Operating supply current at two clocks (VDD=3V)	/RESET= 'High', Fosc=32KHz (Crystal type, CLKS="0"), Output pin floating, WDT enabled	-	19	35	μA
ICC3	Operating supply current at two clocks (VDD=5.0V)	/RESET= 'High', Fosc=4MHz (Crystal type, CLKS="0"), Output pin floating	-	-	2.0	mA
ICC4	Operating supply current at two clocks (VDD=5.0V)	/RESET= 'High', Fosc=10MHz (Crystal type, CLKS="0"), Output pin floating	-	-	4.0	mA

Note: *These parameters are theoretical values and have not been tested.

7.2 AC Characteristic

Ta=25°C, VDD=5V ± 5%, VSS=0V

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Dclk	Input CLK duty cycle	-	45	50	55	%
Tins	Instruction cycle time (CLKS="0")	Crystal type	100	-	DC	ns
		RC type	500	-	DC	ns
Ttcc	TCC input period	-	(Tins+20)/N*	-	-	ns
Tdrh	Device reset hold time	Ta = 25°C, TXAL, SUT1, SUT0=1, 1	17.6-30%	17.6	17.6+30%	ms
Trst	/RESET pulse width	Ta = 25°C	2000	-	-	ns
*Twdt1	Watchdog timer period	Ta = 25°C SUT1, SUT0=1,1	17.6~30%	17.6	17.6+30%	ms
*Twdt2	Watchdog timer period	Ta = 25°C SUT1, SUT0=1,0	4.5+30%	4.5	4.5+30%	ms
*Twdt3	Watchdog timer period	Ta = 25°C SUT1, SUT0=0,1	288~30%	288	288+30%	ms
*Twdt4	Watchdog timer period	Ta = 25°C SUT1, SUT0=0,0	72~30%	72	72+30%	ms
Tset	Input pin setup time	-	-	0	-	ns
Thold	Input pin hold time	-	-	20	-	ns
Tdelay	Output pin delay time	Cload=20pF	-	50	-	ns

Note: These parameters are theoretical values and have not been tested.

The Watchdog Timer duration is determined by Option Code (Bit 6, Bit 5)

*N = selected prescaler ratio

*Twdt1: The Option word (SUT1, SUT0) is used to define the oscillator set-up time. In Crystal mode the WDT time-out length is the same as set-up time (18ms).

*Twdt2: The Option word (SUT1, SUT0) is used to define the oscillator set-up time. In Crystal mode the WDT time-out length is the same as set-up time (4.5ms).

*Twdt3: The Option word (SUT1, SUT0) is used to define the oscillator set-up time. In Crystal mode the WDT time-out length is the same as set-up time (288ms).

*Twdt4: The Option word (SUT1, SUT0) is used to define the oscillator set-up time. In Crystal mode the WDT time-out length is the same as set-up time (72ms).

APPENDIX

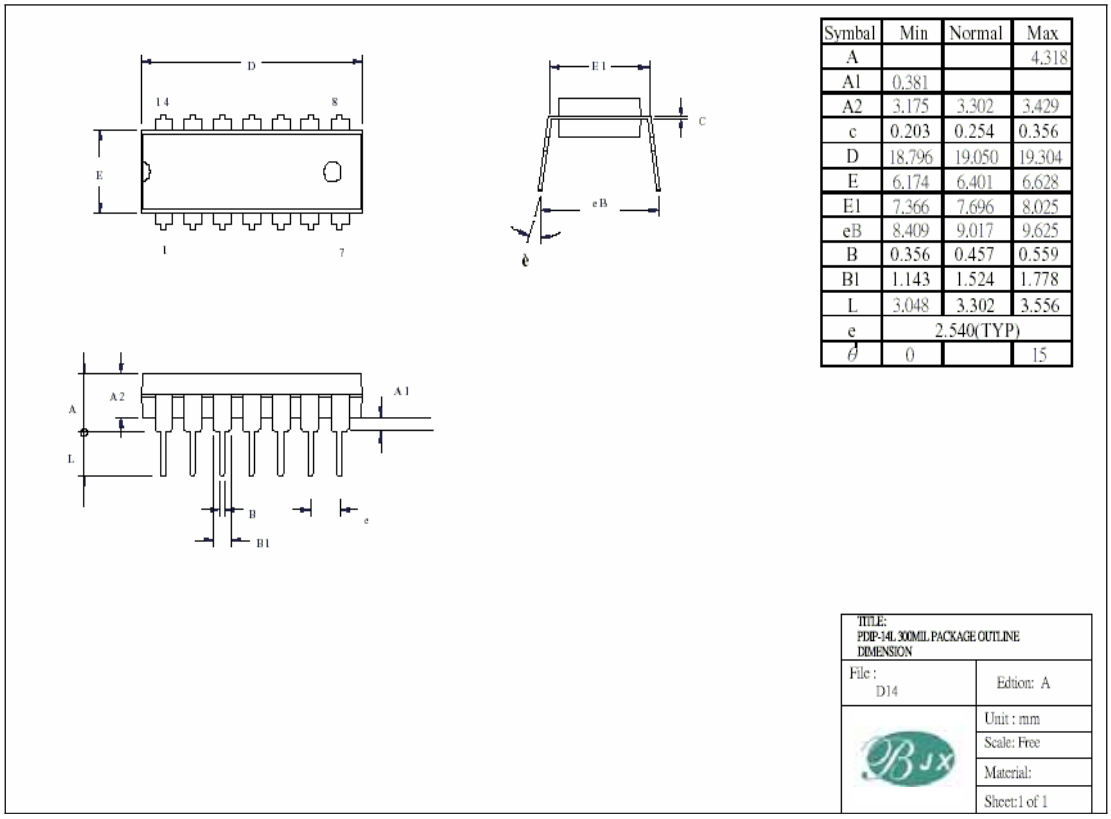
A Package Type

OTP MCU	Package Type	Pin Count	Package Size
BJ8P153C	DIP	14	300 mil

Part no.	BJ8P153C
Electroplate type	Pure Tin
Ingredient (%)	Sn: 100%
Melting point (°C)	232°C
Electrical resistivity (∝&-cm)	11.4
Hardness (hv)	8~10
Elongation (%)	>50%

B Package Information

■ **14-Lead Plastic Dual in line (DIP) – 300 mil**

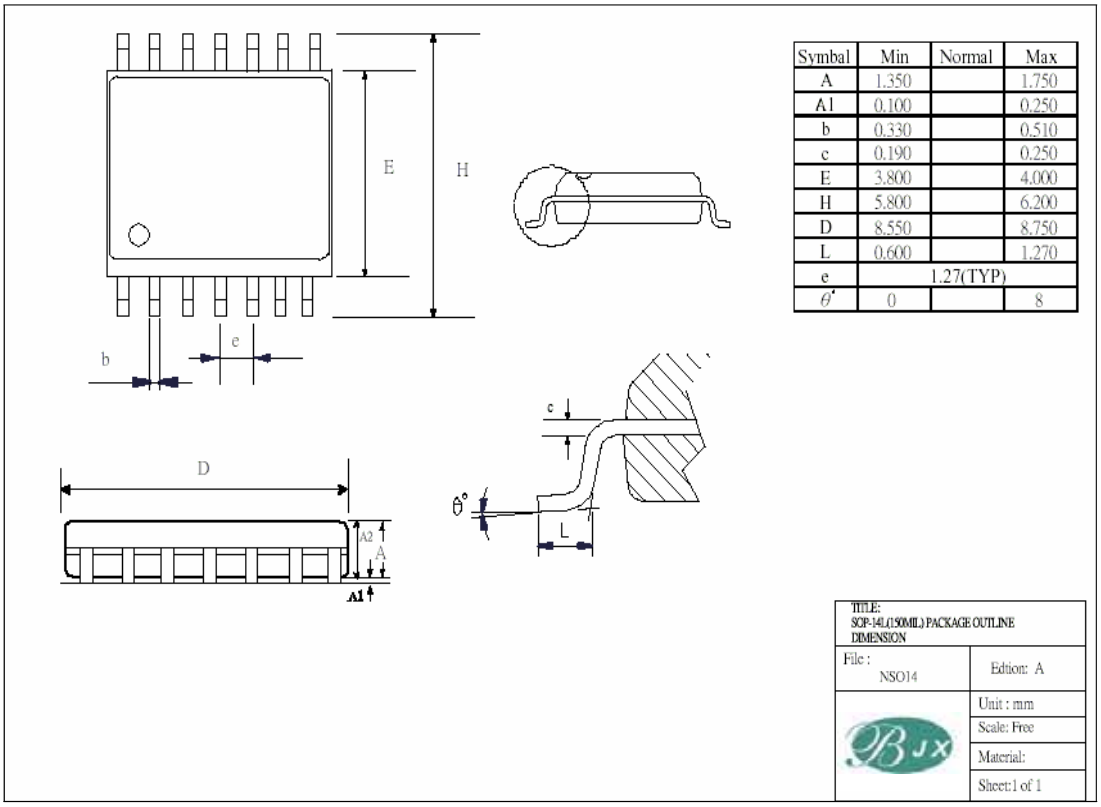


Symbal	Min	Normal	Max
A			4.318
A1	0.381		
A2	3.175	3.302	3.429
c	0.203	0.254	0.356
D	18.796	19.050	19.304
E	6.174	6.401	6.628
E1	7.366	7.696	8.025
eB	8.409	9.017	9.625
B	0.356	0.457	0.559
B1	1.143	1.524	1.778
L	3.048	3.302	3.556
e	2.540(TYP)		
θ	0		15

TITLE: PDIP-14L 300MIL PACKAGE OUTLINE DIMENSION	
File : D14	Edtion: A
	Unit : mm
	Scale: Free
	Material:
	Sheet:1 of 1

Figure B-1a BJ8P153C 14-Lead PDIP Package Type

- **14-Lead Plastic Dual in line (SOP) – 150 mil**



Symbal	Min	Normal	Max
A	1.350		1.750
A1	0.100		0.250
b	0.330		0.510
c	0.190		0.250
E	3.800		4.000
H	5.800		6.200
D	8.550		8.750
L	0.600		1.270
e	1.27(TYP)		
θ°	0		8

Figure B-1b BJ8P153C 14-Lead SOP Package Type

C Device Characteristics

The graphs provided in the following pages were derived based on a limited number of samples and are shown here for reference only. The device characteristic illustrated herein are not guaranteed for its accuracy. In some graphs, the data maybe out of the specified warranted operating range.

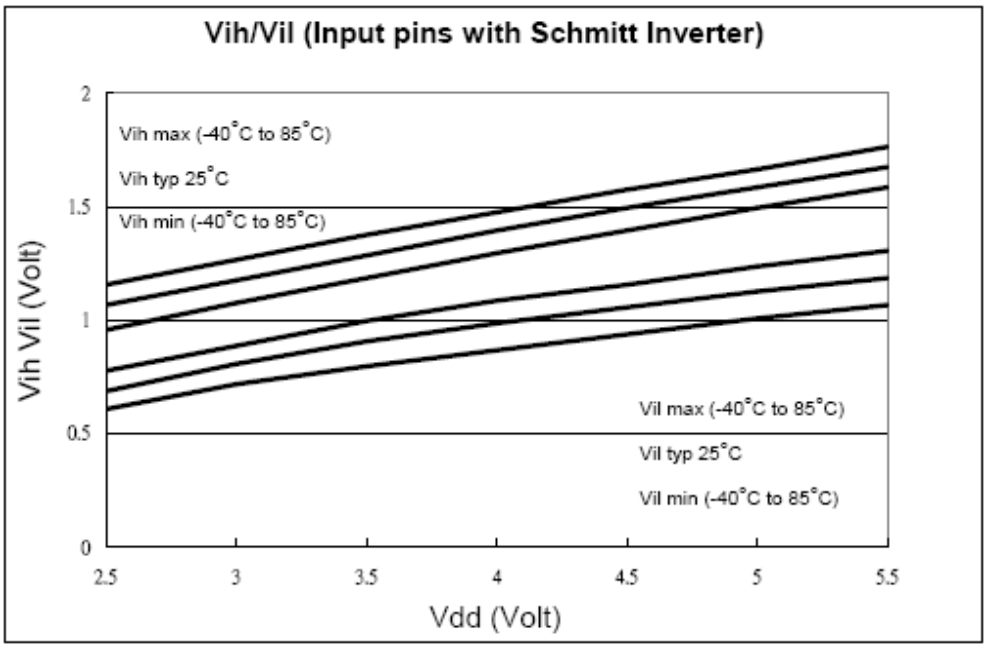


Fig. C-1 Vih, Vil of P60~P63, P66, P67 vs. VDD

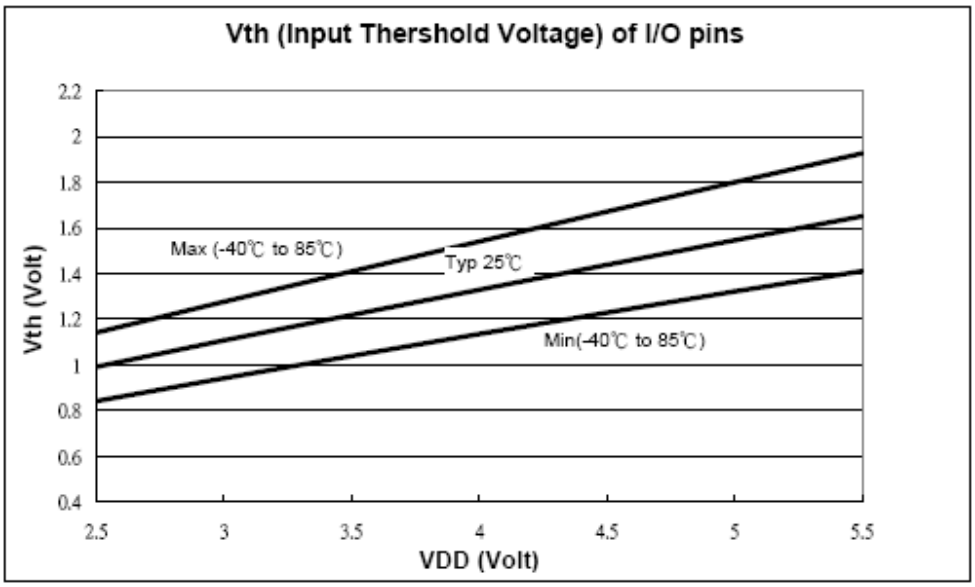


Fig. C-2 Vth (Threshold voltage) of P50~P53, P64~P65 vs. VDD

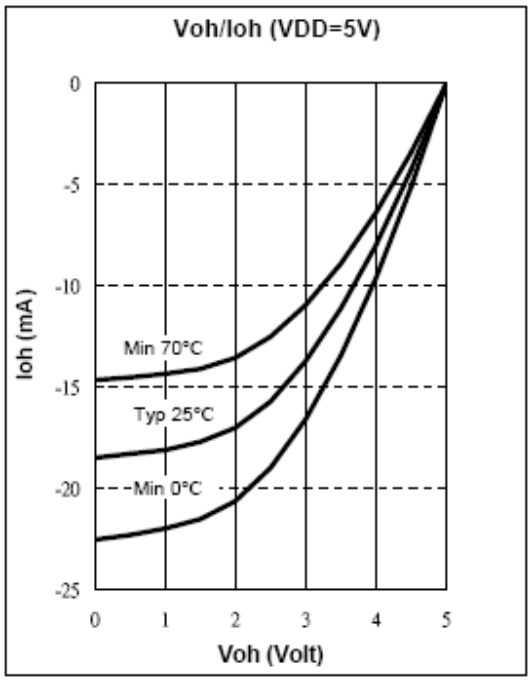


Fig. C-3 Port 5 and Port 6 Voh vs. Ioh, VDD=5V

Fig. C-4 Port 5 and Port 6 Voh vs. Ioh, VDD=3V

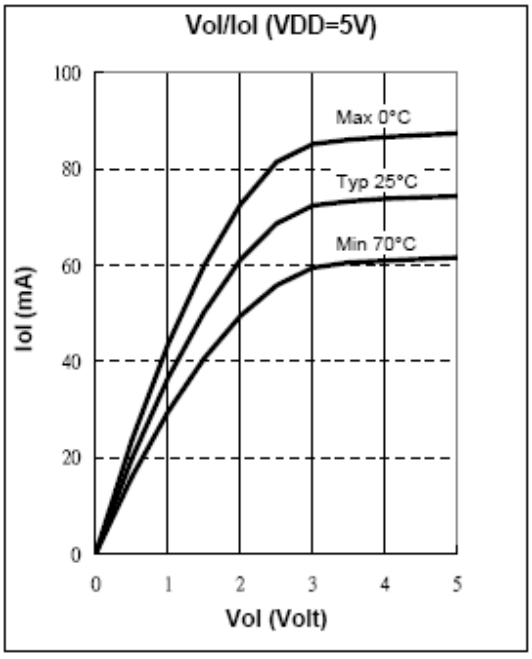


Fig. C-5 Port 5, Port 6.0~Port 6.3 and Port 6.6~Port 6.7 Vol vs. Iol, VDD=5V

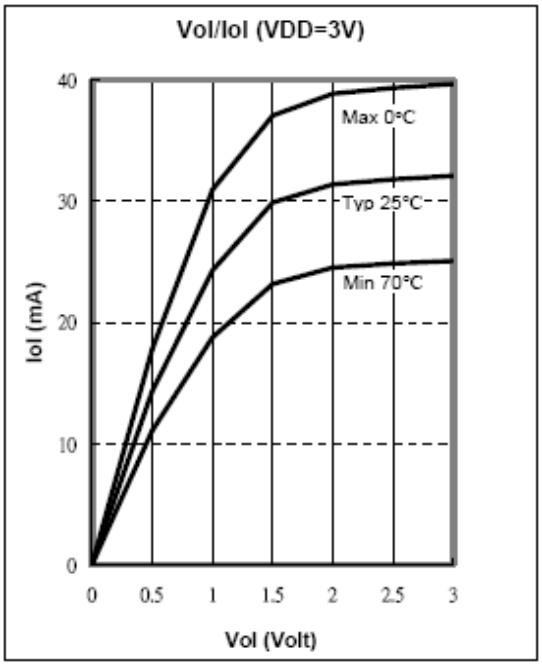


Fig. C-6 Port 5, Port 6.0~Port 6.3 and Port 6.6~Port 6.7 Vol vs. Iol, VDD=3V

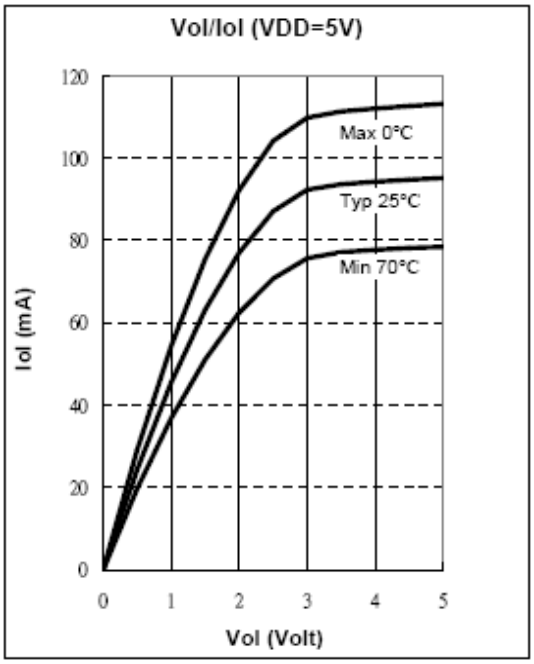


Fig. C-7 Port 6.4 and Port6.5 Vol vs. Iol, VDD=5V

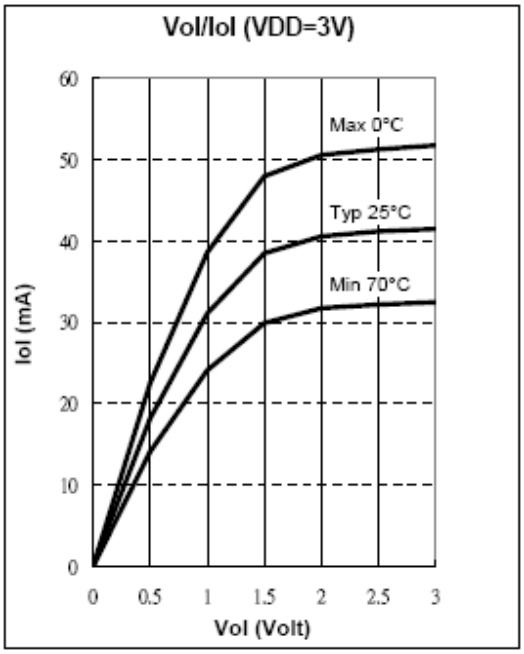


Fig. C-8 Port 6.4 and Port 6.5 Vol vs. Iol, VDD=3V

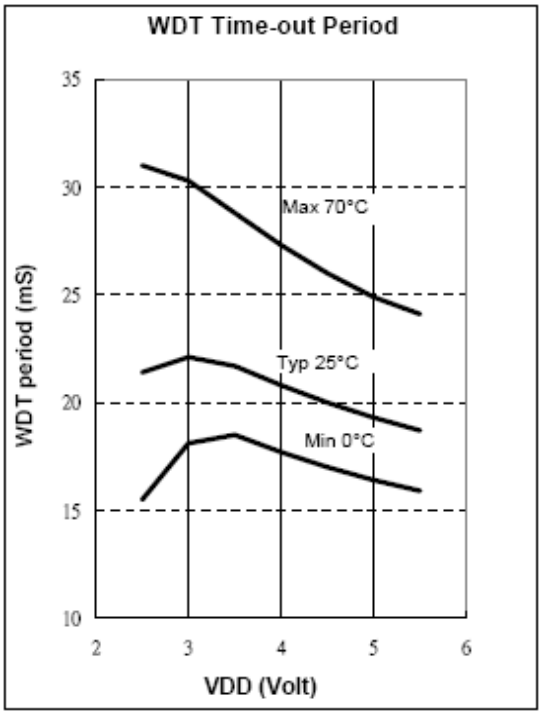


Fig. C-9 WDT time-out period vs. VDD, Prescaler set to 1:1

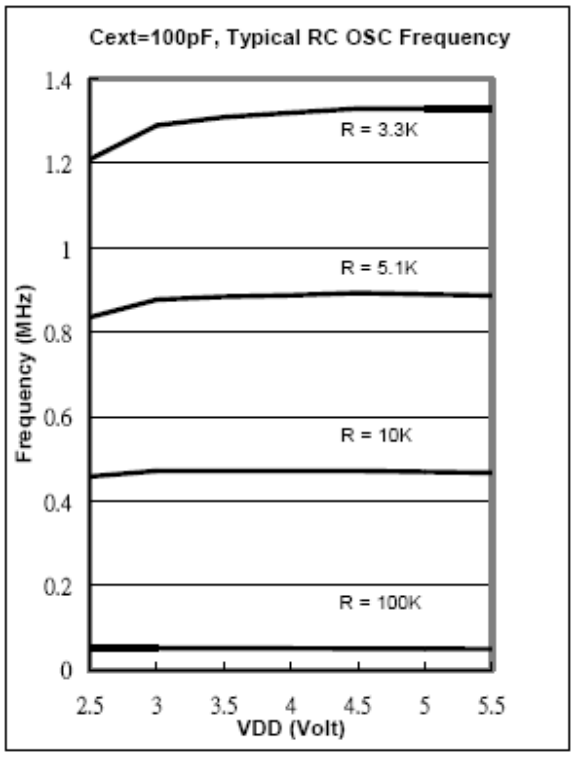


Fig. C-10 Typical RC OSC Frequency vs. VDD (Cext=100pF, Temperature at 25°C)

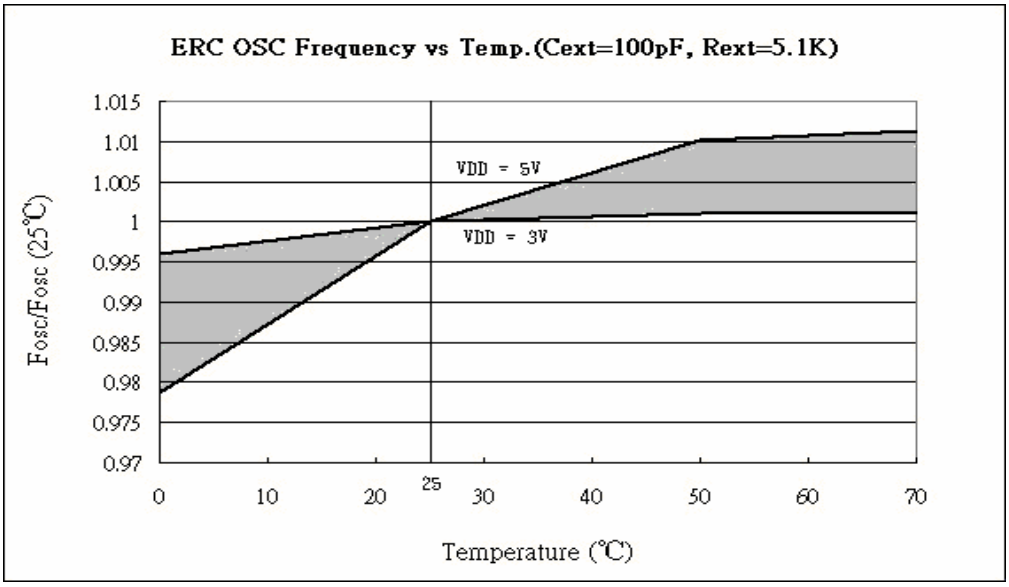


Fig. C-11 Typical RC OSC Frequency vs. Temperature (R and C are ideal components)

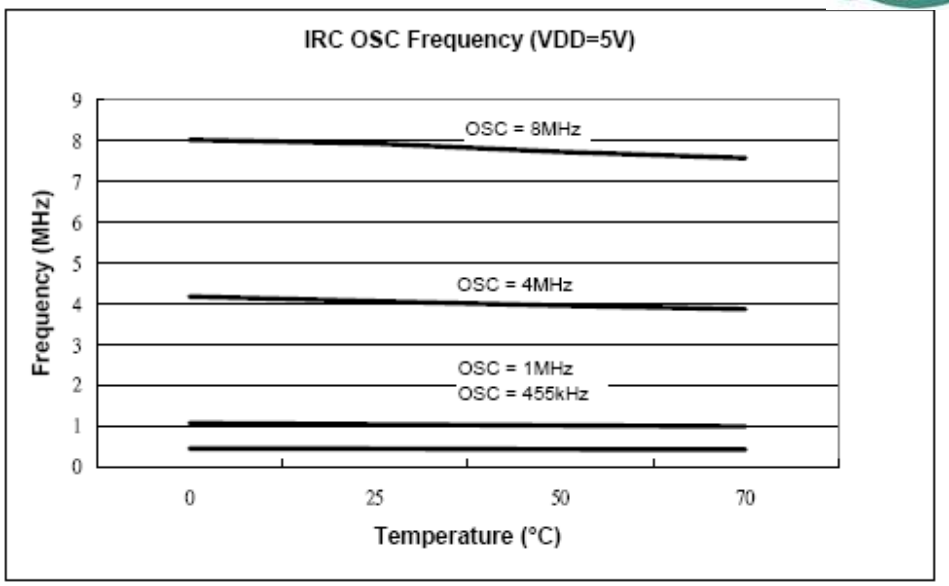


Fig. C-12 Internal RC OSC Frequency vs. Temperature, VDD=5V

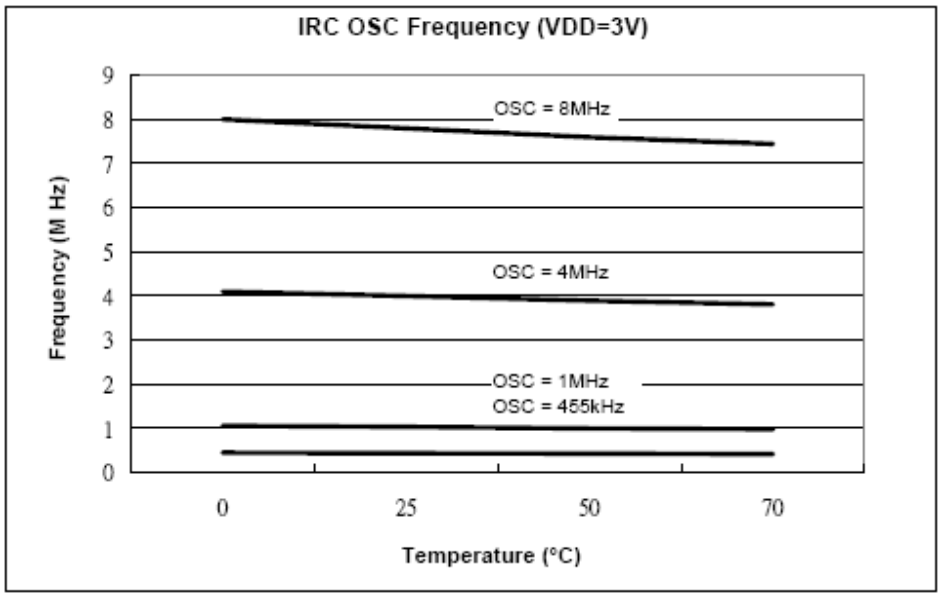


Fig. C-13 Internal RC OSC Frequency vs. Temperature, VDD=3V

Four conditions exist with the Operating Current ICC1 toICC4. These conditions are as follows:

ICC1: VDD=3V, Fosc=32kHz, 2 clocks, WDT disabled

ICC2: VDD=3V, Fosc=32kHz, 2 clocks, WDT enabled

ICC3: VDD=5V, Fosc=4MHz, 2 clocks, WDT enabled

ICC4: VDD=5V, Fosc=10M Hz, 2 clocks, WDT enabled

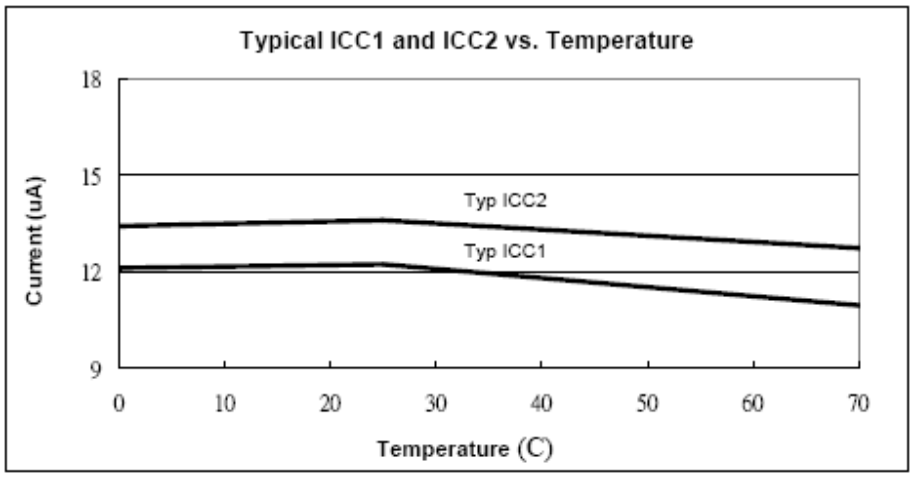


Fig. C-14 Typical operating current (ICC1 and ICC2) vs. Temperature

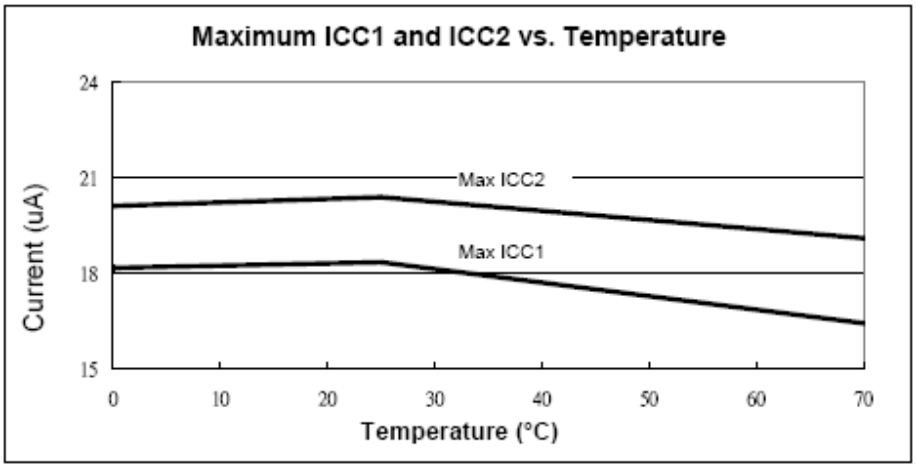


Fig. C-15 Maximum operating current (ICC1 and ICC2) vs. Temperature

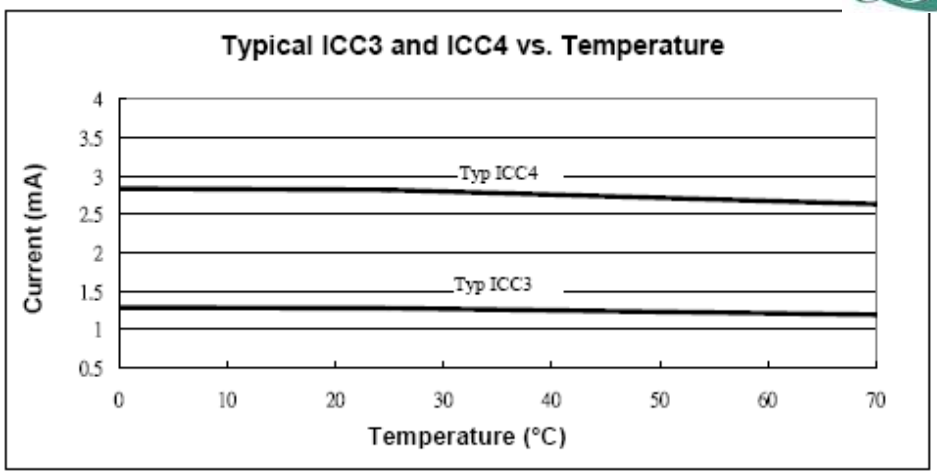


Fig. C-16 Typical operating current (ICC3 and ICC4) vs. Temperature

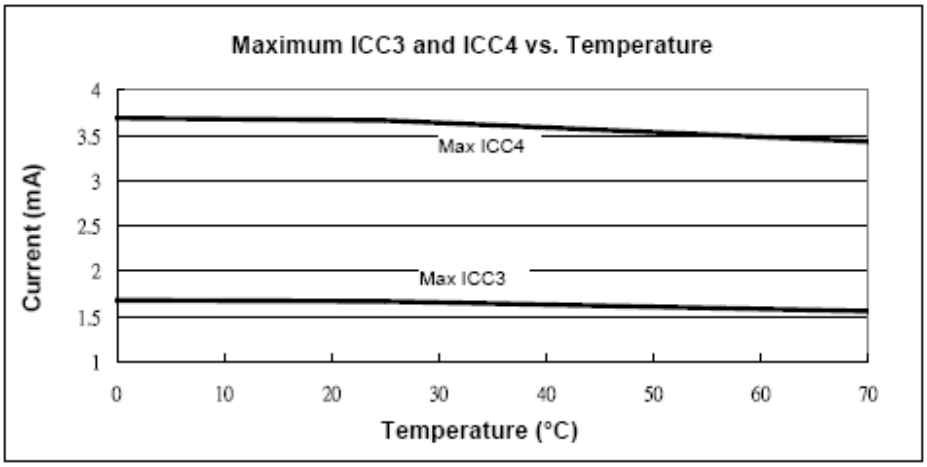


Fig. C-17 Maximum Operating Current (ICC3 and ICC4) vs. Temperature

The following two conditions exist with the Standby Current ISB1 and ISB2:

ISB1: VDD=5V, WDT disable

ISB2: VDD=5V, WDT enable

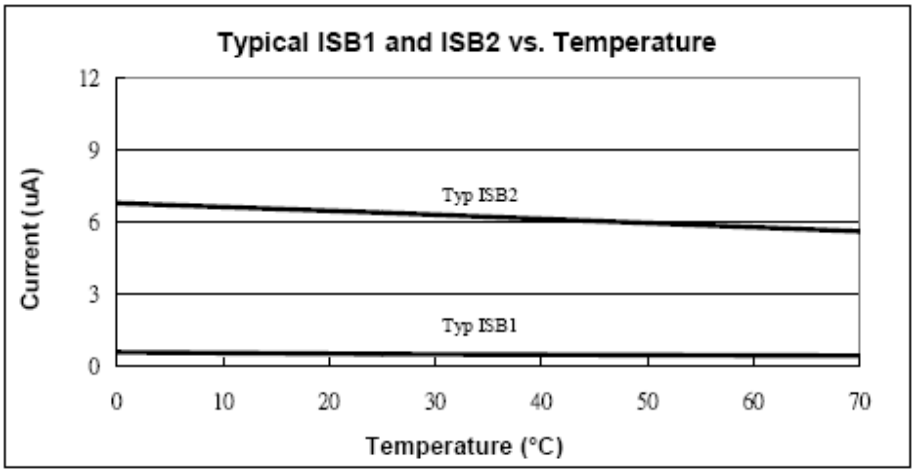


Fig. C-18 Typical Standby Current (ISB1 and ISB2) vs. Temperature