



Typical Application Circuit

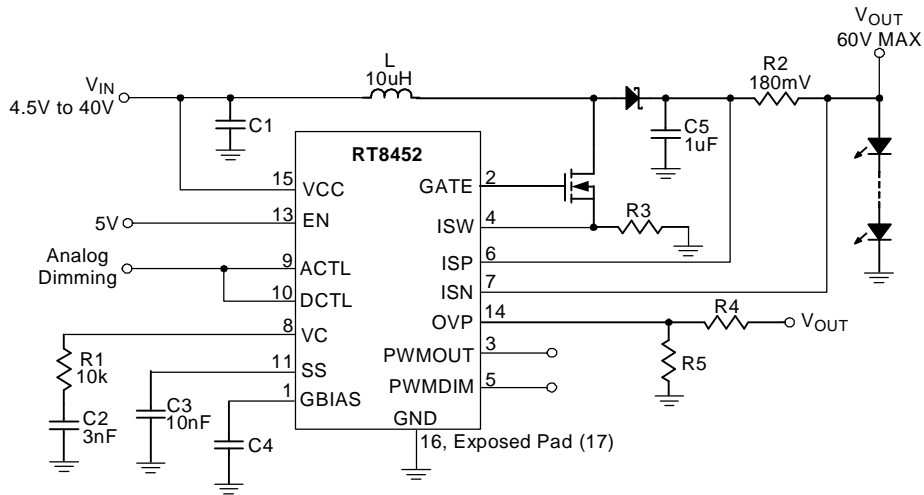


Figure 1. Analog Dimming in Boost Configuration

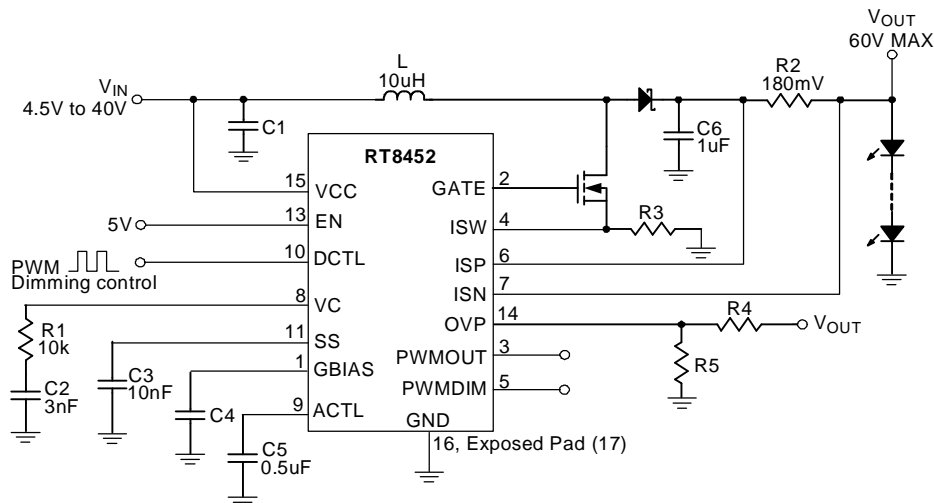


Figure 2. PWM to Analog Dimming in Boost Configuration

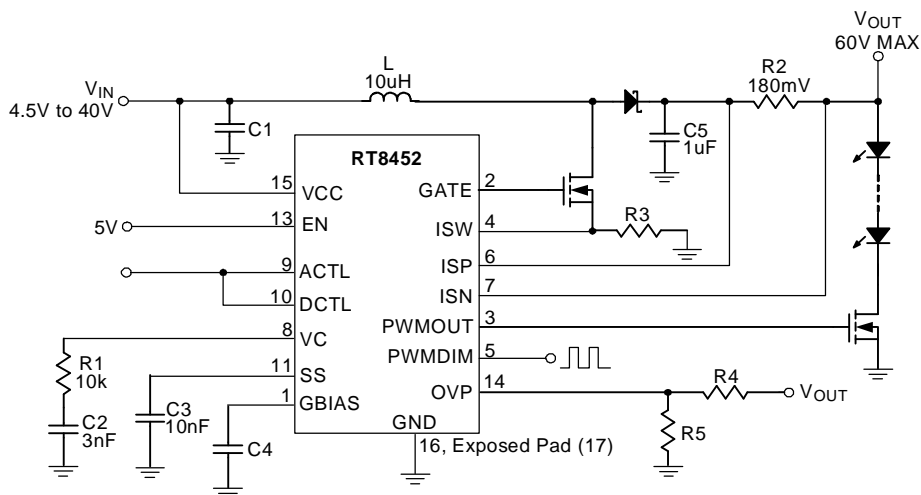


Figure 3. True PWM Dimming in Boost Configuration

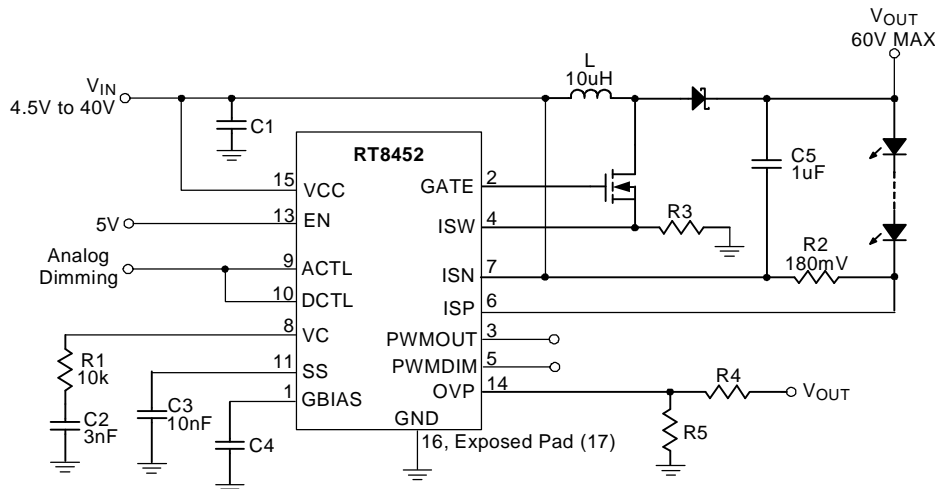


Figure 4. Analog Dimming in Buck-Boost Configuration

### Functional Pin Description

SOP-16	QFN3X3-16	Pin Name	Pin Function
1	1	GBIAS	The Internal Gate Driver Bias Pin. A good bypass capacitor is required.
2	2	GATE	The External MOSFET Switch Gate Driver Output Pin.
3	3	PWMOUT	The Output Pin for the PWM Dimming FET Driver.
4	4	ISW	The External MOSFET Switch Current Sense Pin. Connect the current sense resistor between external N-MOSFET switch and the ground.
5	5	PWMDIM	The Control Input Pin for the PWM Dimming FET Driver.
6	6	ISP	The LED Current Sense Amplifier Positive Input.
7	7	ISN	The LED Current Sense Amplifier Negative Input. Voltage threshold between ISP and ISN is 180mV.
8	8	VC	The PWM Control Loop Compensation Pin.
9	9	ACTL	The Analog Dimming Control Pin. The effective programming voltage range of the pin is between 0.3V and 1.2V.
10	10	DCTL	By adding a 0.1uF filtering capacitor on ACTL pin, the PWM dimming signal on DCTL pin can be averaged and converted into analog dimming signal on the ACTL pin following the formula below. $V_{ACTL} = 1.2V \times \text{PWM Dimming Duty Cycle}$ .
11	11	SS	The Soft-Start Pin. A capacitor of at least 10nF is required for proper soft start.
12	12	NC	No Internal Connection.
13	13	EN	The Chip Enable (Active High) Pin. When this pin voltage is low, the chip is in shutdown mode.
14	14	OVP	The Over Voltage Protection Pin. The PWM converter turns off when The voltage of the pin goes higher than 1.2V.
15	15	VCC	The Power Supply Pin of the Chip. For good bypass, a low ESR Capacitor is required.
16	16 Exposed Pad (17)	GND	The Ground Pin. The exposed pad must be soldered to a large PCB And connected to GND for maximum power dissipation.

Function Block Diagram

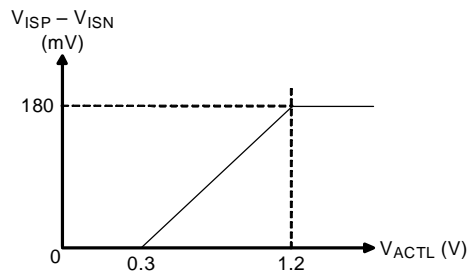
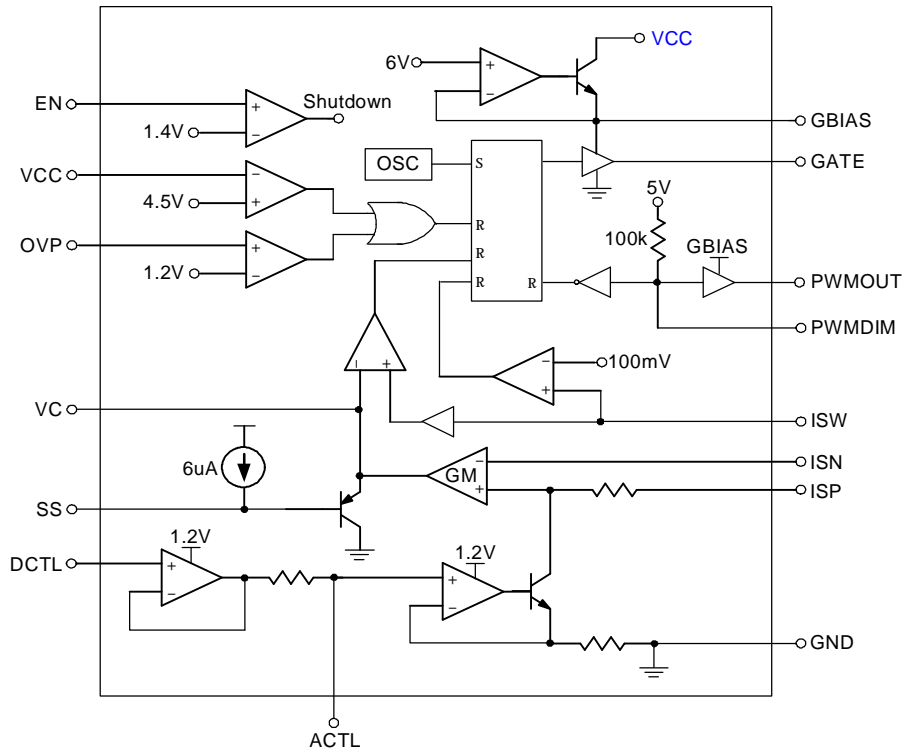


Figure 5

**Absolute Maximum Ratings** (Note 1)

Supply Input Voltage, $V_{CC}$ -----	45V
GBIAS, GATE, PWMDIM, PWMOUT, ISW -----	10V
ISP, ISN -----	65V
DCTL, ACTL, OVP, EN -----	20V
Power Dissipation, $P_D$ @ $T_A = 25^\circ\text{C}$	
SOP-16 -----	1.053W
WQFN-16L 3x3 -----	1.471W
Package Thermal Resistance (Note 4)	
SOP-16, $\theta_{JC}$ -----	95°C/W
SOP-16, $\theta_{JC}$ -----	45°C/W
WQFN-16L 3x3, $\theta_{JA}$ -----	68°C/W
WQFN-16L 3x3, $\theta_{JC}$ -----	7.5°C/W
Junction Temperature -----	150°C
Lead Temperature (Soldering, 10 sec.) -----	260°C
Storage Temperature Range -----	-65°C to 150°C
ESD Susceptibility (Note 2)	
HBM (Human Body Mode) -----	2kV
MM (Machine Mode) -----	200V

**Recommended Operating Conditions** (Note 3)

Junction Temperature Range -----	-40°C to 125°C
Ambient Temperature Range -----	-40°C to 85°C

**Electrical Characteristics**

( $V_{CC} = 24V$ , No Load on any Output,  $T_A = 25^\circ\text{C}$ , unless otherwise specified)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
<b>Overall</b>						
Supply Voltage	$V_{CC}$		4.5	--	40	V
Supply Current	$I_{VCC}$	$V_C \leq 0.4V$ (Switching off)	--	4	6	mA
Shutdown Current	$I_{SHDN}$	$V_{EN} \leq 0.7V$	--	12	--	uA
Shutdown Threshold	$V_{EN}$		--	1.4	--	V
EN Input Current		$V_{EN} \leq 5V$	--	--	0.5	uA
<b>Current Sense Amplifier</b>						
Input Threshold ( $V_{ISP} - V_{ISN}$ )		$4.5V \leq \text{common mode} \leq 40V$	170	180	190	mV
ISP / ISN Input Current	$I_{ISP} / I_{ISN}$	$4.5V \leq V_{ISP} = V_{ISN} \leq 60V$	--	140	--	uA
VC Output Current	$I_{VC}$	$V_{ISP} - V_{ISN} = 120mV$ , $0.5V \leq V_C \leq 2.4V$	--	$\pm 20$	--	uA
VC Threshold for PWM Switch Off			--	0.7	--	V
<b>LED Dimming</b>						
Analog Dimming ACTL Pin Input Current	$I_{ACTL}$	$0.3V \leq V_{ACTL} \leq 1.3V$	--	--	1	uA

*To be continued*

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
LED Current Off Threshold at ACTL	V <sub>ACTL_Off</sub>		--	0.2	--	V
DCTL Input Current	I <sub>DCTL</sub>	0.3V ≤ V <sub>DCTL</sub> ≤ 6V	--	--	0.5	uA
<b>PWM Control</b>						
Switching Frequency	f <sub>SW</sub>		800k	1M	1.2M	Hz
Maximum Duty Cycle (Note 5)			--	86	--	%
Minimum on Time			--	200	--	ns
<b>Switch Gate Driver</b>						
GBIAS Voltage	V <sub>GBIAS</sub>	I <sub>GBIAS</sub> = 20mA	--	5.7	--	V
Gate Voltage High	V <sub>Gate_H</sub>	I <sub>Gate</sub> = -50mA	--	4.2	--	V
		I <sub>Gate</sub> = -100uA	--	5	--	
Gate Voltage Low	V <sub>Gate_L</sub>	I <sub>Gate</sub> = 50mA	--	0.25	--	V
		I <sub>Gate</sub> = 100uA	--	0.1	--	
GATE Drive Rise and Fall Time		1nF Load	--	15	--	ns
PWM Switch Current Limit Threshold	I <sub>SW_LIM</sub>		--	100	--	mV
<b>PWM Dimming Gate Driver</b>						
PWMDIM Threshold (Low to High)			--	1.5	--	V
PWMDIM Threshold Hysteresis			--	0.5	--	V
PWMOUT Drive Rise and Fall Time		1nF Load	--	40	--	ns
<b>OVP and Soft Start</b>						
OVP Threshold	V <sub>OVP_th</sub>		--	1.2	--	V
OVP Input Current	I <sub>OVP</sub>	0.7V ≤ V <sub>OVP</sub> ≤ 1.5V	--	--	0.1	uA
Soft Start Pin Current	I <sub>SS</sub>	V <sub>SS</sub> ≤ 2V	--	6	--	uA

**Note 1.** Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device.

These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

**Note 2.** Devices are ESD sensitive. Handling precaution recommended. The human body model is a 100pF capacitor discharged through a 1.5kΩ resistor into each pin.

**Note 3.** The device is not guaranteed to function outside its operating conditions.

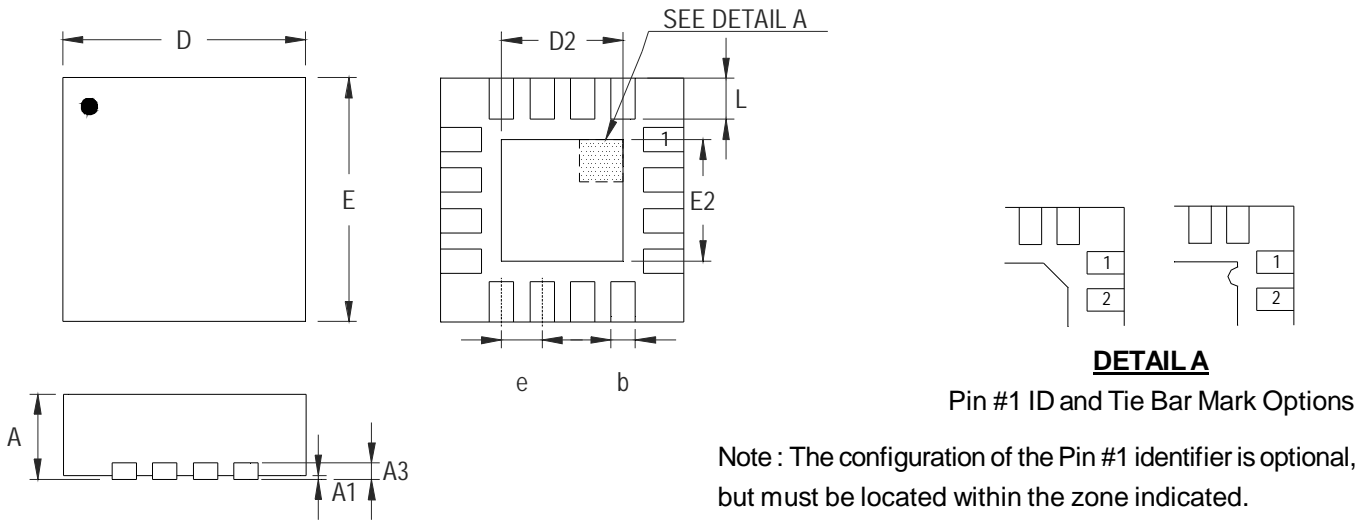
**Note 4.** θ<sub>JA</sub> is measured in the natural convection at T<sub>A</sub> = 25°C on a high effective four layers thermal conductivity test board of JEDEC 51-7 thermal measurement standard.

**Note 5.** When the natural maximum duty cycle of 1MHz switching frequency is reached, the switching cycle will be skipped (not reset) as the operating condition requires to effectively stretch and achieve higher on cycle than the natural maximum duty cycle set by the 1MHz switching frequency.

**Datasheet Revision History**

Version	Date	Page No.	Item	Description
00C	2008/2/22			first edition
01C	2008/2/27		Features Typical Application Circuit Functional Pin Description Function Block Diagram Electrical Characteristics	Modify
02C	2008/3/18		Ordering Information	Modify

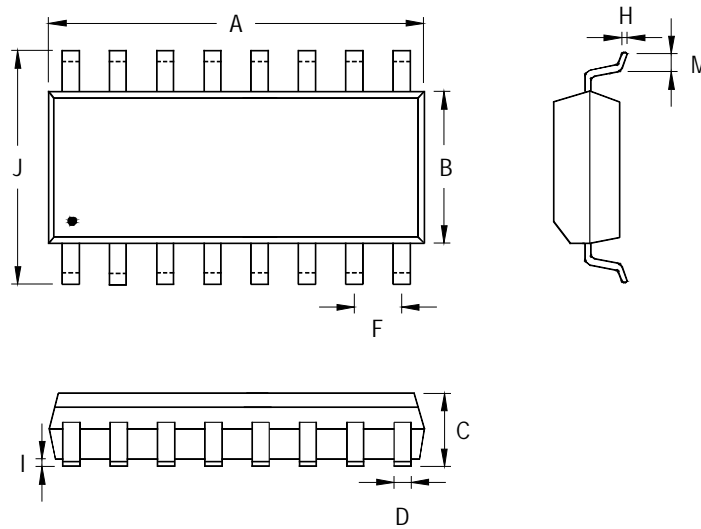
Outline Dimension



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
A3	0.175	0.250	0.007	0.010
b	0.180	0.300	0.007	0.012
D	2.950	3.050	0.116	0.120
D2	1.300	1.750	0.051	0.069
E	2.950	3.050	0.116	0.120
E2	1.300	1.750	0.051	0.069
e	0.500		0.020	
L	0.350	0.450	0.014	0.018

W-Type 16L QFN 3x3 Package





Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	9.804	10.008	0.386	0.394
B	3.810	3.988	0.150	0.157
C	1.346	1.753	0.053	0.069
D	0.330	0.508	0.013	0.020
F	1.194	1.346	0.047	0.053
H	0.178	0.254	0.007	0.010
I	0.102	0.254	0.004	0.010
J	5.791	6.198	0.228	0.244
M	0.406	1.270	0.016	0.050

**16-Lead SOP Plastic Package**

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