Modeling Average Current Mode Control

Philip Cooke

cooke@unitrode.com
Unitrode Integrated Circuits Corporation
7 Continental Boulevard, Merrimack, NH 03054-4334
Phone: (603) 429-8751, FAX: (603) 429-8564

Abstract - An averaged small signal model is presented which predicts some of the previously reported phenomena and offers new insights with analytical expressions useful for design. Detailed analysis is given for the buck converter topology with the boost and buck-boost results also provided. The modulator gain, for a first order approximation, is shown to be constant as in voltage mode control. Guidelines are presented to optimize the design of the current loop and control-to-output transfer functions are given which are necessary to compensate the voltage loop. Experimental data is provided, in the case of the buck converter, to develop and verify the model.

I. INTRODUCTION

There is a tradeoff between complexity and ease of use for models employed in the design of average current mode control circuits. It is desirable to have expressions that lend insight into dominant system behavior and are practical and simple enough to design with. This paper will present an average current mode control model for the buck converter topology in continuous conduction mode. Details for the boost and buck-boost topologies are also included in the tables. Experimental results from the buck converter are used to develop the model and verify the accuracy of the derived analytical expressions.

One average current mode control model detailed in [1, 2] is an extension of peak current mode control and includes the sampling effect [3, 4]. There are feedforward terms from the input and output voltages but it contains a non-linear equation for the modulator gain. It was shown in [5] that for peak current mode control these feedforward terms are required to properly model time varying effects. Furthermore, in [6], a model was proposed questioning the inclusion of the sampling term for average current mode control. However, the model described in [6] doesn't include the feedforward terms one might expect in average current mode control since it is similar to peak current mode control. The aim of this work is to extend [6] to include these feedforward terms thus satisfying the time varying effects for average current mode control as was done for peak current mode control and to use the first order approximation that the modulator gain is constant. In addition, approximate expressions for the poles and zeroes are provided for design purposes.

II. MODEL DEVELOPMENT

It has been reported [5] that the following equation for the duty ratio of peak current mode control takes into account time varying effects but ignores the sampling effect

$$\hat{d}(t)=\frac{1}{M_E T_S}\left[\hat{v}_C(t)-R_I\hat{i}_L(t)-\frac{D^2T_S}{2}\hat{m}_1(t)-\frac{D'^2T_S}{2}\hat{m}_2(t)\right] \quad (1)$$

where M_E is the external slope compensation in volts per second, T_S is the switching period, v_C is the output of the voltage loop error amplifier, R_I is the total current sense gain, i_L is the inductor current, D and D′ are the duty and complementary duty ratios respectively (D′ = 1-D), and m_1 and m_2 are the rising and falling slopes (with units of volts per second) of the sensed current waveform scaled by R_I. Table I lists values for m_1 and m_2 for the three basic converter topologies in continuous conduction mode (CCM). In this table V_G is the input voltage, V_O is the output voltage and L is the power stage inductance. For the buck-boost converter $V_O < 0$. The modulator gain is extracted (see [7]) from (1) as

$$F_M=\frac{1}{M_E T_S}. \quad (2)$$

After using the expressions in Table I and (2), conversion of (1) into the frequency domain yields

$$\hat{D}(s)=F_M\cdot\left(\hat{V}_C(s)-R_I\hat{I}_L(s)-G_G\hat{V}_G(s)-G_O\hat{V}_O(s)\right) \quad (3)$$

TABLE I

SENSED INDUCTOR VOLTAGE SLOPES FOR CURRENT MODE CONTROL IN CCM

Topology	m_1	m_2
Buck	$\frac{V_G-V_O}{L}R_I$	$\frac{V_O}{L}R_I$
Boost	$\frac{V_G}{L}R_I$	$\frac{V_O-V_G}{L}R_I$
Buck-Boost	$\frac{V_G}{L}R_I$	$-\frac{V_O}{L}R_I$

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where G_G is the line voltage feedforward term, G_O is the output voltage feedforward term (these are listed in Table II for CCM) and the carets indicate small signal variables. This review of peak current mode control was necessary to now develop the model for average current mode control.

A typical circuit for average current mode control is shown in Fig. 1. Since the current loop block is a linear circuit, the frequency domain representation of $v_{CI}(t)$ is

$$\hat{V}_{CI}(s) = \hat{V}_C(s) + \frac{Z_F(s)}{R_{CLI}}\hat{V}_C(s) - \frac{Z_F(s)}{R_{CLI}}\left(R_I\hat{I}_L(s)\right) = \left(1 + G_{CL}(s)\right)\hat{V}_C(s) - G_{CL}(s)R_I\hat{I}_L(s) \quad (4)$$

where

$$Z_F(s) = \frac{sR_{CL2}C_{CL2} + 1}{s\left(sR_{CL2}C_{CLI}C_{CL2} + C_{CLI} + C_{CL2}\right)} \quad (5)$$

and the current loop compensation transfer function is defined as

$$G_{CL}(s) = \frac{Z_F(s)}{R_{CLI}} = \frac{\omega_{CLI}}{s}\cdot\frac{1 + s/\omega_{CLZ}}{1 + s/\omega_{CLP}} \quad (6)$$

with $\omega_{CLI} = 1/(R_{CLI}(C_{CLI}+C_{CL2}))$, $\omega_{CLZ} = 1/(R_{CL2}C_{CL2})$ and $\omega_{CLP} = (C_{CLI}+C_{CL2})/(R_{CL2}C_{CLI}C_{CL2})$. Here R_I is the total current sense gain given by $R_I = A_{CL}R_S$ where A_{CL} is the gain of the current sense amplifier (or current transformer) and R_S is the current sense resistor.

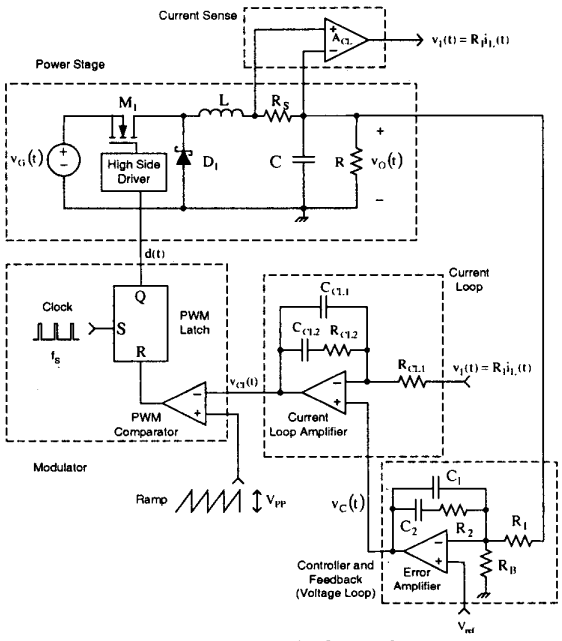

Fig. 1: Average Current Mode Control

TABLE II

FEEDFORWARD TERMS FOR CURRENT MODE CONTROL

Topology	G_G	G_O
Buck	$\frac{D^2T_SR_I}{2L}$	$\frac{(1-2D)T_SR_I}{2L}$
Boost	$\frac{(2D-1)T_SR_I}{2L}$	$\frac{(D')^2T_SR_I}{2L}$
Buck-Boost	$\frac{D^2T_SR_I}{2L}$	$-\frac{(D')^2T_SR_I}{2L}$

From Fig. 1 the voltage loop error amplifier transfer function, here called the controller, is given by

$$G_C(s) = -\frac{1}{R_I}\cdot\frac{sR_2C_2 + 1}{s\left(sR_2C_1C_2 + C_1 + C_2\right)} = -\frac{\omega_{CI}}{s}\cdot\frac{1 + s/\omega_{CZ1}}{1 + s/\omega_{CP1}} \quad (7)$$

with $\omega_{CI} = 1/(R_I(C_1+C_2))$, $\omega_{CZ1} = 1/(R_2C_2)$ and $\omega_{CP1} = (C_1+C_2)/(R_2C_1C_2)$. Equations 4 and 7 describe the portion of Fig. 2 below and including the $V_{CI}(s)$ signal node. Also in this figure the H term is the feedback voltage divider in the voltage loop, it is calculated from

$$H = \frac{R_B}{R_B + R_I} \quad (8)$$

where R_B is the dc bias resistor. Note that the current loop compensator (6) and the voltage loop controller (7) also appear as blocks in Fig. 2. It is important that the $1+G_{CL}(s)$ block includes the +1 term. Previous work ignored this and it turns out that it adds a low frequency zero to the control-to-output transfer function. The top half of this figure, from the $\hat{V}_{CI}(s)$ signal node and above, resembles peak current mode control and will now be explained.

The best way to understand the modulator and power stage is to build a working prototype and measure the transfer function from $\hat{V}_{CI}(s)$ to $\hat{V}_O(s)$. A UC3886 average current mode controller was used in the prototype circuit with the following component values: power stage M_1 is an IRF3315S, D_1 is a 32CTQ030, L = 20μH (with a DCR of R_L = 7.5mΩ), C = 330μF (with an ESR of R_C = 25mΩ), R = 2Ω; current sense and current loop compensation R_S = 50mΩ, A_{CL} = 10V/V, R_{CLI} = 15kΩ, R_{CL2} = 15kΩ, C_{CLI} = 220pF, C_{CL2} = 5600pF; and controller $R_B = \infty$, R_1 = 5.11kΩ, R_2 = 24.3kΩ, C_1 = 330pF and C_2 = 6800pF. The design procedure to calculate the current loop compensation component values is given in a later section. Note that R_B wasn't necessary since V_{ref} = 2V which is the desired output

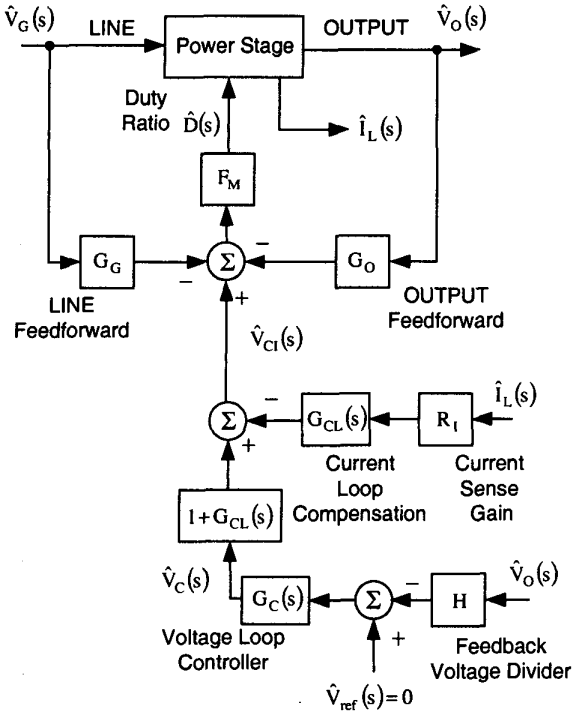

Fig 2: Average Current Mode Control Small Signal Model

voltage. The switching frequency, f_S, was approximately 100kHz and V_G was adjusted between 3V to 7.5V to vary the duty ratio. Although desired, a lower voltage MOSFET with a lower gate charge (less than 95nC) and $R_{ds,on}$ (less than 82mΩ) was not available at the time the circuit was built.

The $\hat{V}_{CI}(s)$ to $\hat{V}_O(s)$ transfer function was measured with an AP Instruments 102B Network Analyzer using the analog signal injection method. The signal was injected into the voltage loop for three duty ratios, D = 0.31, 0.50 and 0.75. The results are shown in Fig. 3. Both the current loop and voltage loop were closed for this measurement. This looks remarkably like the transfer function for the modulator and power stage of voltage mode control. For such a case, the low frequency gain is $F_M V_O/D$ and in this figure the solid lines represent the theoretical voltage mode modulator and power stage transfer function which include the resistance of the inductor (R_L) and the ESR of the capacitor (R_C) [8]. Therefore, the modulator gain for average current mode control is the same as voltage mode control and is approximately constant, given by

$$F_M = \frac{1}{V_{PP}} \qquad (9)$$

where V_{PP}, equal to 1.8V in the prototype circuit, is the peak-to-peak voltage of the ramp oscillator shown in Fig. 1. This was proposed in [6], here experimental results strengthen the concept.

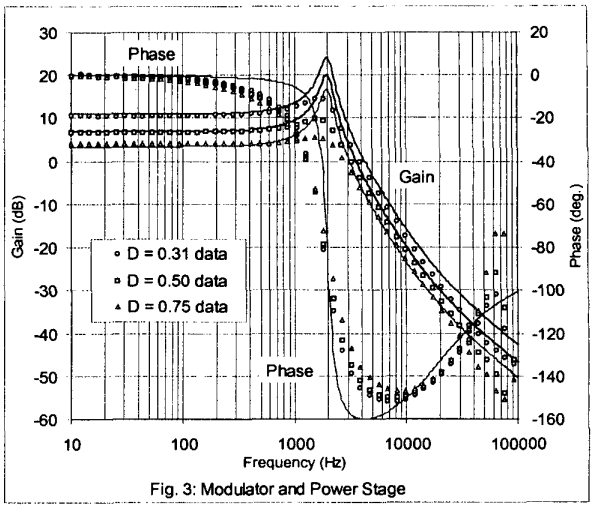

Fig. 3: Modulator and Power Stage

As was presented in [1, 2] the proposed non-linear modulator gain models the non-monotonic variation in the current loop – loop gain (simply called the current loop gain) as the duty ratio varies from a minimum to a maximum. This behavior seems to be a function of how much peak-to-peak ripple is on the output of the current loop amplifier, $v_{CI}(t)$, relative to the ramp peak-to-peak voltage. For low ripple conditions (9) is valid, for higher ripple conditions (9) is an approximation.

The final step in justifying the average current mode control diagram in Fig. 2 is to explain the G_G and G_O blocks. These feedforward blocks are new and expand on the work presented in [6]. Average current mode control may be considered as true state feedback since the average inductor current is sensed. Peak current mode control is an approximation of this behavior and one would expect that the two small signal control diagrams would have common features. One approach is to accept Fig. 2 with G_G and G_O as given in peak current mode control (Table II) and

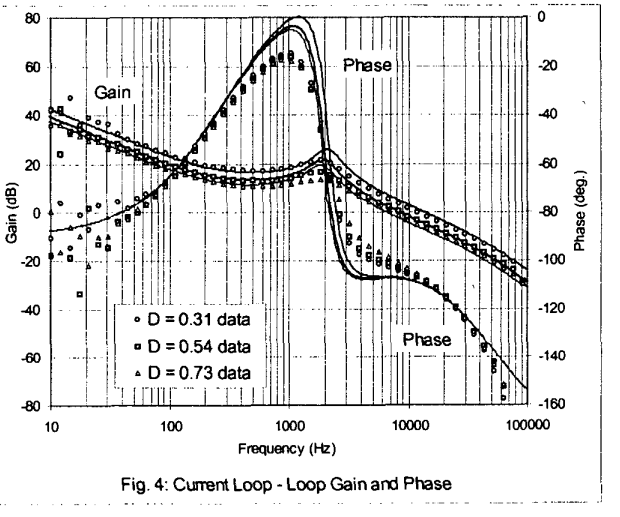

Fig. 4: Current Loop - Loop Gain and Phase

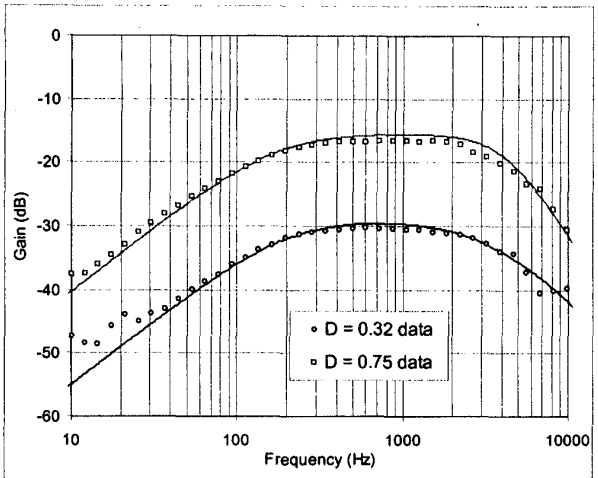

Fig. 5: Open Loop Line to Output $G_{OG}(s)$ Transfer Function

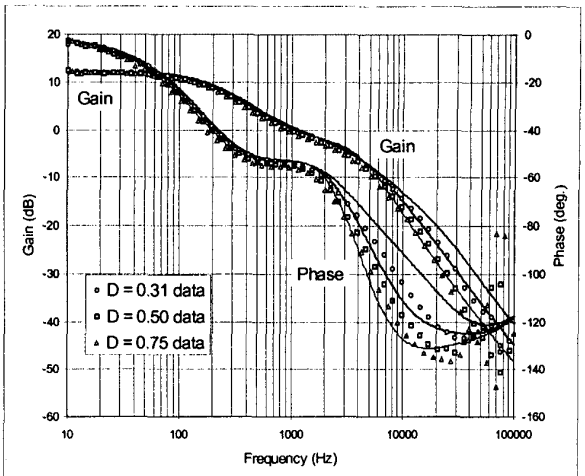

Fig. 6: Control to Output $G_{OC}(s)$ Transfer Function

compare the measured transfer functions and loop gains with the derived theoretical results. That is the approach taken here and continued in the next section.

III. EXPERIMENTAL VERIFICATION OF MODEL

Current loop gain was measured by injecting a signal into the current loop with the voltage loop open. Figure 4 shows the current loop gain, measured and theoretical, for D = 0.31, 0.54 and 0.73. The buck current loop gain may be derived using the techniques from [7], yielding

$$\frac{T_I(s)}{} = \frac{F_M R_I V_O (sRC+1)}{LDRCs^2 + LDs + DR + F_M R_I V_O R T_S (1-2D)/(2L)} G_{CL}(s). \quad (10)$$

This is the expression for the current loop gain ignoring R_L and R_C, however the theoretical results (solid lines) in Fig. 4 include these parasitic effects. It isn't difficult to include these terms while deriving the expressions, although some get too lengthy to present here. The biggest difference occurs at the resonant frequency (about 2kHz in this case) where (10) would show a higher Q and a commensurate change in phase at this frequency than what the solid lines in Fig. 4 depict. The results presented in Fig. 4 are encouraging and verifies, in part, the accuracy of the proposed model.

The next step is to measure the line-to-output $G_{OG}(s)$ transfer function (also called audio susceptibility) with the voltage loop open. To do this a bipolar operational power supply was used to provide a V_G with a superimposed small amplitude analog signal. The results are shown in Fig. 5 for D = 0.32 and D = 0.75 along with the theoretical results from the derived equation for the buck converter

$$G_{OG}(s) = \frac{RD^2(1-F_M R_I V_O T_S/(2L))s(s+\omega_{CLP})(1+s/\omega_{ESR})}{a_4 s^4 + a_3 s^3 + a_2 s^2 + a_1 s + a_0} \quad (11)$$

with $\omega_{ESR} = 1/(R_C C)$. In (11) T_S is the switching period ($1/f_S$) and

$a_4 = LDRC$,

$a_3 = LDRC\omega_{CLP} + LD$,

$a_2 = LD\omega_{CLP} + DR + F_M R_I V_O R T_S(1\text{-}2D)/(2L) + F_M R_I V_O RC\omega_{CLP}\omega_{CLI}/\omega_{CLZ}$,

$a_1 = DR\omega_{CLP} + F_M R_I V_O R T_S(1\text{-}2D)\omega_{CLP}/(2L) + F_M R_I V_O RC\omega_{CLP}\omega_{CLI} + F_M R_I V_O \omega_{CLP}\omega_{CLI}/\omega_{CLZ}$

and

$a_0 = F_M R_I V_O \omega_{CLP}\omega_{CLI}$.

This transfer function has four poles and three zeroes, one zero at the origin, a second is the current loop compensator pole and the third is the ESR zero. Equation 11 was derived neglecting the R_L and R_C series resistive terms of the inductor and capacitor. After which the $1+s/\omega_{ESR}$ factor was added since it appears in the transfer functions when R_L and R_C are not neglected. However, when these parasitic parameters (R_L and R_C) are included the expressions for the denominator "a" terms get unwieldy and for a well designed converter (11) is a good approximation.

The last transfer function to be measured is the control-to-output transfer function, $G_{OC}(s)$, and is plotted in Fig. 6 along with the theoretical result

$$G_{OC}(s) = \frac{F_M V_O R \omega_{CLP}\omega_{CLI}(1+s/\omega_{ESR})}{a_4 s^4 + a_3 s^3 + a_2 s^2 + a_1 s + a_0} N(s) \quad (12)$$

where

$$N(s) = 1 + \left(\frac{1}{\omega_{CLI}} + \frac{1}{\omega_{CLZ}}\right)s + \frac{s^2}{\omega_{CLI}\omega_{CLP}} \quad (13)$$

for the buck converter at three duty ratios, D = 0.31, 0.50 and 0.75. Notice that (12) has the same denominator as (11). The N(s) polynomial (13) also appears in the control-to-output transfer functions of the boost and buck-boost converters. Now that the model has been verified, a design procedure is suggested in the next section.

IV. DESIGN GUIDELINES

Procedures to design the current loop are given in [1, 6 & 9]. These are modified slightly and summarized below.

The current loop compensator is designed using a lag network with a high frequency pole (6). Place the pole (ω_{CLP}) between one-third and one-half of the switching frequency, this will attenuate switching noise. Place the zero (ω_{CLZ}) below the power stage resonant frequency given by $\omega_O = (LC)^{-1/2}$, a factor of one half is a good starting value. As ω_{CLZ} is reduced, the midband gain increases as does the current loop crossover frequency.

The last step is to solve for R_{CLI} in the current loop integrator gain, ω_{CLI}. It is desirable to maximize ω_{CLI} since it increases the current loop gain proportionally for all frequencies, but too much gain can cause excessive voltage ripple at the output of the current loop amplifier. This ripple may lead to clipping of the signal and possible switching instability. Therefore, there exists constraints on the maximum magnitude of the integrator gain, these are calculated at the switching frequency ($\omega_S = 2\pi f_S$) from

$$\left|G_{CL}(j\omega_s)\right| \le \min\left(\frac{2}{m_1 F_M T_S}, \frac{L}{F_M |V_O| R_I T_S}\right). \qquad (14)$$

The first constraint is presented in [6], it avoids clipping of the current amplifier at low duty ratios or high line, thus avoiding switching instabilities. The second constraint, given in [9], also avoids switching instability. In (14) the min(x, y) functional notation means the minimum of x or y and $|V_O|$ is the absolute value of V_O to address the buck-boost case ($V_O < 0$). To simplify the design an approximation for $|G_{CL}(s)|$ at $s = j\omega_S$ is R_{CL2}/R_{CL1}. However, this approximation is only exact if the compensator pole is actually placed beyond the switching frequency. It is more accurate to use $|G_{CL}(j\omega_S)|$. Some iteration may be necessary. The current loop design is now complete.

Closing the voltage loop is accomplished by using the control-to-output transfer function, given in general form, as

TABLE III

PARAMETER VALUES FOR AVERAGE CURRENT MODE CONTROL $G_{OC}(S)$ (15) IN CCM ($K = 1+\omega_{CLI}/\omega_{CLZ}$)

Para-meter	Buck	Boost	Buck-Boost
K_{OC}	$\frac{R}{R_I}$	$\frac{D'R}{2R_I}$	$\frac{D'R}{(1+D)R_I}$
ω_{Z1}	$\frac{1}{R_C C}$	$\frac{1}{R_C C}$	$\frac{1}{R_C C}$
ω_{Z2} RHP	∞	$-\frac{(D')^2 R}{L}$	$-\frac{(D')^2 R}{DL}$
ω_{Z3}, ω_{Z4}	$\frac{\omega_{CLP}}{2}\left(K \pm \sqrt{K^2 - 4\frac{\omega_{CLI}}{\omega_{CLP}}}\right)$	$\frac{\omega_{CLP}}{2}\left(K \pm \sqrt{K^2 - 4\frac{\omega_{CLI}}{\omega_{CLP}}}\right)$	$\frac{\omega_{CLP}}{2}\left(K \pm \sqrt{K^2 - 4\frac{\omega_{CLI}}{\omega_{CLP}}}\right)$
ω_{P1}	$\frac{1}{RC}$	$\frac{2}{RC}$	$\frac{1+D}{RC}$
ω_{P2}	ω_{CLP}	ω_{CLZ}	ω_{CLZ}
Q_{OC}	$\frac{\omega_{CLZ}}{\omega_{OC}}\left(1 + \frac{D}{F_M R_I V_O \omega_{CLI} C}\right)$	$\sqrt{\frac{F_M R_I V_O}{L}\frac{\omega_{CLI}}{\omega_{CLZ}\omega_{CLP}}}$	$\sqrt{\frac{F_M R_I (V_G - 2V_O)}{L(1+D)}\frac{\omega_{CLI}}{\omega_{CLZ}\omega_{CLP}}}$
ω_{OC}	$\sqrt{\frac{F_M R_I V_O}{LD}\omega_{CLI} + \frac{1}{LC}}$	$\sqrt{\frac{F_M R_I V_O}{L}\frac{\omega_{CLP}\omega_{CLI}}{\omega_{CLZ}}}$	$\sqrt{\frac{F_M R_I (V_G - 2V_O)}{L(1+D)}\frac{\omega_{CLP}\omega_{CLI}}{\omega_{CLZ}}}$

$$G_{OC}(s) = K_{OC}\frac{(1+s/\omega_{Z1})(1+s/\omega_{Z2})(1+s/\omega_{Z3})(1+s/\omega_{Z4})}{(1+s/\omega_{P1})(1+s/\omega_{P2})\left(1+\frac{s}{Q_{OC}\omega_{OC}}+\left(\frac{s}{\omega_{OC}}\right)^2\right)}. \quad (15)$$

The dc gain K_{OC}, the zeroes and the approximate poles are listed in Table III. These expressions are for CCM and are useful for design purposes. For the boost and buck-boost designs (and derived variants) in CCM a low frequency RHP zero exists in the control-to-output gain. Because of this, the voltage loop – loop gain (voltage loop gain) crossover frequency is limited to about one tenth of the RHP zero frequency.

The expressions for ω_{P1}, ω_{P2}, ω_{OC} and Q_{OC} are approximations. An analysis of the migration of the poles of $G_{OC}(s)$ as D varies from 0 to 1 for all converter designs (the boost and buck-boost converter equations are given in the Appendix) show some movement. The boost converter roots migrate the least amount, the buck-boost complex pole pair changes its imaginary component by a factor slightly more than 10. For the buck converter, however, both the real and imaginary parts of the poles are sensitive and migrate, even to the point of becoming all real, as D varies from 0 to 1. Therefore, for the buck converter the approximations given for ω_{P2}, ω_{OC} and Q_{OC} are valid for high D, under these conditions the voltage loop gain has the smallest phase margin. The expressions in Table III for the boost and buck-boost poles seem to track the actual $G_{OC}(s)$ pole migration fairly well.

For the component values used in the prototype circuit a brief description of the buck $G_{OC}(s)$ pole migration is now given. The lowest real pole, ω_{P1}, ($\approx$ 1/(RC)), stays real over the entire D range but varies slightly. For low D, less than about 0.3, there is one complex pole pair slightly below ω_{CLP} and a second real root at about ω_{CLZ}. From a D of about 0.3 to about 0.5 there are four real roots. Above approximately 0.5 there is one complex pole pair between the low frequency pole ω_{P1}, ($\approx$ 1/(RC)) and the higher frequency real pole, ω_{P2}, which is now approximately ω_{CLP}. Therefore it is wise to use (12, 17, and 20, refer to Appendix) for computer verification over the desired range of duty ratio, especially in the case of the buck converter (12), after the design is complete.

V. CONCLUSIONS

A small signal model for average current mode control in continuous conduction mode was derived and compared to experimental data. It was shown that it is reasonable to approximate the modulator gain as a constant. The feedforward terms used in peak current mode control were also necessary for average current mode control – experimental data compared with theory substantiates this approach. Approximate expressions for the buck, boost and buck-boost converters were given which will enable the engineer to design the control loops. Exact expressions for the current loop gain, control-to-output and line-to-output transfer functions were also provided which are useful in computer design verification programs.

APPENDIX

This appendix lists the exact expressions for the current loop gain, control-to-output and line-to-output transfer functions for the boost and buck-boost converters. As was done for the buck equations, block diagram manipulation and the Maple symbolic computer program were used to derive these expressions. The current loop gain for the boost converter is

$$T_I(s) = \frac{F_M R_I V_O (sRC+2) G_{CL}(s)}{LRCs^2 + (L - F_M R_I V_O D'T_S/2)s + D'^2R + F_M R_I V_O D'^3 RT_S/(2L)}. \quad (16)$$

The control-to-output transfer function is

$$G_{OC}(s) = \frac{F_M V_O R \omega_{CLP}\omega_{CLI}\left(\frac{-L}{RD'}s + D'\right)(1+s/\omega_{ESR})}{b_4 s^4 + b_3 s^3 + b_2 s^2 + b_1 s + b_0} N(s). \quad (17)$$

The line-to-output transfer function is

$$G_{OG}(s) = \frac{(c_3 s^3 + c_2 s^2 + c_1 s + c_0)(1+s/\omega_{ESR})}{b_4 s^4 + b_3 s^3 + b_2 s^2 + b_1 s + b_0} \quad (18)$$

where

$c_3 = F_M R_I V_O T_S(2D-1)/(2D')$,
$c_2 = D'R - F_M R_I V_O D'RT_S(2D-1)/(2L) + F_M R_I V_O T_S(2D-1)\omega_{CLP}/(2D')$,
$c_1 = D'R\omega_{CLP} - F_M R_I V_O D'RT_S\omega_{CLP}(2D-1)/(2L) + F_M R_I V_O \omega_{CLP}\omega_{CLI}/(D'\omega_{CLZ})$,
$c_0 = F_M R_I V_O \omega_{CLP}\omega_{CLI}/D'$,
$b_4 = LRC$,
$b_3 = LRC\omega_{CLP} - F_M R_I V_O D'T_S/2 + L$,
$b_2 = F_M R_I V_O RC\omega_{CLP}\omega_{CLI}/\omega_{CLZ} - F_M R_I V_O D'T_S\omega_{CLP}/2 + D'^2R + F_M R_I V_O D'^3 RT_S/(2L) + L\omega_{CLP}$,
$b_1 = F_M R_I V_O RC\omega_{CLP}\omega_{CLI} + D'^2R\omega_{CLP} + F_M R_I V_O D'^3 RT_S\omega_{CLP}/(2L) + 2F_M R_I V_O \omega_{CLP}\omega_{CLI}/\omega_{CLZ}$

and

$b_0 = 2F_M R_I V_O \omega_{CLP}\omega_{CLI}$.

The current loop gain for the buck-boost converter is

$$T_I(s) = \frac{F_M R_I (sRC(V_G - V_O) + V_G - 2V_O) G_{CL}(s)}{LRCs^2 + (L + F_M R_I V_O D'T_S/2)s + D'^2R + F_M R_I D'^3 RT_S(V_G - V_O)/(2L)}. \quad (19)$$

The control-to-output transfer function is

$$G_{OC}(s) = \frac{F_M R \omega_{CLP} \omega_{CLI} \left(\frac{V_O L}{RD'} s + D'(V_G - V_O) \right)(1 + s/\omega_{ESR})}{d_4 s^4 + d_3 s^3 + d_2 s^2 + d_1 s + d_0} N(s) \quad (20)$$

where $V_O < 0$ for the buck-boost converter and the line-to-output transfer function is

$$G_{OG}(s) = \frac{(e_3 s^3 + e_2 s^2 + e_1 s + e_0)(1 + s/\omega_{ESR})}{d_4 s^4 + d_3 s^3 + d_2 s^2 + d_1 s + d_0} \quad (21)$$

where

$e_3 = F_M R_I V_O T_S D^2/(2D')$,

$e_2 = F_M R_I D^2 D' R T_S (V_G - V_O)/(2L) - DD'R + F_M R_I V_O T_S D^2 \omega_{CLP}/(2D')$,

$e_1 = F_M R_I D^2 D' R T_S \omega_{CLP} (V_G - V_O)/(2L) - DD'R\omega_{CLP} + F_M R_I V_O D \omega_{CLP} \omega_{CLI}/(D' \omega_{CLZ})$,

$e_0 = F_M R_I V_O D \omega_{CLP} \omega_{CLI}/D'$,

$d_4 = LRC$,

$d_3 = LRC\omega_{CLP} + F_M R_I V_O D' T_S/2 + L$,

$d_2 = F_M R_I RC(V_G - V_O)\omega_{CLP}\omega_{CLI}/\omega_{CLZ} + D'^2 R + F_M R_I D'^3 R T_S (V_G - V_O)/(2L) + F_M R_I V_O D' T_S \omega_{CLP}/2 + L\omega_{CLP}$,

$d_1 = F_M R_I RC(V_G - V_O)\omega_{CLP}\omega_{CLI} + D'^2 R\omega_{CLP} + F_M R_I D'^3 R T_S (V_G - V_O)\omega_{CLP}/(2L) + F_M R_I (V_G - 2V_O)\omega_{CLP}\omega_{CLI}/\omega_{CLZ}$

and

$d_0 = F_M R_I \omega_{CLP} \omega_{CLI} (V_G - 2V_O)$.

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