Modeling and Practical Design Issues for Average Current Control

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Abstract – **This paper addresses modeling and practical design issues for PWM converters with average current control. A straightforward averaged modeling method is proposed, and the resulting models are shown to be accurate enough for practical design purpose. Limitations of previously published models that incorporate sampling effect are discussed. The proposed averaged model is then applied for stability analysis and control design. In particular, conditions under which switching instability may occur are identified, and design method that avoids the instability problem is presented. The proposed modeling and design methods are demonstrated and further validated by a prototype synchronous-switch buck converter with 5V input and 2V output.**

I. INTRODUCTION

Average current control [1] has been frequently used for controlling DC/DC as well as single-phase power factor correction (PFC) converters. Compared to peak current control, average current control has the following advantages: 1) no needs for an external compensation ramp, 2) increased current loop gain in DC and at low frequencies, and 3) improved immunity to noise in the sensed current signal. The increased DC and low-frequency gain of the current loop is especially attractive for single-phase PFC applications using boost-derived topologies, where it is desirable that the average, rather than the peak of the inductor current follows precisely a sinusoidal reference. High current loop gain in DC and at low frequencies is also a desirable feature for buck-derived converters used as current sources.

Modeling and design of average current control has been the subject of several technical papers and seminar notes [1-3]. Detailed design guidelines for the current compensator are provided in [1], which is a valuable reference for practicing engineers. In particular, optimum gain of the current compensator that maximizes current loop gain, yet avoids current loop subharmonic oscillation problem, is suggested in [1] for different topologies. However, it was found that this optimum gain often leads to high switching-frequency ripple in the current compensator output when the converter operates with narrow duty cycle. As a result, switching instability may occur.

Small-signal models for average current controlled PWM converters have been presented in [2] and [3]. These models have the following limitations: 1) They are all small-signal models, hence cannot be used for large-signal analysis; 2) Sampling effect is incorporated in certain form as a means to improve model accuracy, but adds complexity to the model. Inclusion of the sampling effect has proven to be valuable for improving the accuracy of averaged models for peak current control [4], but its effect in average current control is arguable. In terms of PWM process, average current control more closely resembles voltage-mode control (for both use an artificial triangular waveform for PWM) than peak current control. State-space averaged models without incorporating sampling effect have proven to be accurate up to half of the switching frequency in the case of voltage-mode controlled PWM converters. Considering this, it is legitimate to ask why the sampling effect needs to be considered in average current control, but not in voltage-mode control?

In this paper, straightforward state-space averaging is re-applied to average current controlled PWM converter (Section II). In this approach, a complete averaged model is obtained by combining the state-space averaged model of converter power stage with the model of the current compensator. The comparator that generates the PWM signal is simply modeled as a constant gain; the arguable, often confusing sampling effect is not considered. It will be shown that the resulting model is simpler, valid for large signal, and in fact also more accurate than previous models that take into account the sampling effect. Possible degrading of model accuracy under large ripple conditions is discussed, and it is shown that inclusion of sampling effect doesn't improve model accuracy in that case.

Section IV of the paper deals with current compensator design and switching instability problem. Conditions under which switching instability may occur are identified, and limitations of previous design method are discussed from this prospect. New design method that avoids the instability problem is presented. Finally, in Section V, a 5V-input/2V-output buck converter is used as an example to demonstrate the proposed design method. The buck converter uses synchronous switch to achieve high efficiency, and the control is implemented using a Unitrode control chip. Experimental results are presented as well.

II. AVERAGED MODELING

The average current control scheme is depicted in Fig. 1. Principle of this control method is as follows [1]: The inductor current, i_L, of the converter is sensed by a resistor, R_s, and compared with voltage v_c that represents the required average

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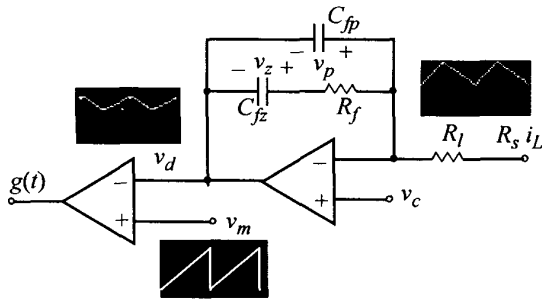

Fig. 1. Current compensator and PWM in average current control.

inductor current. The difference is amplified by the compensator consisting of R_l, R_f, C_{fz}, and C_{fp}, and the output of the amplifier is compared to the triangular PWM signal v_m at the comparator inputs to generate switching control signals for the converter. The transfer function of the compensator can be written as

$$H_c(s) = \frac{K_c(1 + s/\omega_z)}{s(1 + s/\omega_p)} \tag{1}$$

where the DC gain, K_c, the high-frequency pole, ω_p, and the zero, ω_z, are defined by

$$K = \frac{1}{R_l(C_{fp} + C_{fz})},\ \omega_z = \frac{1}{R_f C_{fz}},\ \omega_p = \frac{C_{fz} + C_{fp}}{R_f C_{fz} C_{fp}}.$$

As discussed in [2], the pole at the origin is used to boost DC and low-frequency gain of the current loop, the zero is needed for extending current loop crossover frequency, and the high-frequency pole is added to filter the switching ripple of the sensed current signal and increase noise immunity.

A. The Modeling Method

A PWM converter with average current control has three basic functional blocks: the power stage, the current compensator, and the modulator. The proposed modeling method is based on modeling the power stage and the modulator independently and then combining the results with the model of the current compensator (1) to form a complete model. The power stage is modeled by using straightforward state-space averaging. Assuming continuous conduction mode of operation (discontinuous conduction mode will be discussed later) and that the power stage is described by state-space models

$$\frac{d}{dt}\begin{bmatrix} i_L \\ v_C \end{bmatrix} = \boldsymbol{A}_1 \begin{bmatrix} i_L \\ v_C \end{bmatrix} + \boldsymbol{b}_1 v_g \quad \text{and} \quad \frac{d}{dt}\begin{bmatrix} i_L \\ v_C \end{bmatrix} = \boldsymbol{A}_2 \begin{bmatrix} i_L \\ v_C \end{bmatrix} + \boldsymbol{b}_2 v_g,$$

respectively, in the on- and off-time period of the switch, the averaged model of the power stage is simply

$$\frac{d}{dt}\begin{bmatrix} i_L \\ v_C \end{bmatrix} = d\left(\boldsymbol{A}_1 \begin{bmatrix} i_L \\ v_C \end{bmatrix} + \boldsymbol{b}_1 v_g\right) + (1-d)\left(\boldsymbol{A}_2 \begin{bmatrix} i_L \\ v_C \end{bmatrix} + \boldsymbol{b}_2 v_g\right) \tag{2}$$

where d is the duty ratio of the switch, and v_g the input voltage.

As in the modeling of voltage-mode controlled PWM converters, the modulator can be modeled by a constant gain

$$K_m = \frac{1}{V_m} \tag{3}$$

where V_m is the peak-to-peak voltage of the triangular carrier signal, v_m (see Fig. 1). Equations (2) and (3) may now be combined with the compensator model (1), which can also be put in a state-space form, to form a complete model for the converter, as represented by the diagram in Fig. 2. Notice that no small-signal assumption has been made thus far; hence the resulting model is valid for large-signal operation.

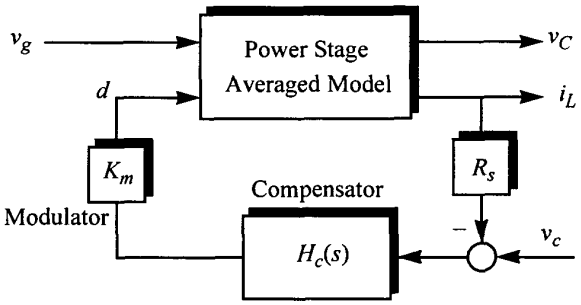

Fig. 2. Block diagram representation of the averaged model.

B. Small-Signal Model and Transfer Functions

If only small-signal behavior is of interests, the power stage averaged model can be linearized and the results can be represented using a matrix of transfer functions:

$$\begin{bmatrix} \hat{V}_C(s) \\ \hat{I}_L(s) \end{bmatrix} = \begin{bmatrix} G_{iv}(s) & G_{dv}(s) \\ G_{ic}(s) & G_{dc}(s) \end{bmatrix} \begin{bmatrix} \hat{V}_g(s) \\ \hat{D}(s) \end{bmatrix} \tag{4}$$

Various transfer functions can be derived. The same diagram in Fig. 2 also represents the small-signal model structure. This can be compared to that presented in [2] which includes a 2nd-order transfer function in current feedback path to represent the sampling effect, and additional paths for the duty ratio signal (so-called feedback and feedforward gain). The modulator gain used in [2] is dependent of the duty ratio as well as current compensator parameters, and is usually much lower than (3).

1) Current Loop Gain

With reference to (4) and Fig. 2, the current loop gain is calculated to be

$$T_c(s) = R_s K_m H_c(s) G_{dc}(s). \tag{5}$$

2) Control-To-Inductor Current Transfer Function

Voltage v_c is the control signal for the current loop. Note that the output of the current compensator (see Fig. 1) is directly offset by v_c, that is,

$$\hat{V}_d(s) = \hat{V}_c(s) + H_c(s)[\hat{V}_c(s) - R_s\hat{I}_L(s)].$$

Considering this, the following control-to-inductor current transfer function can be determined:

$$\frac{\hat{I}_L(s)}{\hat{V}_c(s)} = \frac{K_m[H_c(s)+1]G_{dc}(s)}{1+T_c(s)} \quad (6)$$

3) Control-To-Output Transfer Function

Note that, when ESR of the output capacitor is considered, the output voltage, v_0, is related to v_C by $\hat{V}_0(s) = (1 + r_C C)\hat{V}_C(s)$ Considering this, the control-to-output transfer function is

$$\frac{\hat{V}_o(s)}{\hat{V}_c(s)} = \frac{K_m(1+r_C Cs)[H_c(s)+1]G_{dv}(s)}{1+T_c(s)}. \quad (7)$$

Other transfer functions, such as audio susceptibility and output impedance, can be calculated in a similar way.

C. Examples

The state-space averaged model of a buck converter as shown in Fig. 3 is

$$L\frac{di_L}{dt} = dv_g - \frac{R(v_C - r_C i_L)}{R+r_C}, \quad C\frac{dv_C}{dt} = \frac{i_L R - v_C}{R+r_C}.$$

The transfer functions from duty ratio to inductor current and capacitor voltage are calculated to be

$$G_{dc}(s) = \frac{[1+(R+r_C)Cs]V_g}{R+(L+RCr_C)s+(RLC+r_C LC)s^2},$$

$$G_{dv}(s) = \frac{[1+r_C Cs]V_g}{R+(L+RCr_C)s+(RLC+r_C LC)s^2}.$$

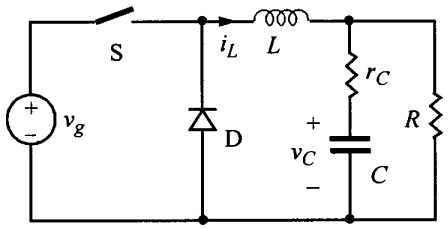

Fig. 3. Example buck converter topology.

As can be seen, both transfer functions are proportional to the input voltage. Using (5), the current loop gain is obtained as

$$T_c(s) = \frac{R_s K_m V_g[1+(R+r_C)Cs][1+H_c(s)]}{R+(L+RCr_C)s+(RLC+r_C LC)s^2}. \quad (8)$$

Apparently, the gain has a pole at the origin, a pair of complex poles, and a high-frequency pole, ω_p. Characteristics of the current loop gain will be discussed in detail in following sections.

D. Discontinuous Conduction Mode

The discontinuous conduction mode (DCM) of operation doesn't affect the overall structure of the model. The only thing that needs to be modified is the power stage averaged model. The averaged model presented in [5] and [6] can be readily applied for this purpose, and the rest of the analysis will be the same as outlined in the last subsection.

III. MODEL VALIDATION

To validate the averaged model, detailed switching model simulation of a buck converter has been conducted by using SABER. The parameters of the simulated buck converter are given in Table 1. In addition, a 5mΩ ESR has been considered for the output capacitor, and a 50mΩ resistor is put in series with the inductor to represent the switching losses as well as conduction losses of the switch and the inductor. Using the design method to be discussed in Section V, following parameters are chosen for the current compensator: ω_z = 6723 rad/s, ω_p = 1131x10^3 rad/s, K_c = 98000. The peak-to-peak value of the ramp signal, v_m, is 2.7V; hence the modulator gain is K_m = 1/2.7.

Table 1: Simulated Buck Converter Parameters

V_g	L	C	f_s	V_{out}	R
5V	13μH	750μF	180kHz	2V	0.43Ω

To determine the small-signal current loop gain, a 50Ω resistor is added in series with R_l (refer to Fig. 1), and a sinusoidal voltage is applied across it. The current loop gain is then determined by first simulating the circuit for long enough time to reach steady-state operation and then comparing the amplitudes and phases of the voltages on both sides of the 50Ω resistor at the frequency of the injected voltage. The results are shown in Fig. 4, where the solid lines represent the responses predicted by the transfer function (8), while the dots are simulated responses at some discrete frequencies. The predicted frequency responses agree very well with switching model simulation results up to about 1/3 of the switching frequency. The phase dependency becomes significant above 1/3 of the switching frequency. This is common to all average-based models because the converter response is then dependent on the phase of the disturbance, and this sensitivity is not picked up with an average-based LTI model. *The switching model simulation doesn't indicate the existence of the sampling effect, which has been included in previous models [2] and would create additional 180° phase shift at half the switching frequency.*

Control-to-inductor current and control-to-output voltage responses of the converter are simulated using similar method (by injecting a sinusoidal disturbance to the control voltage, v_c), and the results are given in Fig. 5 and Fig. 6 (represented by the dots), respectively, where they are also compared with the responses predicted by the transfer functions derived in the previous section (solid lines). Very good agreement between model predictions and simulated responses are again observed.

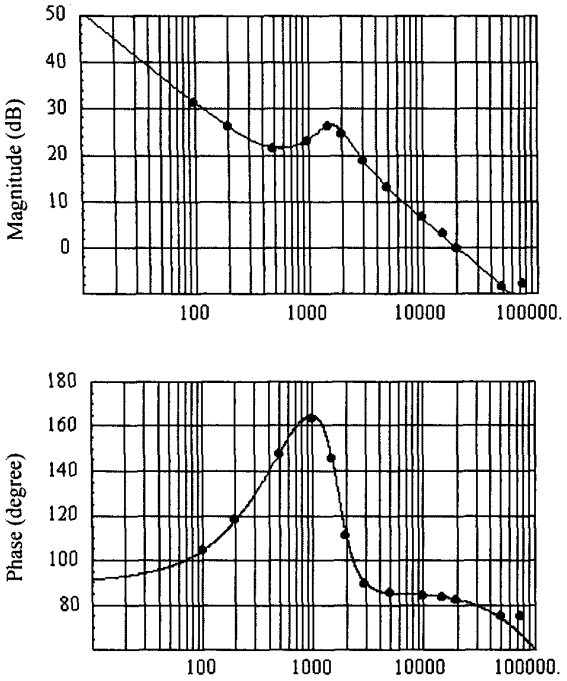

Fig. 4. Current loop gain of the example buck converter.

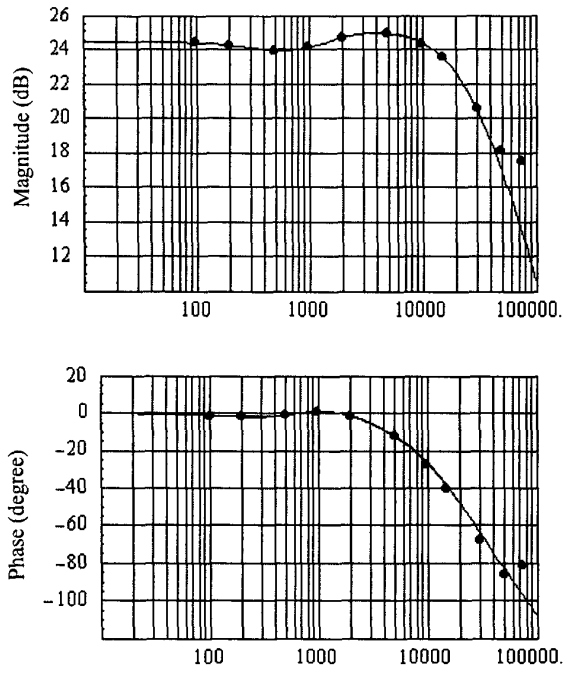

Fig. 5. Small-signal control-to-inductor current responses of the example buck converter.

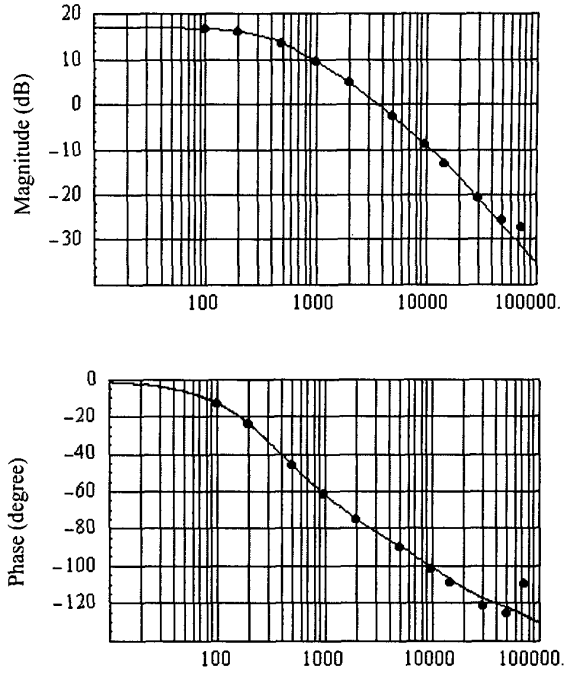

Fig. 6. Small-signal control-to-output voltage responses of the example buck converter.

It is known that the accuracy of average-based models may degrade if some variables, especially the input to the modulator, contains significant ripple. The peak-to-peak ripple voltage of the modulator input, v_d, in the previous simulation is measured to be 0.37V, or 30% of its DC value. To quantify the effect of ripple on averaged model accuracy, the example buck converter is also simulated with 15V as well as 20V input voltage (while the output voltage is kept at 2V). The peak-to-peak ripple in v_d is 120% of its DC level under 15V input, and more than 160% under 20V input. It is found that, *despite the high ripple in v_d, the predicted magnitude responses of the loop gain are as accurate as that at 5V input* - there is no observable discrepancy at up to 1/3 of the switching frequency.

The discrepancy in phase responses, however, does become larger as the ripple in v_d (relative to its DC level) increases. Fig. 7 shows the simulated phase responses of the loop gain under both input voltages (curve b for V_g = 15V and curve c for V_g = 20V), together with the responses predicted by the averaged model developed in this paper (curve a) as well as the previous model [2] that includes the sampling effect (curve d). The response predicted by either model is independent of the input voltage. However, simulated responses are indeed dependent of the input voltage (thus the ripple in v_d). As can be seen, the phase discrepancy starts from about 10kHz (about 1/20 of the switching frequency), increases as the frequency goes high, and is larger for higher ripple in v_d. But the total phase shift never reaches 180°, and it's also apparent that the new averaged model is still more accurate than the previous model.

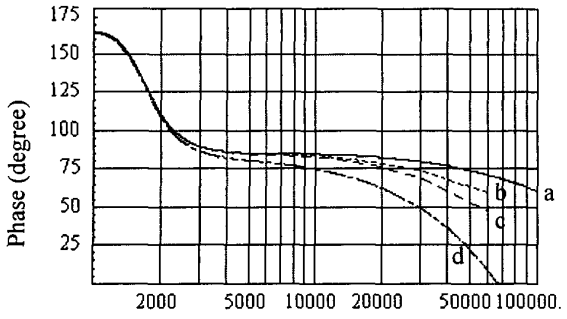

Fig. 7. Phase responses of the example buck converter with two different input voltages. From top down: a) prediction by the new model; b) switching model simulation results for V_g = 15V; c) switching model simulation results for V_g = 20V; d) prediction by the model presented in [2].

As will be discussed in the next section, the ripple in v_d needs to be limited in order to avoid switching instability problem in a practical circuit. For example, if the compensator gain is such determined that the peak-to-peak ripple in v_d does not exceed its DC value under maximum input voltage, the maximum phase discrepancy of the averaged model will be bounded to be less than 10 degrees under all operation conditions. For this reason, we believe that the accuracy of the new averaged model is satisfactory for practical design purpose. Nevertheless, it remains an important task to resolve this phase discrepancy problem and derive averaged models that are accurate also under large ripple conditions. We believe the method presented in [7] can be employed for this purpose. More results will be reported later.

IV. LOOP GAIN AND SWITCHING INSTABILITY

The current compensator has three parameters: the DC gain, K_c, the zero, ω_z, and the high-frequency pole, ω_p. The high-frequency pole shall be placed near the switching frequency in order to provide sufficient filtering for switching frequency ripple [1]. On the hand, the zero, ω_z, shall be placed before the resonant frequency, ω_0, of the power stage, usually between one third and half of ω_0, to maximize current loop crossover frequency [2].

As far as the design of K_c is concerned, an *optimum* value was suggested in [1], which was calculated by setting the upslope of the current compensator output in the off-time interval of the switch equal to the slop of the ramp signal v_m. The upslope of compensator output was simply calculated by multiplying the downslope of the voltage across current sensing resistor by the gain of the compensator at switching frequency, which is approximately R_f/R_l, that is,

$$\frac{R_f}{R_l}\cdot\frac{R_s V_0}{L} \le V_m f_s \quad \rightarrow \quad \frac{R_f}{R_l} \le \frac{V_m f_s L}{V_0 R_s}. \tag{9}$$

The compensator output may intersect the ramp signal again in the off-time period if the DC gain is higher than that defined by (9), leading to switching instability [1].

It was pointed out in [2] that switching instability may also occur when a converter operates with high input voltage, or, correspondingly, low duty ratio, even if K_c doesn't exceed the optimum value defined by (9). Indeed, since the small-signal model of [2] predicts more than 180 degrees phase shift of the current loop at 70kHz for the example buck converter (see Fig. 7), the current loop would be unstable if the magnitude crossover frequency is higher than 70kHz. Since the current loop gain at 70kHz is 0.45dB at 20V input voltage, which can be calculated from (8), the current loop would be unstable according to the model presented in [2]. However, simulation results don't indicate any stability problem under this operation condition, as the waveform in Fig. 8 shows.

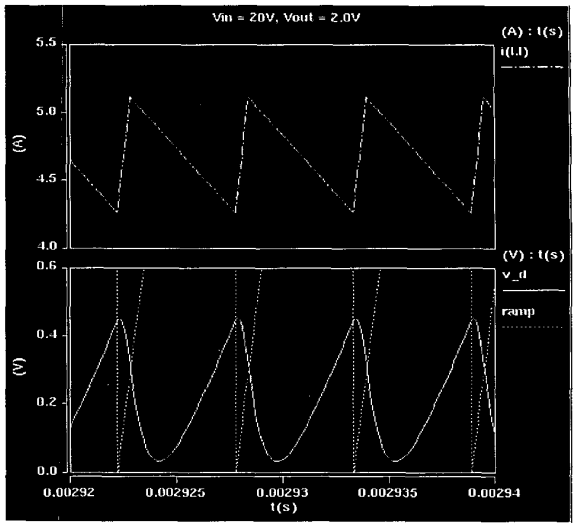

Fig. 8. Steady-state waveform of the example buck converter at V_g = 20V. Upper: inductor current; lower: current compensator output and the ramp signal.

The current amplifier in our SABER simulation has been implemented using an ideal op-amp which has unlimited output range. In a real circuit, however, v_d will be clipped if it reaches the lower limit of the amplifier output. If this happens, the slope of v_d may be different when the amplifier eventually comes out of the clipping mode, and switching instability will occur if the modified slope of v_d exceeds that of the ramp signal. Therefore, in a practical design, the ripple in v_d shall be low compared to its DC level to avoid clipping or clamping of current amplifier output. Since the ripple in v_d is relatively high when the converter operates at low duty ratio, caution must be taken especially at high input voltage. The optimum gain defined by (9), which is independent of the input voltage, doesn't take into account this potential ripple instability problem and is usually too high for low duty ratio operation. On the other hand, since the ripple instability is caused by non-linearity of the current amplifier, one shouldn't expect a small-signal model to be able to predict it [2].

A. DC Gain Selection

Since ripple instability is caused by the presence of high ripple in current compensator output, it can be avoided by limiting the ripple amplitude of v_d. Note that the peak-to-peak ripple of the voltage across current sensing resistor, R_s, is $m_1 dR_s/f_s$, m_1 being the upslope of the inductor current. Neglecting high-frequency components, the peak-to-peak ripple in v_d at switching frequency can be calculated by multiplying $m_1 dR_s/f_s$ by current amplifier gain at the switching frequency, that is,

$$v_d^{(f_s)} = \frac{m_1 dR_s}{f_s} \cdot |H_c(s)|_{s=2\pi jf_s}. \tag{10}$$

To avoid clipping of the current amplifier output, $v_d^{(f_s)}$ shall not exceed twice of the average of v_d. Therefore, the current compensator gain at switching frequency shall satisfy the following constraint in order to avoid switching instability:

$$|H_c(s)|_{s=2\pi jf_s} \le \frac{2V_m f_s}{m_1 R_s} \tag{11}$$

As an example, consider again the buck converter. Since the upslope of the current is $m_1 = (V_g - V_0)/L$, the current compensator gain at switching frequency shall not exceed

$$\frac{2V_m L f_s}{(V_g - V_0)R_s}. \tag{12}$$

Apparently, for high input voltage, the DC gain calculated from this expression is much lower than that defined by (9). On the other hand, however, the DC gain defined by (12) will exceed that by (9) for low input voltage. Therefore, the following relation shall be met in order to avoid switching instability at both high and low input†:

$$\frac{R_f}{R_l} \le \min\left[\frac{2V_m L f_s}{(V_{g,max} - V_0)R_s}, \frac{V_m L f_s}{V_0 R_s}\right] \tag{13}$$

The above limit applies to buck topology only. For boost and buck-boost topologies, the following limit has been derived:

$$\frac{R_f}{R_l} \le \min\left[\frac{2V_m L f_s}{V_{g,max} R_s}, \frac{V_m L f_s}{V_0 R_s}\right] \tag{14}$$

Once ω_p and ω_z have been defined, (13) or (14) can be used to determine the DC gain of the current compensator.

B. Analytical Approach

The discussions in the last subsection involve several approximations and are intended for easy applications. More accurate, analytical relations can be derived and used for rigorous designs. The key is the ripple component of current compensator output in steady-state operation, which has been calculated as follows:

1) For $t \in [0, d/f_s]$

$$\tilde{v}_d^{(1)} = \frac{K_c R_s e^{-\omega_p t}}{2f_s \omega_p \omega_z (\alpha - 1)}[a_0\alpha + a_1\alpha^d + a_2(1-\alpha)e^{t\omega_p}] \tag{15}$$

2) For $t \in [d/f_s, 1/f_s]$ ($t' = t - d/f_s$)

$$\tilde{v}_d^{(2)} = \frac{K_c R_s}{2\omega_p \omega_z}\left[a_3 + \frac{e^{-\omega_p t'}}{f_s(\alpha - 1)}(a_4\alpha + a_5\alpha^{1-d})\right] \tag{16}$$

where

$$\begin{aligned}
a_0 &= 2f_s(m_1 + m_2 + I_{pp}\omega_p) - 2(1-d)\omega_p m_2 \\
a_1 &= 2[d\omega_p m_1 - f_s(m_1 + m_2 + I_{pp}\omega_p)] \\
a_2 &= f_s(2m_1 - 2m_1 t\omega_p + I_{pp}\omega_p) \\
a_3 &= 2m_2 + I_{pp}\omega_p - 2m_2 t\omega_p \\
a_4 &= 2d\omega_p m_1 - 2f_s(m_1 + m_2 + I_{pp}\omega_p) \\
a_5 &= 2f_s(m_1 + m_2 + I_{pp}\omega_p) - 2(1-d)\omega_p m_2 \\
\alpha &= e^{\omega_p/f_s}
\end{aligned}$$

and m_1, m_2, and I_{pp} are the upslope, downslope, and peak-to-peak ripple of the inductor current. *The results are applicable to all single-inductor topologies.* More advanced design and analysis can be carried out based on (15) and (16). Details are omitted here because of the limit of space.

V. DESIGN EXAMPLE AND EXPERIMENTAL RESULTS

To demonstrate the modeling and design method discussed thus far, a prototype buck converter has been designed and built. The basic parameters of the buck converter have been given before in Table 1. Synchronous rectifier is used in order to achieve high efficiency. Both the high-side switch and the synchronous rectifier use Siliconix N-channel MOSFET Si4450DY, which has low $R_{DS(on)}$. The Unitrode integrated control chip UC3870 is selected because it can drive both FETs.

The Unitrode UC3870 has a built-in x10 amplifier which can be used to amplify the sensed current signal, allowing the use of small current sensing resistor. However, gain measurement of the amplifier indicates that it has a pole at about 180kHz. The switching frequency is therefore set at the same frequency so that this built-in pole can be utilized (as part of current compensator); that way, only the zero and the pole at origin need to be implemented in the current compensator, which can be realized using the circuit shown in Fig. 9.

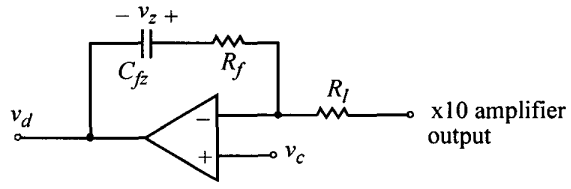

Fig. 9. Current amplifer used in the prototype buck converter.

†. Note that $|H_c(s)|_{s=2\pi jf_s} \approx R_f/R_l$, as used in [1].

The zero of the current compensator is set at 1kHz because the resonant frequency of the power stage is calculated to be around 2kHz. A 6mΩ current sensing resistor is used, and the maximum input voltage is assumed to be 15V. The peak-to-peak voltage of the built-in ramp signal is 2.7V, that is, V_m = 2.7V. With these, the current compensator gain (excluding that of the x10 amplifier) can be calculated from (13):

$$\frac{R_f}{R_l} \le \frac{2V_m L f_s}{(V_{g,max} - V_0)10R_s} = 16.2$$

Hence the following values are chosen for the passives shown in Fig. 9: R_l = 5.1 kΩ, R_f = 75 kΩ, C_{fz} = 2000 pF. This completes the design of the current loop.

The converter has been built on a prototype circuit board. The efficiency of the prototype converter is 86% at 5V input and 2V output, excluding the gate drive losses. Small-signal responses of the converter have also been measured using Vanable Frequency Analyzer. The dashed lines in Fig. 10 are the measured control-to-output voltage responses of the converter at 5V input and 2V output (load current equals to 4.6A). The solid lines are the responses predicted by the averaged model derived in Section II. As can be seen, the measurements are almost identical to model predictions.

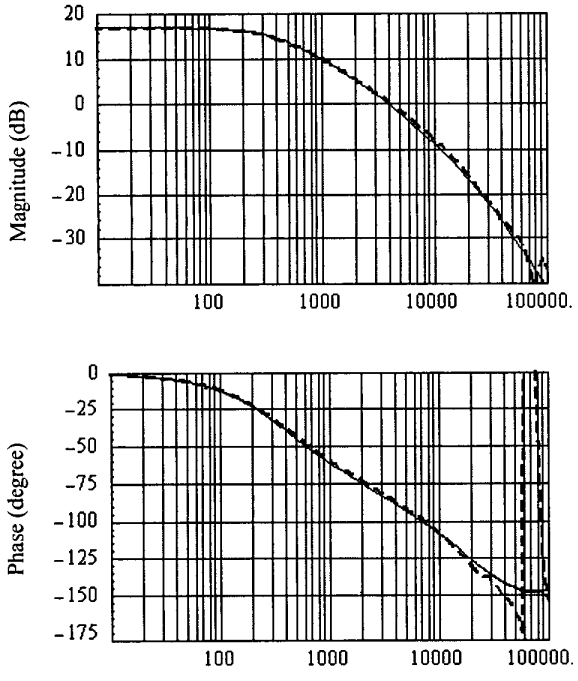

Fig. 10. Control-to-output-voltage response of the example buck converter. Solid line: model prediction; dashed line: experimental measurement.

VI. CONCLUSIONS

Large-signal averaged models for PWM converters using average current control have been presented. The model is obtained by combining the state-space averaged model of converter power stage with the model of the current compensator; the modulator is simply modeled as a constant gain. Detailed switching model simulation results indicated that the averaged model is accurate up to 1/3 of the switching frequency, as long as the ripple in the output of current compensator is not excessively high. The sampling effect, which was included in previous models and would create additional 180° phase shift at half the switching frequency in current loop gain response, was not observed.

Design and stability analysis of the current loop have been studied by use of the averaged model. It was found that switching instability may occur at high input voltage when the duty ratio is low. This instability is caused by clipping of the current amplifier when its output contains too high ripple, rather than by the lack of phase margin in the current loop, as was previously believed. Simple expressions have been derived as the limit for maximum current loop gain under which switching instability can be avoided. In addition, analytical solutions for the ripple components of current compensator output have been provided which can be used for more rigorous design and analysis. The design method has been demonstrated using a buck converter, and measured small-signal responses of the prototype converter verified the accuracy of the averaged model.

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