CURRENT MODE CONTROL OF A FULL BRIDGE DC-TO-DC CONVERTER WITH A TWO INDUCTOR RECTIFIER

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Abstract—In this paper, both peak current mode and average current mode control schemes will be investigated as applied to a full bridge PWM converter with a two inductor rectifier. The two inductor rectifier circuit offers reduced secondary side current rating and is most suitable for high current applications. With current mode control, the two inductor rectifier is modeled as two parallel connected buck converters.

I. INTRODUCTION

Since its inception in the late 1960s, current mode control has been widely applied to switch mode power supplies. This approach offers improved dynamic response and paralleling capability as compared to voltage mode control or duty cycle control by effectively eliminating the phase lag of the control to inductor current transfer function.

Two types of current mode control relevant to this work are peak and average current mode control. Peak current mode control (PCMC) offers inherent input voltage feedforward, pulse by pulse peak current limiting and consequent flux balance in isolated power supplies. Despite these advantages, PCMC incurs poor noise immunity, average current error, and instabilities in the absence of slope compensation. Alternatively, average current mode control (ACMC) exhibits accurate regulation of the programmed current and improved noise immunity without slope compensation.

In this paper, peak and average current mode control techniques are applied to a full bridge PWM converter with two inductor rectifier. The two inductor rectifier circuit offers reduced secondary side current rating compared to a full bridge or center tapped rectifier topology and is most suitable for high current applications. Furthermore, the two inductor rectifier can be modeled as two parallel buck converters. However the analysis differs from parallel connected modules in that the output inductors share the same output filter capacitor. This leads to cross coupling between the two converters which needs to be accounted for.

II. THE FULL BRIDGE PWM CONVERTER WITH A TWO INDUCTOR RECTIFIER

A full bridge PWM DC-to-DC converter with a two inductor rectifier was first proposed by the author in [1] and is shown in Fig. 1. The two inductor rectifier circuit was first reported in [2].

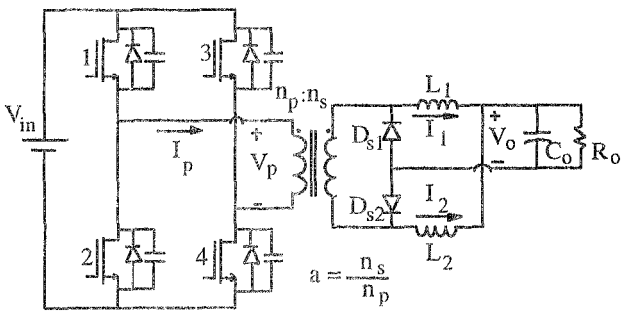

Fig. 1: A full bridge PWM DC-to-DC converter with a two inductor rectifier

The output voltage is controlled using phase shift control which allows zero voltage switching (ZVS) of the input bridge. The advantages of the two inductor rectifier circuit include lower secondary side current rating and hence lower losses, frequency doubling at the output capacitor, output current doubling in addition to an inherent 2:1 voltage ratio. This makes this converter attractive for high current, low voltage applications.

Three circuit modes can be identified for the converter of Fig. 1 within half a switching cycle: a power delivery mode (mode-I), a freewheeling mode (mode-II) and a commutation mode (mode-III) as shown in Fig. 2.

In phase shift control, when a switch in the leading edge is turned off, the energy available for achieving ZVS for the leading leg is the output filter energy. However, for the lagging leg switches, the only energy available for commutation is the leakage inductance energy. Hence, the leading leg switches achieve ZVS even at light loads, whereas ZVS is lost in the lagging leg switches below a certain load condition. Typical voltage and current waveforms are shown in Fig. 3. In the steady state the output voltage is given by

$$V_o = \frac{a \cdot D \cdot V_{in}}{2} \qquad (1)$$

Note that since the output current is the sum of the two output filter currents, the current rating of transformer secondary winding is one half the load current. This effectively reduces the ac winding losses in the transformer and output filter inductors.

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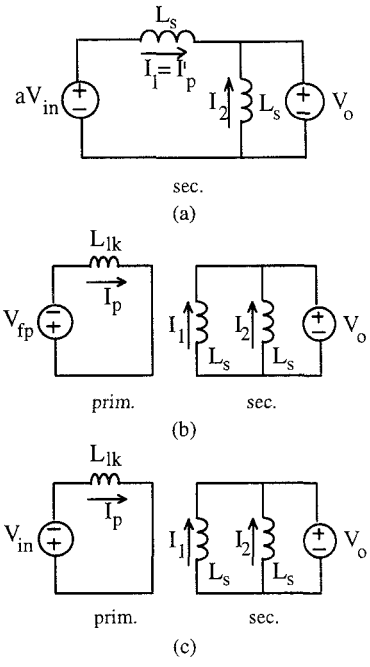

Fig. 2: Equivalent circuit modes of the converter

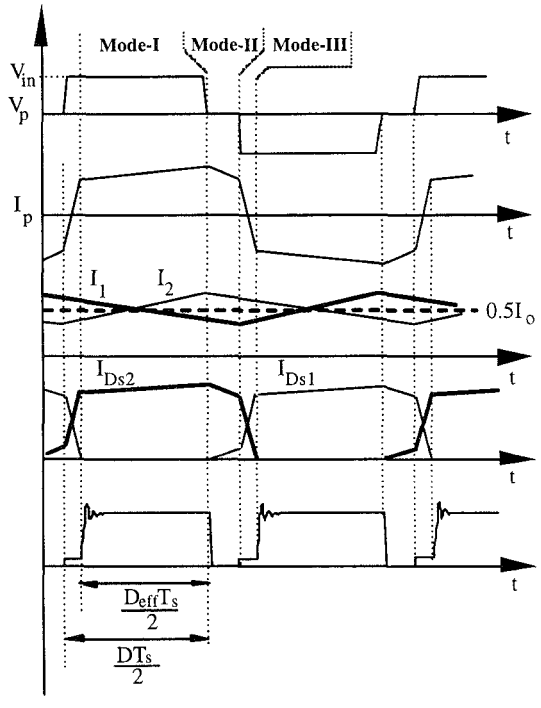

Fig. 3: Typical waveforms of the converter

Adopting current mode control ensures current sharing between the two output filter inductors. An inner current loop regulates the filter inductor currents while an outer voltage loop regulates the output voltage. In power supply applications operating in current limit, the inner current loop is the only active loop.

The two inductor rectifier can be modeled as two parallel connected buck converters. However the analysis differs from parallel connected modules in that the output inductors share the same output filter capacitor. This results in cross coupling between the two output inductor currents and care must be taken when designing the control loops.

III. Average Current Mode Control Implementation

Average current mode control is preferred for accurate control of the average output current and offers higher noise immunity compared with peak current control. This is advantageous in current limited power supplies where the supply current is limited. For this mode of control, current sensing can be performed either on the input side or the output side of the isolation transformer. However, with input current sensing, the negative slope of the output current needs to be synthesized which can result in an error if the output filter inductors are designed using swinging cores. On the other hand, output current sensing offers accurate measurement of the average output current but does not guarantee flux balancing in the isolation transformer. As a result, a dc blocking capacitor is needed to prevent flux imbalance. Figure 4 shows a converter schematic with average current control and output current sensing. In this configuration, a dc blocking capacitor (C_b) is utilized to prevent flux imbalance.

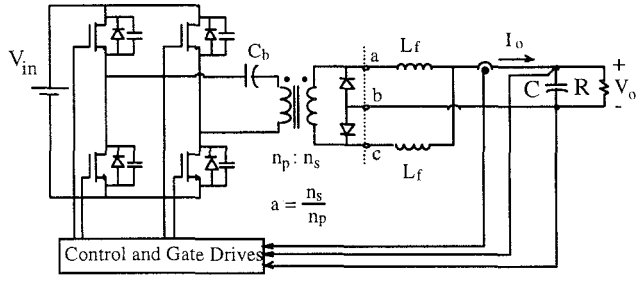

Fig. 4: Converter under average current mode control

Different techniques have been proposed to analyze switching converters utilizing current mode control [3-5]. The simplified PWM switch model will be used to analyze the system at hand and is shown in Fig. 5 [3].

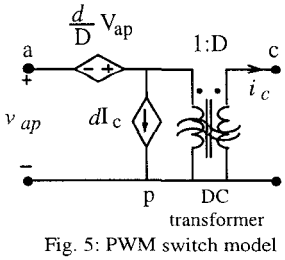

Fig. 5: PWM switch model

Since the output current is the sum of the two output filter inductor currents, the system can be reduced to two parallel connected buck converters [7,8]. Furthermore, since the

output filter inductor currents are not individually regulated, the small signal model of the system can be reduced to that of a single buck converter with average current mode control where the resultant filter inductor is the parallel combination of the two output inductors. Although each inductor current is not separately regulated, any difference between the average currents will be corrected by the input dc blocking capacitor which maintains zero net dc flux within the transformer. This guarantees that the two inductor currents remain equal. Note that the effective switching frequency of the resultant system is twice the switching frequency for the two filter inductor currents are out of phase which results in frequency doubling at the output.

Using the PWM switch model and assuming the transformer is ideal, the equivalent small signal model of the converter is shown in Fig. 6.

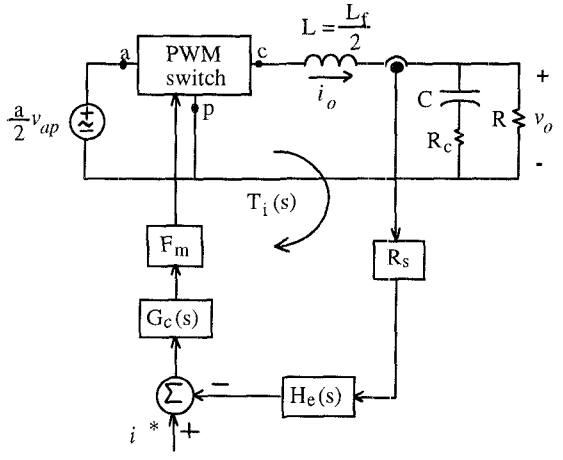

Fig. 6: Small signal model of the converter

Here, R_S is the sense resistor, $H_e(s)$ is the sampling gain, F_m is the modulator gain and $G_C(s)$ is the compensation transfer function. The sampling and modulator gains are defined in [6] to be

$$H_e(s) = 1 + \frac{s}{Q_z \omega_n} + \frac{s^2}{\omega_n^2} \tag{2}$$

$$F_m = \frac{1}{S_e + S_n'} \tag{3}$$

where,

$$Q_z = -\frac{2}{\pi} \tag{4}$$

$$\omega_n = \pi \cdot f_s \tag{5}$$

$$S_n' = S_n \cdot \omega_i \left[DT_s + \left(\frac{1}{\omega_z} - \frac{1}{\omega_p} \right) \cdot \left(1 - e^{-\omega_p DT_s} \right) \right] \tag{6}$$

In average current mode control, a possible current compensation transfer function is given by

$$G_c(s) = \frac{k_i \cdot \left(1 + \frac{s}{\omega_z} \right)}{s \cdot \left(1 + \frac{s}{\omega_p} \right)} \tag{7}$$

This transfer function represents an integrator followed by a lead-lag network. To ensure stability, the zero should be placed before the power stage filter frequency of the current loop where the phase shift of the integrator is canceled by the zero at half the switching frequency. The pole is normally placed above half the switching frequency to roll off the gain and thereby eliminate high frequency noise. Furthermore, this pole placement minimizes interaction with the current loop.

By straightforward analysis, the control to output current loop transfer function is given by

$$T_i(s) = R_s \cdot H_e(s) \cdot G_c(s) \cdot F_m \cdot F_i(s) \tag{11}$$

where

$$F_i(s) = \frac{V_{ap}}{R} \cdot \frac{1 + RCs}{LCs^2 + \left(R_c C + \frac{L}{R} \right) \cdot s + 1} \tag{12}$$

is the direct (forward) gain transfer function.

The loop transfer function for a 5kW converter were computed using MATLAB and the results are shown in Fig. 7 (see appendix A).

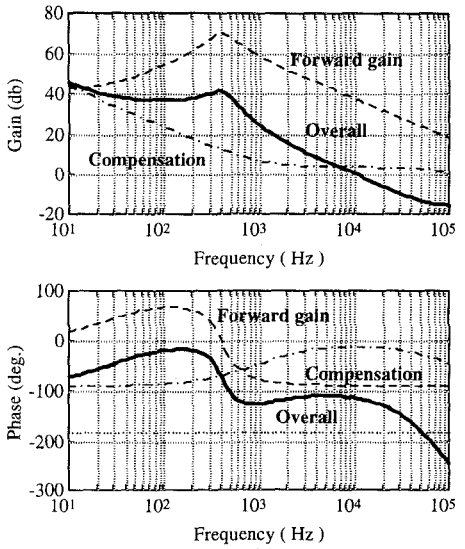

Fig. 7: Loop transfer function with average current control

It is clear from the above figure that the current loop can be stabilized with proper compensator design and without slope compensation. In fact, the compensator gain can be adjusted in a similar fashion to adding slope compensation in peak current mode systems. The gain margin of the current loop is 13.5dB and the phase margin is 67.7° while the current loop bandwidth is 10kHz.

The corresponding closed loop transfer function of the system is shown in Fig. 8 and the output current step response is shown in Fig. 9.

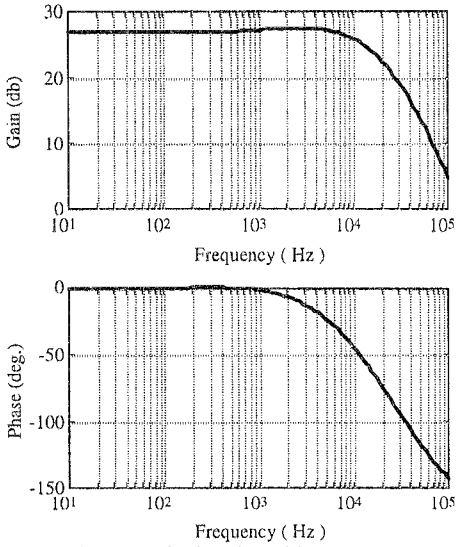

Fig. 8: Closed loop transfer function with average current control

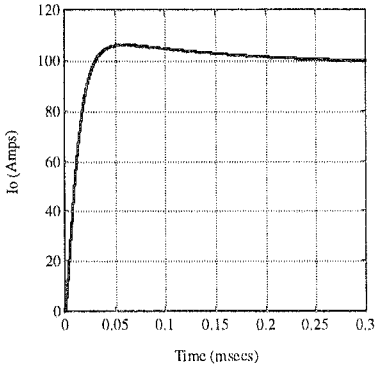

Fig. 9: Output current step response with average current control

As expected, the output current overshoot is low (5%) and the system reaches steady state in 0.3ms.

To verify the analysis results, a SPICE average model of the converter was simulated. In this case, the system was modeled as two parallel connected buck converters with a single output current loop. The resultant current loop transfer function is shown in Fig. 10 while the step response of the converter is shown in Fig. 11. It is clear from these figures that the simulation data match the analytical ones. Note also that the output filter current response is the same as the total output current.

III. Peak Current Mode Control Implementation

In applications where flux balancing is required on the primary side of the transformer and dc blocking capacitors are not used, peak current control can be adopted to ensure current sharing between the two inductors.

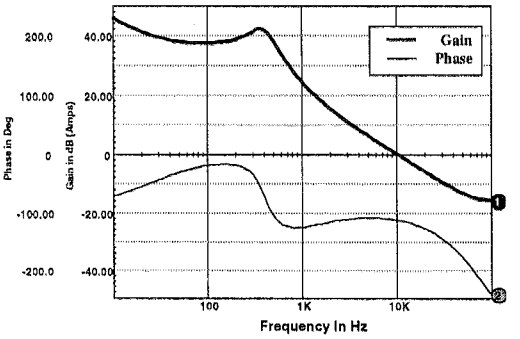

Fig. 10: Loop transfer function with average current control

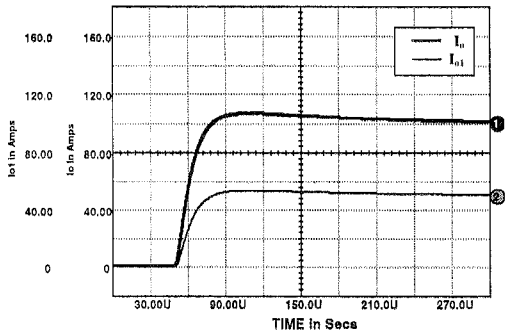

Fig. 11: Output currents step response with average current control

Unlike average current mode control, since peak current control regulates the peak of the inductor currents, the average output current may not be regulated. In this case, the negative slope needs to be reconstructed or an outer average current loop can be used to regulate the output current.

The implementation of the peak current loop control is similar to that of average current control except that the current sensing is done on the primary side of the transformer and no dc blocking capacitor is used. In this case, the switch currents in one leg can be sensed using current transformers. This offers one more level of protection since an active switch current limit is implemented.

The small signal equivalent circuit with peak current mode control is shown in Fig. 12 [9]. Note that each of inductor currents are driven at half the actual duty cycle of the converter. Hence, in the small signal model, the duty cycle D needs to be halved.

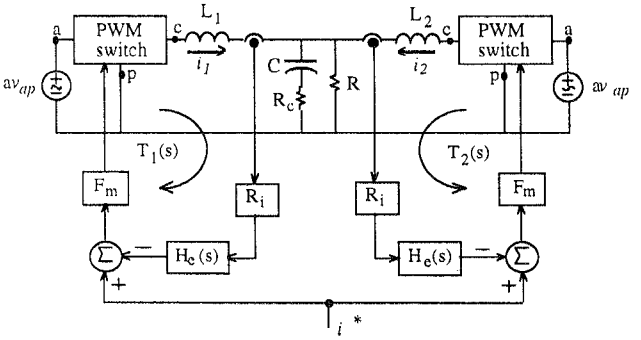

Fig. 12: Small signal model with peak current mode control

In contrast to average current mode control small signal model, the peak current small signal model is more involved in that the two converters are coupled via the common output filter capacitor. As a result, the system can no longer be reduced to that of a single buck converter with peak current control. The equivalent control block diagram of the system under peak current mode is shown in Fig. 13.

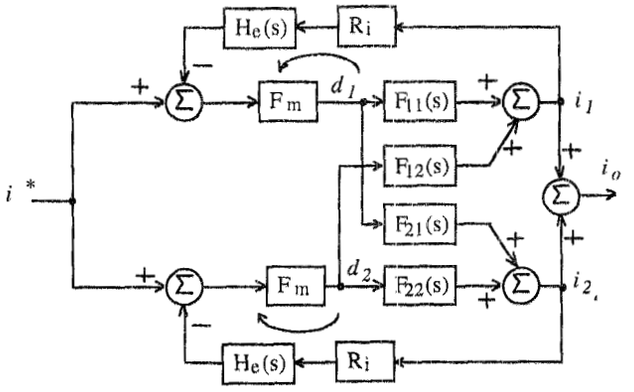

Fig. 13: Block diagram of the peak current control model

The transfer functions are computed using the average PWM switch model as shown in Fig. 14.

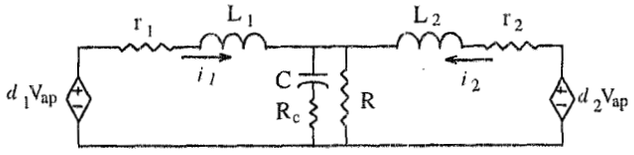

Fig. 14: Small signal equivalent circuit

The direct (forward) gain transfer function is given by [10]

$$F_{11}=\frac{V_{ap}}{L_1+L_2}\cdot\frac{L_2Cs^2+\left(R_pC+\frac{L_2}{R_t}\right)\cdot s+\frac{R}{R_t}}{s\cdot\left[L_pCs^2+\left(R_pC+\frac{L_p}{R_t}\right)\cdot s+\frac{R}{R_t}\right]} \quad (13)$$

where

$$F_{ij}=i_i/d_j \quad (14)$$

The cross coupled transfer function is given by

$$F_{12}=\frac{-V_{ap}}{L_1+L_2}\cdot\frac{R_pCs+\frac{R}{R_t}}{s\cdot\left[L_pCs^2+\left(R_pC+\frac{L_p}{R_t}\right)\cdot s+\frac{R}{R_t}\right]} \quad (15)$$

where

$$L_p=L_1//L_2 \quad (16)$$

$$R_p=R//R_c \quad (17)$$

$$R_t=R+R_c \quad (18)$$

Note that for $L_1=L_2$, $F_{21}=F_{12}$ and $F_{22}=F_{11}$.

To guarantee stability, each loop of the system must be stable. Two current loops can be identified, a direct loop associated with each current with its corresponding duty cycle and a cross coupled loop with the complementary duty cycle. These loops are given by,

$$T_{11}(s)=T_{22}(s)=R_i\cdot H_e(s)\cdot F_m\cdot F_{11}(s) \quad (19)$$

$$T_{12}(s)=T_{21}(s)=-R_i^2\cdot H_e^2(s)\cdot F_m^2\cdot F_{12}(s)\cdot F_{21}(s) \quad (20)$$

Here, the negative sign of T_{12} and T_{21} implies that the phase lag at the cross over frequency should be less than 360° as opposed to the conventional 180°.

The control to output transfer function may be evaluated as

$$\frac{i_1}{i^*}=\frac{F'_{11}+F'_{21}+F'_{11}F'_{22}H'_e-F'_{12}H'_eF'_{21}}{1+\left(F'_{11}+F'_{22}+F'_{11}F'_{22}H'_e-F'_{12}H'_eF'_{21}\right)\cdot H'_e} \quad (21)$$

where

$$F'_{ij}=F_m\cdot F_{ij} \quad (22)$$

$$H'_e=R_s\cdot H_e \quad (23)$$

The condition for instability of the control to output transfer function (21) is

$$\left(F'_{11}+F'_{22}+F'_{11}F'_{22}H'_e-F'_{12}H'_eF'_{21}\right)\cdot H'_e=-1 \quad (24)$$

which imposes an additional criteria for overall system stability.

The converter of appendix A was further analyzed using MATLAB with peak current mode control. The direct and cross coupled loop transfer functions are shown in Fig. 15.

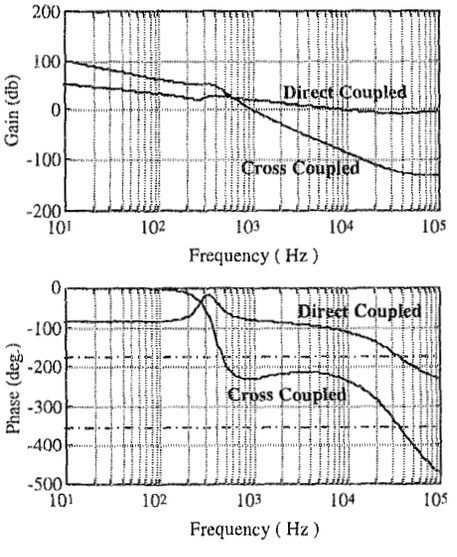

Fig. 15: Direct and cross coupled loop gains

As shown above, both loops can be stabilized with slope compensation. In this case, the added slope, S_e is assumed to

be one half the down slope of the output filter inductor currents, S_f or

$$S_e = -\frac{1}{2}S_f = \frac{R_i V_o}{2L} \qquad (25)$$

Again, note that the cross coupled loop phase margin is computed in reference to 360°.

The stability condition of (24) was evaluated and the results are shown in Fig. 16. The loop transfer function for a single converter case is overlaid for reference.

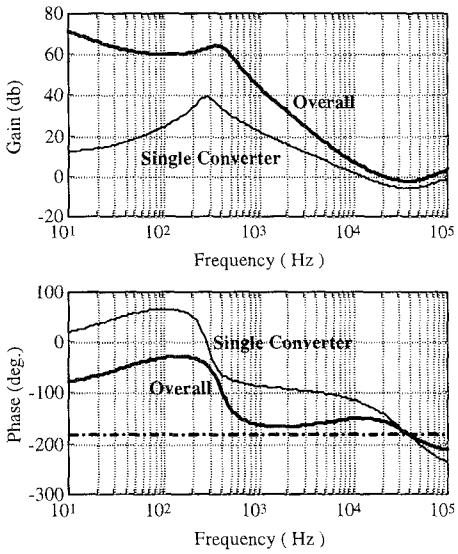

Fig. 16: Loop gains with peak current control, $S_e = -0.5 \cdot S_f$

As expected, the loop transfer response of a single converter is stabilized with the addition of slope compensation. Unlike the single converter case, the overall loop response of the system has higher gain and the phase characteristics reveal the presence of a low frequency pole and a high frequency zero which reduces the relative stability of the of the system. To improve stability of the current loop, more slope compensation may be added. Figure 17 shows the loop response with additional slope compensation where $S_e = -S_f$. The resultant gain margin is 6.5dB while the phase margin is 45°. The closed loop transfer function of the system is shown in Fig. 18.

A SPICE average model of the converter was simulated to verify the analysis results presented above. The system was modeled as two parallel connected buck converters with two individual peak current loops. The resultant closed loop transfer function is shown in Fig. 19, while the step response of the converter is shown in Fig. 20. As shown in Fig. 19, the simulated loop response matches the analytical model of Fig. 18.

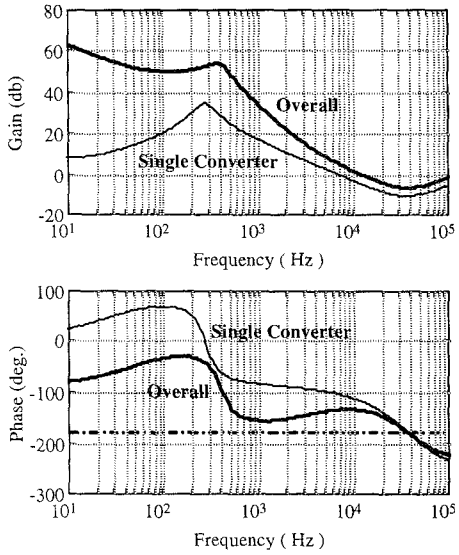

Fig. 17: Loop gains with peak current control, $S_e = -S_f$

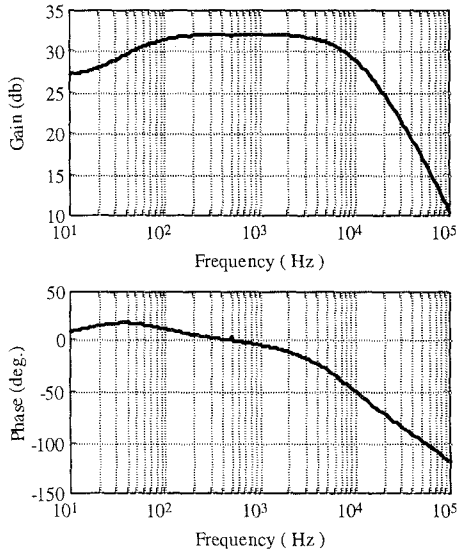

Fig. 18: Closed loop gains with peak current control, $S_e = -S_f$

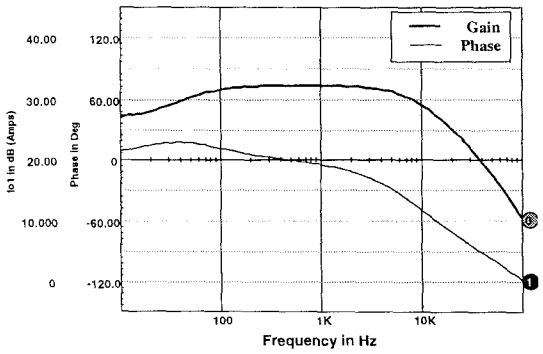

Fig. 19: SPICE loop gains with peak current control, $S_e = -S_f$

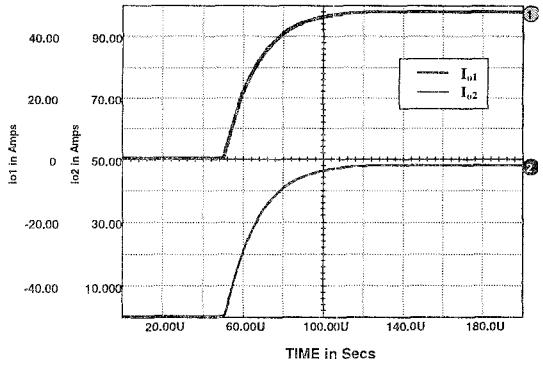

Fig. 20: Step response under peak current mode control

IV. CONCLUSIONS

In this paper, the analysis and implementation of peak and average current mode control techniques applied to a full bridge PWM converter with two inductor rectifier were discussed. The two inductor rectifier circuit offers reduced secondary side current rating compared to a full bridge or center tapped rectifier topology and is suitable for high current applications. Furthermore, the two inductor rectifier can be modeled as two parallel buck converters.

In average current mode control, the two converters are reduced to a single converter operating at twice the switching frequency. An integrator in series with a lead lag network ensures stability of the current loop. In contrast, the system in peak current mode control cannot be reduced to that of a single buck converter. This is due to the presence of cross coupling between the two converters for the output inductors share the same output filter capacitor. It has been shown that unlike the single converter case, the relative stability of the overall peak current loop is less than that of the single loop. As a result, more slope compensation may be required to improve the relative stability of the system.

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Appendix A:

The analyzed 5kW converter data:

V_{in}=320 V	V_o=48 V,	I_o=100 A
R=0.55 Ω	a=2.5	f_s=75 kHz
L_f=30 μH	C_o=10000 μF	R_c=20 mΩ
R_s=0.024 Ω	R_i=0.045 Ω	V_p=5V (ramp peak)