MC34063A

DC-to-DC Converter Control Circuits

DESCRIPTION

The MC34063A Series is a monolithic control circuit containing the primary functions required for DC-to-DC converters. These devices consist of an converters. Temperature compensated reference, Comparator，controlled duty cycle oscillator with an active current limit circuit，driver and high current output switch. This series was specifically designed to be incorporated in Step-Down and Step-Up and Voltage applications with a minimum number of external components.

The MC34063 is available in the plastic DIP-8, SOP-8 and SOIC-8 package.

Features

- Operation from 3.0V to 40 V Input
- Low Standby Current
- Current limiting
- Output Switch current to 1.5A
- Output Voltage Adjustable
- Frequency Operature to 100kHz
- Precision 2% Reference

APPLICATION

- Battery Chargers
- NICs/Switches/Hubs
- ADSL Modems
- Negative Voltage Power Supplies

ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	40	V_{dc}
Comparator Input Voltage Range	V_{IR}	-0.3 to +40	V_{dc}
Switch Collector voltage	$V_{C(switch)}$	40	V_{dc}
Switch Emitter Voltage(V_{PIN}=40V)	$V_{E(switch)}$	40	V_{dc}
Switch Collector to Emitter Voltage	$V_{CE(switch)}$	40	V_{dc}
Drive Collector Voltage	$V_{C(driver)}$	40	V_{dc}
Driver Collect Current(Note 1)	$I_{C(dirver)}$	100	mA
Switch Current	I_{SW}	1.5	A
Operating Junction Temperature	T_J	+150	℃
Operating Ambient Temperature Range	T_A	0 to +70	℃
Storage Temperature Range	T_{stg}	-65 to +150	℃

ELECTRICAL CHARACTERISTICS

(VCC=5.0 V, Ta=Tlow to Thigh,unless otherwise specified.)

Characteristics	Symbol	Min	Type	Max	Unit
OSCILLATOR					
Frequency (V_{pin5}=0V,C_T=1.0nF,T_A=25℃)	f_{OSC}	24	33	42	KHz
Charge Current(V_{CC}=5.0V to 40 V,T_A=25℃)	I_{CHG}	24	35	42	uA
Discharge Current(V_{CC}=5.0V to 40V,T_A=25℃)	I_{dischg}	140	220	260	uA
Discharge to Charge Current Ratio (Pin 7 to V_{CC},T_A=25℃)	I_{dischg}/I_{chg}	5.2	6.5	7.5	---
Current Limit Sense Voltage(I_{cha}=I_{discha};T_A=25℃)	$V_{ipk(sence)}$	250	300	350	mV
OUTPUT SWITCH (NOTE 2)					
Saturation Voltage, Darlington Connection (I_{SW}=1.0A,Pins 1,8 connected)	$V_{CE(sat)}$	---	1.0	1.3	V
Saturation Voltage, Darlington Connection (I_{SW}=1.0A,R_{pin8}=82 to V_{CC}, Forced â≈20)	$V_{CE(sat)}$	---	.045	0.7	V
DC Current Gain(I_{SW}=1.0A,V_{CE}=5.0V,T_A=25℃)	h_{FE}	50	75	---	---
Collector Off-State Current (V_{CE}=40V)	$L_{C(off)}$	---	40	100	uA
COMPARATOR					
Threshold Voltage (T_A=25℃) (T_A=T_{low} to T_{high})	V_{th}	1.225 1.21	1.25 ----	1.275 1.29	V
Threshold Voltage Line Regulation (V_{CC}=3.0V to 40V)	Reg_{line}	---	1.4	5.0	mV
Input Bias Current(V_{in}=0V)	L_{IB}	---	-20	-400	nA
TOTAL DEVICE					
Supply Current (V_{CC}=5.0V to 40V, C_T=1.0nF, Pin7=V_{CC}, Vpin5>Vth, Pin2=Gnd, remaining pins open)	I_{CC}	---	---	4.0	mA

NOTES:

1. Maximum package power dissipation limits must be observed.
2. Low duty cycle pulse techniques are used during test to maintain junction temperature as close to ambient temperature as possible.

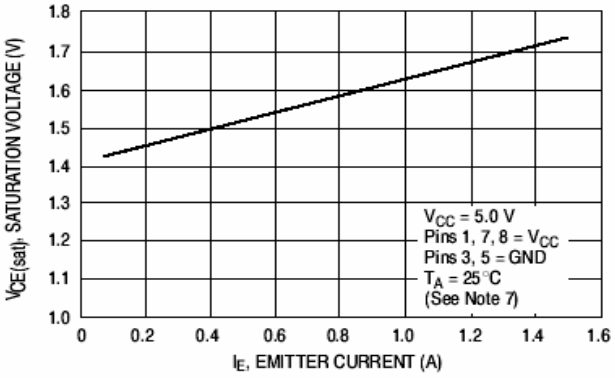


Figure 4. Emitter Follower Configuration Output Saturation Voltage versus Emitter Current

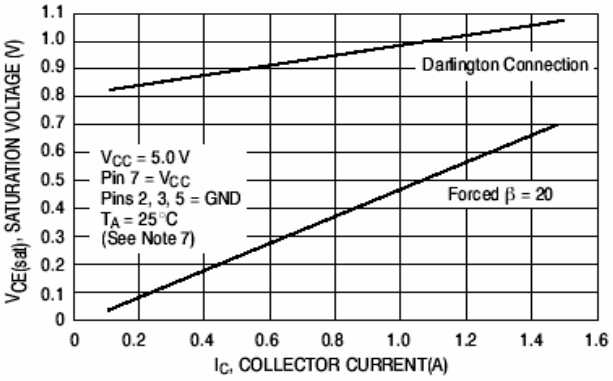


Figure 5. Common Emitter Configuration Output Switch Saturation Voltage versus Collector Current

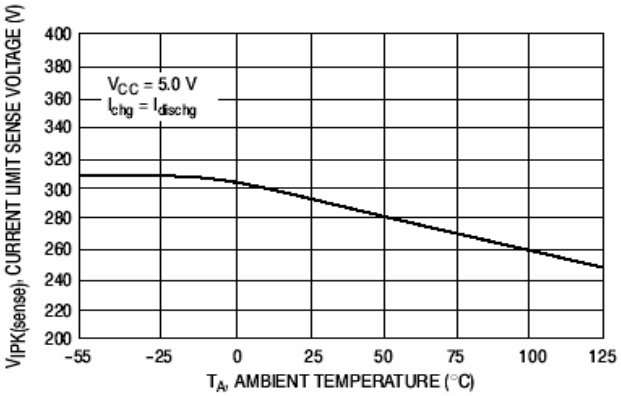


Figure 6. Current Limit Sense Voltage versus Temperature

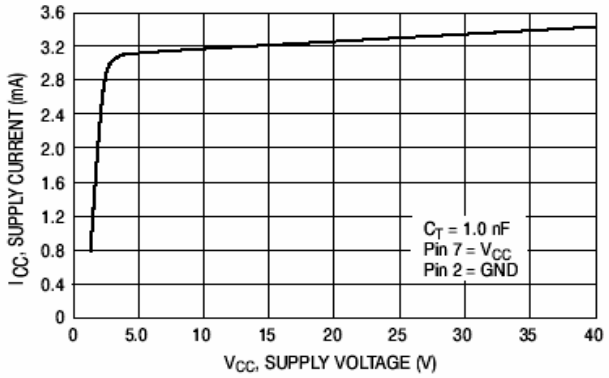
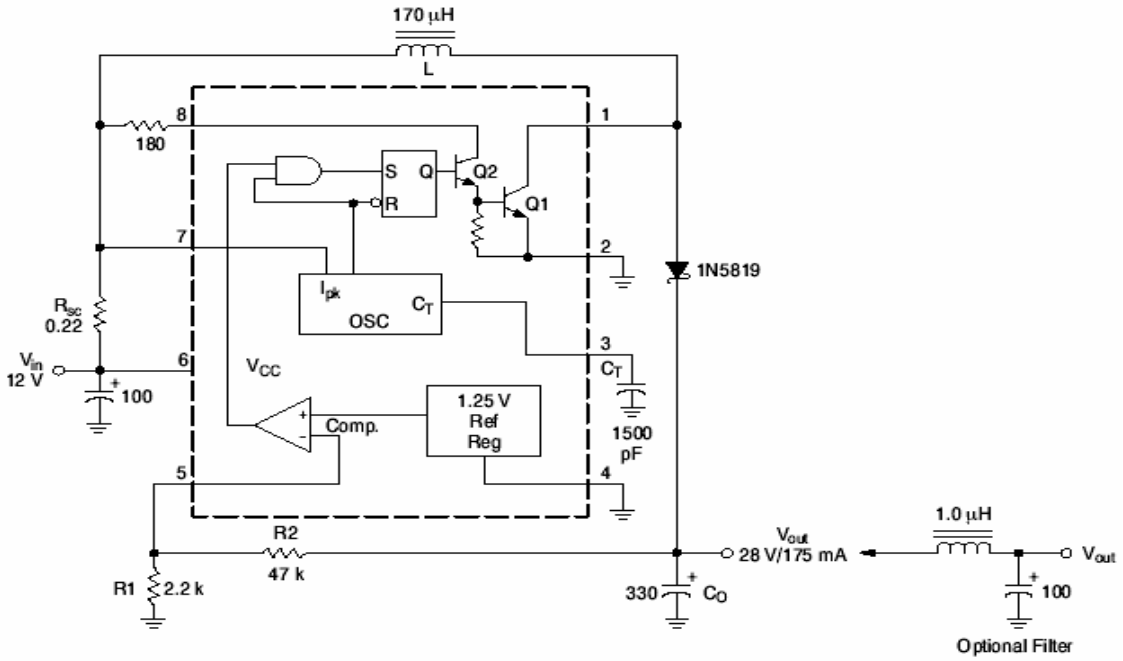


Figure 7. Standby Supply Current versus Supply Voltage

7. Low duty cycle pulse techniques are used during test to maintain junction temperature as close to ambient temperature as possible.



Test	Conditions	Results
Line Regulation	V_{in} = 8.0 V to 16 V, I_O = 175 mA	30 mV = ±0.05%
Load Regulation	V_{in} = 12 V, I_O = 75 mA to 175 mA	10 mV = ±0.017%
Output Ripple	V_{in} = 12 V, I_O = 175 mA	400 mVpp
Efficiency	V_{in} = 12 V, I_O = 175 mA	87.7%
Output Ripple With Optional Filter	V_{in} = 12 V, I_O = 175 mA	40 mVpp

Figure 8. Step−Up Converter

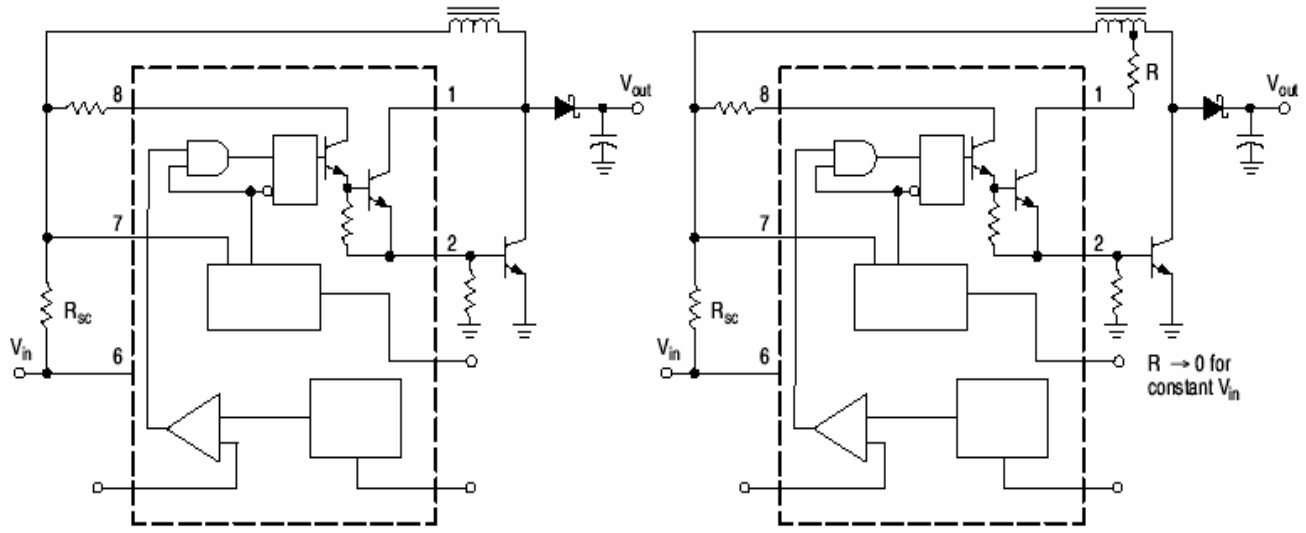
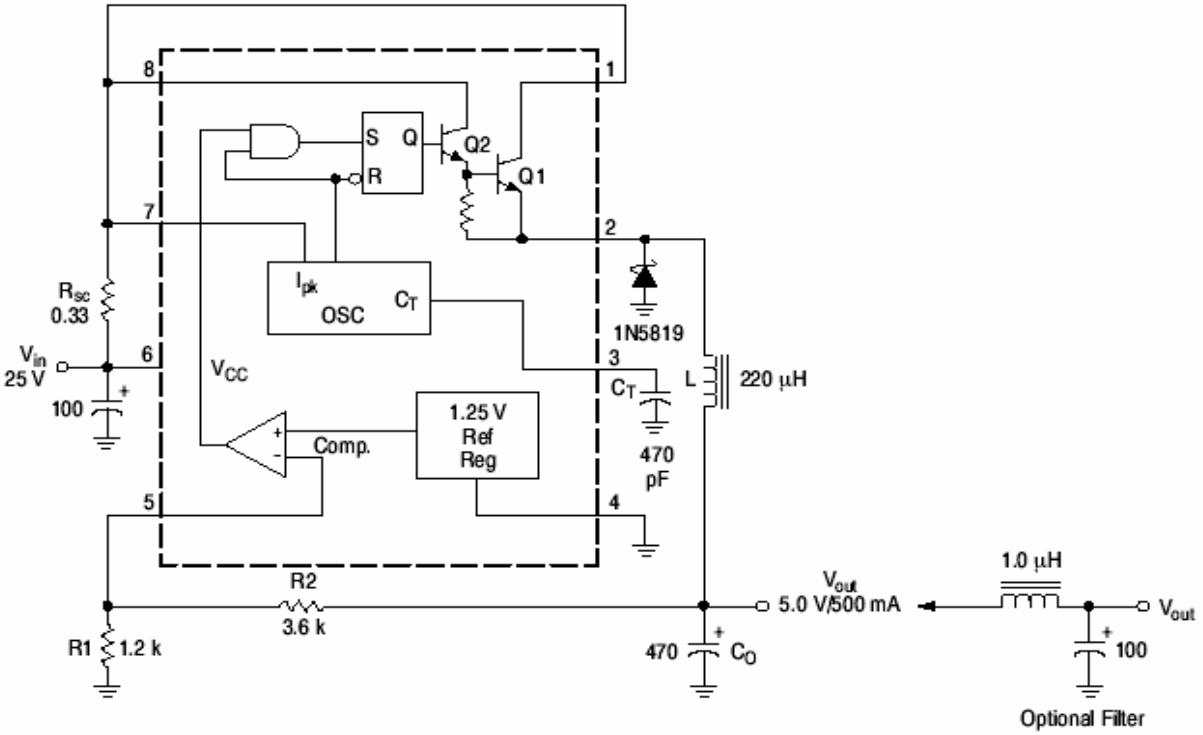


Figure 9. External Current Boost Connections for I_C Peak Greater than 1.5 A

9a. External NPN Switch **9b. External NPN Saturated Switch**

(See Note 8)

8. If the output switch is driven into hard saturation (non−Darlington configuration) at low switch currents (≤ 300 mA) and high driver currents (≥30 mA), it may take up to 2.0 μs to come out of saturation. This condition will shorten the off time at frequencies ≥ 30 kHz, and is magnified at high temperatures. This condition does not occur with a Darlington configuration, since the output switch cannot saturate. If a non−Darlington configuration is used, the following output drive condition is recommended.



Test	Conditions	Results
Line Regulation	V_{in} = 15 V to 25 V, I_O = 500 mA	12 mV = ±0.12%
Load Regulation	V_{in} = 25 V, I_O = 50 mA to 500 mA	3.0 mV = ±0.03%
Output Ripple	V_{in} = 25 V, I_O = 500 mA	120 mVpp
Short Circuit Current	V_{in} = 25 V, R_L = 0.1 Ω	1.1 A
Efficiency	V_{in} = 25 V, I_O = 500 mA	83.7%
Output Ripple With Optional Filter	V_{in} = 25 V, I_O = 500 mA	40 mVpp

Figure 10. Step−Down Converter

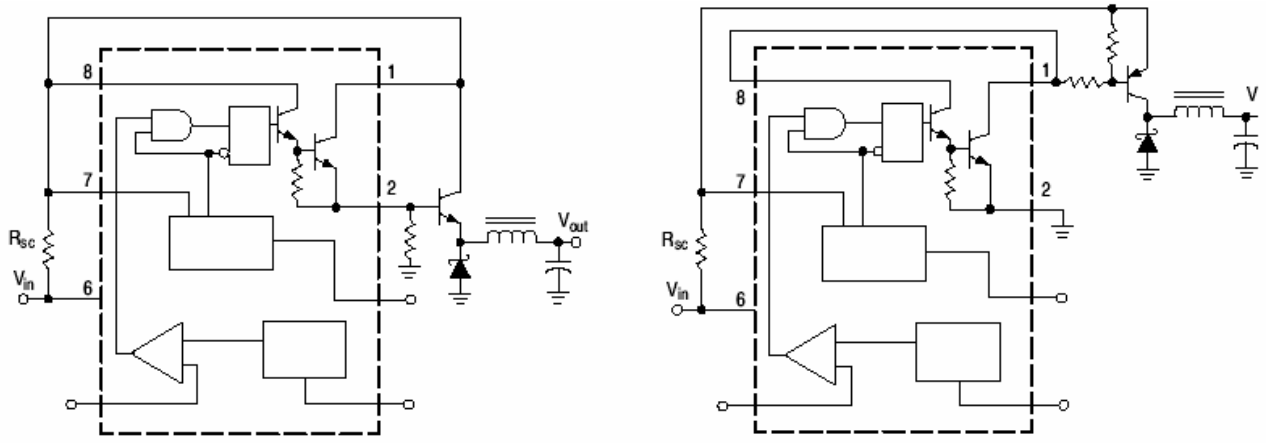
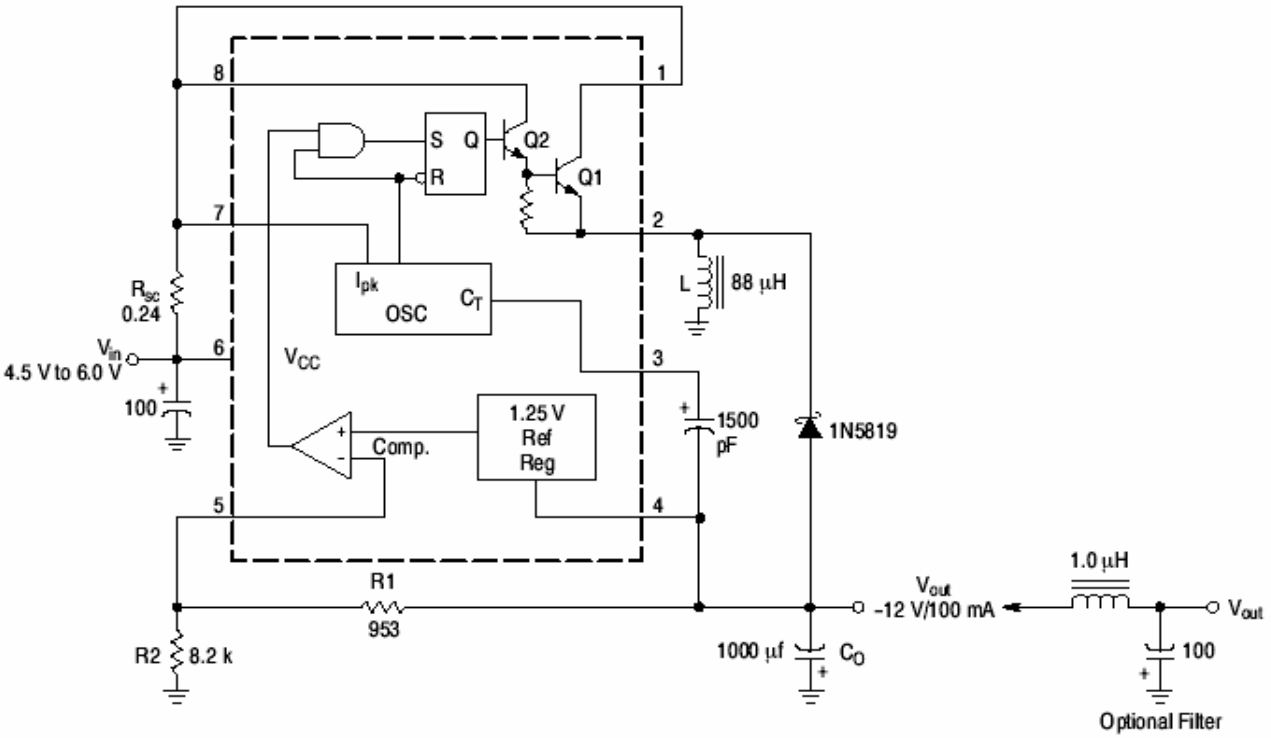


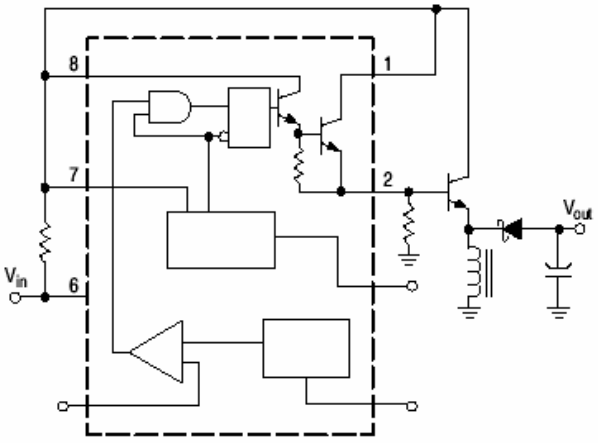
Figure 11. External Current Boost Connections for I_C Peak Greater than 1.5 A

11a. External NPN Switch **11b. External PNP Saturated Switch**



Test	Conditions	Results
Line Regulation	V_{in} = 4.5 V to 6.0 V, I_O = 100 mA	3.0 mV = ±0.012%
Load Regulation	V_{in} = 5.0 V, I_O = 10 mA to 100 mA	0.022 V = ±0.09%
Output Ripple	V_{in} = 5.0 V, I_O = 100 mA	500 mVpp
Short Circuit Current	V_{in} = 5.0 V, R_L = 0.1 Ω	910 mA
Efficiency	V_{in} = 5.0 V, I_O = 100 mA	62.2%
Output Ripple With Optional Filter	V_{in} = 5.0 V, I_O = 100 mA	70 mVpp

Figure 12. Voltage Inverting Converter



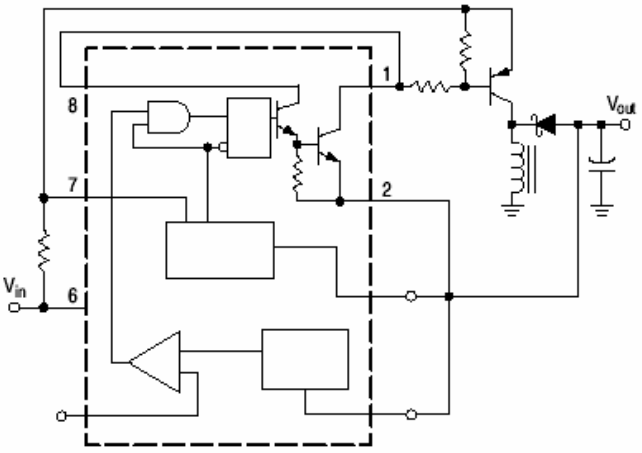


Figure 13. External Current Boost Connections for I_C Peak Greater than 1.5 A

13a. External NPN Switch **13b. External PNP Saturated Switch**

Calculation	Step−Up	Step−Down	Voltage−Inverting
t_{on}/t_{off}	$\frac{V_{out} + V_F - V_{in(min)}}{V_{in(min)} - V_{sat}}$	$\frac{V_{out} + V_F}{V_{in(min)} - V_{sat} - V_{out}}$	$\frac{\lvert V_{out}\rvert + V_F}{V_{in} - V_{sat}}$
$(t_{on} + t_{off})$	$\frac{1}{f}$	$\frac{1}{f}$	$\frac{1}{f}$
t_{off}	$\frac{t_{on} + t_{off}}{\frac{t_{on}}{t_{off}} + 1}$	$\frac{t_{on} + t_{off}}{\frac{t_{on}}{t_{off}} + 1}$	$\frac{t_{on} + t_{off}}{\frac{t_{on}}{t_{off}} + 1}$
t_{on}	$(t_{on} + t_{off}) - t_{off}$	$(t_{on} + t_{off}) - t_{off}$	$(t_{on} + t_{off}) - t_{off}$
C_T	$4.0 \times 10^{-5} t_{on}$	$4.0 \times 10^{-5} t_{on}$	$4.0 \times 10^{-5} t_{on}$
$I_{pk(switch)}$	$2I_{out(max)}\left(\frac{t_{on}}{t_{off}} + 1\right)$	$2I_{out(max)}$	$2I_{out(max)}\left(\frac{t_{on}}{t_{off}} + 1\right)$
R_{sc}	$0.3/I_{pk(switch)}$	$0.3/I_{pk(switch)}$	$0.3/I_{pk(switch)}$
$L_{(min)}$	$\left(\frac{(V_{in(min)} - V_{sat})}{I_{pk(switch)}}\right) t_{on(max)}$	$\left(\frac{(V_{in(min)} - V_{sat} - V_{out})}{I_{pk(switch)}}\right) t_{on(max)}$	$\left(\frac{(V_{in(min)} - V_{sat})}{I_{pk(switch)}}\right) t_{on(max)}$
C_O	$9\frac{I_{out}t_{on}}{V_{ripple(pp)}}$	$\frac{I_{pk(switch)}(t_{on} + t_{off})}{8V_{ripple(pp)}}$	$9\frac{I_{out}t_{on}}{V_{ripple(pp)}}$

V_{sat} = Saturation voltage of the output switch.

V_F = Forward voltage drop of the output rectifier.

The following power supply characteristics must be chosen:

V_{in} − Nominal input voltage.

V_{out} − Desired output voltage, | V_{out} |= 1.25（1+ R2/R1）

I_{out} − Desired output current.

f_{min} − Minimum desired output switching frequency at the selected values of Vin and I_O.

$V_{ripple(pp)}$ − Desired peak−to−peak output ripple voltage. In practice, the calculated capacitor value will need to be increased due to its equivalent series resistance and board layout. The ripple voltage should be kept to a low value since it will directly affect the line and load regulation.

Figure 15. Design Formula Table

ORDERING INFORMATION

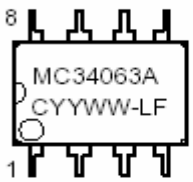
Device	Package	Shipping†
MC33063AD	SOIC−8	98 Units / Rail
MC33063ADG	SOIC−8 (Pb−Free)	
MC33063ADR2	SOIC−8	2500 Units / Tape & Reel
MC33063ADR2G	SOIC−8 (Pb−Free)	
MC33063AP1	DIP−8	50 Units / Rail
MC33063AP1G	DIP−8 (Pb−Free)	
MC33063AVD	SOIC−8	98 Units / Rail
MC33063AVDG	SOIC−8 (Pb−Free)	
MC33063AVDR2	SOIC−8	2500 Units / Tape & Reel
NCV33063AVDR2*		
NCV33063AVDR2G	SOIC−8 (Pb−Free)	
MC33063AVP	DIP−8	50 Units / Rail
MC34063AD	SOIC−8	98 Units / Rail
MC34063ADG	SOIC−8 (Pb−Free)	
MC34063ADR2	SOIC−8	2500 Units / Tape & Reel
MC34063ADR2G	SOIC−8 (Pb−Free)	
MC34063AP1	DIP−8	50 Units / Rail
MC34063AP1G	DIP−8 (Pb−Free)	

*NCV33063A: T_{low} = −40°C, T_{high} = +125°C. Guaranteed by design. NCV prefix is for automotive and other applications requiring site and change control.

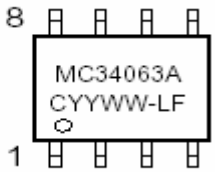
†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

MARKING DIAGRAMS

PDIP−8



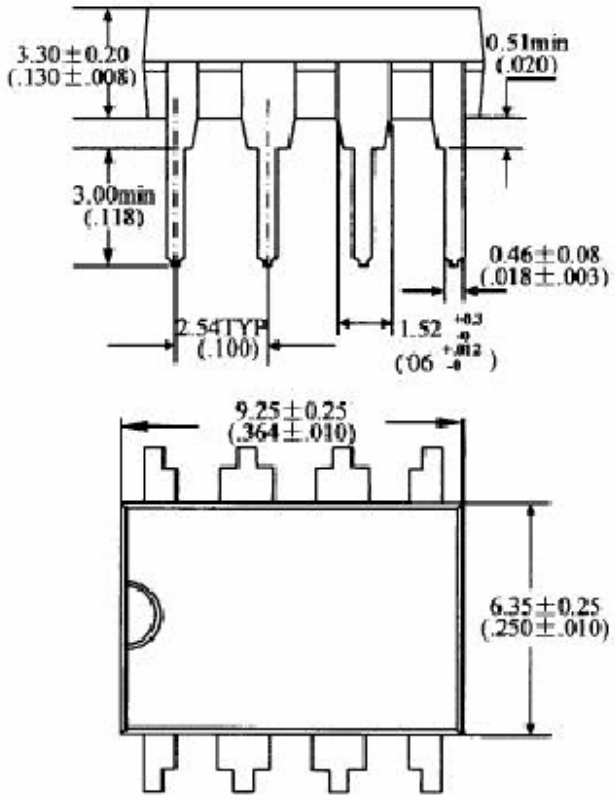
SOIC−8



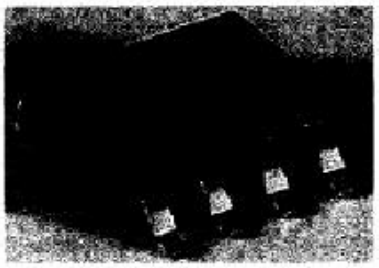
XXXXXX = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week
LF = Pb−Free Package

DIP8L

引线间距 Lead Pitch	2.54mm(100mil)
跨度 Row Spacing	7.62mm(300mil)
载体尺寸 Pad Size	100mil×100mil
	120mil×150mil
载体打凹深度 Depressed Die Pad	0.254±0.05 (0.01±0.002)
单位 Unit	mm(inches)



SOP8L



引线间距 Lead Pitch	1.27mm(50mil)
切筋凸缘 Trim Flange	0~0.1mm(0~3.9mil)
载体尺寸 Pad Size	80mil×80mil
	90mil×100mil
	95mil×150mil
载体打凹深度 Depressed Die Pad	0.229±0.051 (0.009±0.002)
单位 Unit	mm(inches)