# LLC Resonant Converter for 48V to 0.9V VRM

Yanjun Zhang, Dehong Xu, Min Chen
Institute of Power Electronics, Zhejiang University
Hangzhou 310027, China
Email: yjzhang@zju.edu.cn

Yu Han, Zhong Du
Emerson Network Power Co., Ltd.
Shenzhen 518129, China
Email: hanyua@avansys.com

***Abstract*—48V to 0.9V VRM using LLC resonant converter is presented. ZVS is realized for switches and the converter can operate at higher frequency. How to reduce primary current amplitude by reducing power factor angle is explored. The effect of secondary leakage inductance is studied and FEA method is used to find the optimal transformer winding configuration. The resonant inductor can be integrated with transformer primary leakage inductance, which reduces the total magnetic component counts. A prototype of 48V to 0.9V/50A VRM is built to verify the result.**

## I. INTRODUCTION

The computer industry has been quickly expanding for the last decade. The speed and integration density of microprocessors have increased rapidly. Now the processor works with clock frequencies in the 2~3 GHz range. The next generation of processors will work with even higher clock frequencies. As a result, modern microprocessors are being designed to work with lower levels of voltage in order to meet the increasingly high demands for speed and integration density. Now the Intel Pentium • •microprocessors run at the voltage of 1.3V-1.7V, in the future the voltage will be below 1V. The requirements for the microprocessors' power supplies such as Voltage Regulator Modules (VRM) [1] are more and more critical. The output voltage of the VRM we designed here in the paper is 0.9V.

Today's VRMs are mainly pulse width modulation (PWM) converters, such as the multi-phase interleaving synchronous buck [2], the push-pull buck [3], and the push-pull forward topology [4]. Utilizing external resonant method during the switch's transition period, they realize ZVS. To increase the effective switching frequency and dynamics multi-phase converter structure has been implemented. However the complexity of these converters is increased.

For further increasing the switching frequency and keeping high efficiency of the converter, resonant converters attract people's attention once more. LLC resonant converter has been successfully applied in the front end DC/DC conversion in Distributed Power System ([5]-[6]). Here LLC resonant converter is introduced to VRM, as shown in Fig1. In LLC resonant converter, ZVS is realized due to series resonance principle for switches in the half bridge. In traditional two-order LC resonant converter, output voltage regulation ability is lost at light load condition. Three-order LLC resonant converter owns both the advantages of series and parallel resonant circuit, and can regulate the output voltage

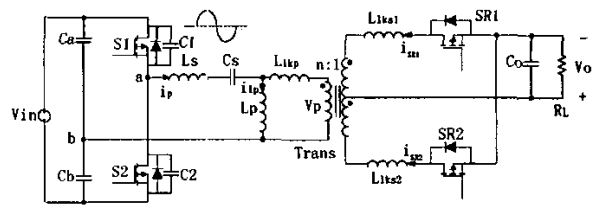



Fig. 1. LLC Resonant Converter for 48Vto 0.9V VRM

in a larger load range. Nevertheless resonant converters needs variable-frequency control, which cause difficulty to the converter design such as gating of synchronous rectifier and power factor for the resonant loop, and the switching frequency range of the converter.

In this paper, DC characteristics of the converter is analyzed and the operation stages are presented. Method to reduce the power factor angle is explored due to its important influence on the converter performance. Secondary side leakage inductance impairs the converter efficiency and FEA method is used to find the optimal transformer winding configuration with least secondary side leakage inductance.

## II. LLC RESONANT CONVERTER ANALYSIS

### A. Operation Stages

The diagram of LLC Resonant Converter is shown in Fig.1. $L_{lkp}$, $L_{lks1}$, $L_{lks2}$ are the leakage inductance at primary and secondary side respectively. Since leakage inductance exists in the secondary side, there is overlapping time of commutation between switch SR1 and switch SR2. As a result, secondary current $i_{SR1}$ and $i_{SR2}$ conducts longer than half period. When the converter is working at frequency higher than series resonant frequency $f_o$, the operation can be divided into five stages. The operation stages and the steady state waveform are shown in Fig2 and Fig3 respectively.

Stage1 (t0-t1):

Before this stage, current $i_p$ through the resonant inductor flows through switch S2, current $i_{SR1}$ flows through switch SR1. At time t0, current $i_{SR2}$ begins to rise, since the gate signal of SR2 is not applied, current $i_{SR2}$ flows through the parallel diode of switch SR2. This stage ends when gate signal of switch S2 is removed.

Stage2 (t1-t2):

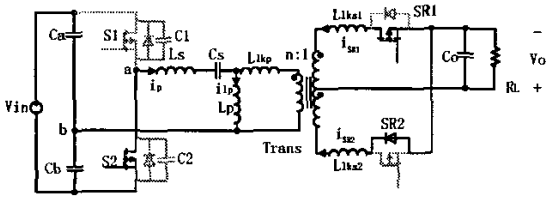
At time t1, switch S2 and SR1 are turned off, current $i_{SR1}$ begins to flow through the parallel diode of switch SR1. Since the resonant circuit operates at induction mode, current $i_p$ is negative at this moment, current $i_p$ begins to charge the

0-7803-8399-0/04/$20.00 ©2004 IEEE.

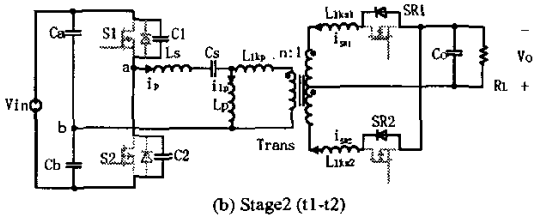
parallel capacitor of switch S2 and discharge the parallel capacitor of switch S1. This stage ends when the voltage on the parallel capacitor of switch S2 is charged to $V_{in}$, and the voltage on the parallel capacitor of switch S1 is discharged to zero. Then current $i_p$ begins to flow through the parallel diode of switch S1, creating ZVS condition for switch S1. To realize ZVS, the following condition should be satisfied,

$$V_{c2} = \frac{1}{C_{oss}} \cdot \int_{\frac{t_d}{2}}^{\frac{t_d}{2}} -\frac{1}{2} \cdot i_p(t) \cdot dt \geq V_{in} \quad (1)$$

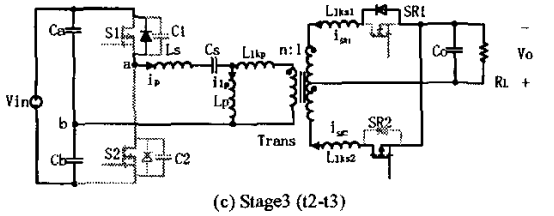
where $V_{c2}$ is the voltage on parallel capacitor C2, $C_{oss}$ is the output capacitance of switch S2, $t_d$ is the dead time in the gate signals of the main switches in the half bridge, current through the resonant inductor $i_p(t) = I_p \sin(\omega t - \phi)$, $\phi$ is the power factor angle, $V_{in}$ is the input voltage.



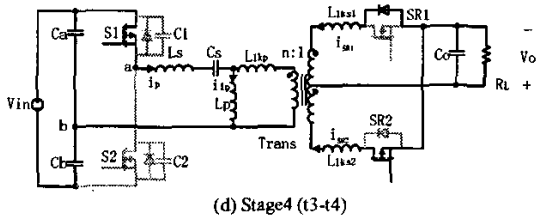

(a) Stage1 (t0-t1)



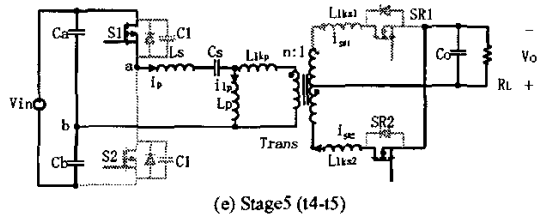

(b) Stage2 (t1-t2)




(c) Stage3 (t2-t3)




(d) Stage4 (t3-t4)




(e) Stage5 (t4-t5)

Fig. 2. Operation Stages

Stage3 (t2-t3):

At time t2, the gate signal of switch SR2 is applied, current $i_{SR2}$ begins to flow through switch SR2. Current $i_p$ flows through the parallel diode of switch S1, the gate signal of switch S1 should be applied during this stage. This stage ends when current $i_p$ turns positive.

Stage4 (t3-t4):

At time t3 current $i_p$ turns positive and begins to flow through switch S1. This stage ends when secondary current $i_{SR1}$ is decreased to zero.

Stage5 (t4-t5):

At time t4, secondary current $i_{SR1}$ is decreased to zero, and secondary current only flows through switch SR2. This stage ends when secondary current $i_{SR1}$ begins to rise at time t5.

The other half switching cycle can be analyzed correspondingly.

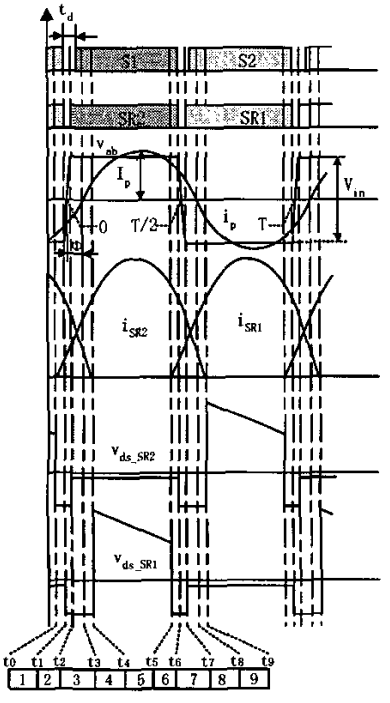



Fig. 3. Steady State Waveforms

## B. DC Characteristics

Fundamental Component Simplification (FES) method is used to simply the analysis. Fundamental component equivalent circuit is shown in Fig4. Input voltage $E_{in}$ is square

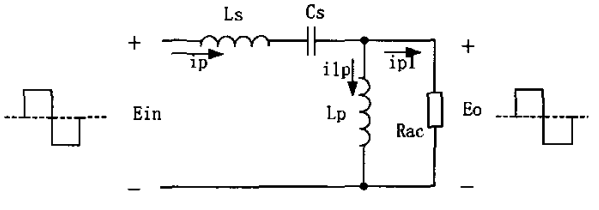



Fig. 4. AC Equivalent Circuit of LLC Resonant Converter

wave which is generated by the half-bridge inverter. Output voltage $E_o$ is the voltage of the transformer primary side. $L_s$ and $C_s$ are the series resonant inductor and capacitor respectively, $L_p$ is the parallel inductor, $R_{ac}$ is the load resistance reflected to the transformer primary side, $R_{ac} = n^2 \cdot \frac{8}{\pi^2} \cdot R_L$, n is the transformer turn ratio, $R_L$ is the load resistance.

AC voltage gain $G_{ac}$ can be analyzed as

$$G_{ac} = \frac{\dot{E}_o}{\dot{E}_{in}} = \frac{R_{ac} // j\cdot\omega\cdot L_p}{j\cdot\omega\cdot L_s + \frac{1}{j\cdot\omega\cdot C_s} + R_{ac} // j\cdot\omega\cdot L_p} \quad (2)$$

We can derive

$$|G_{ac}| = \frac{E_o}{E_{in}} = \frac{1}{\sqrt{\left[1+\frac{1}{k}\cdot\left(1-\frac{f_o^2}{f^2}\right)\right]^2 + \left[\left(\frac{f}{f_o}-\frac{f_o}{f}\right)\cdot\frac{\pi^2}{8n^2}\cdot Q\right]^2}} \quad (3)$$

where $k = \frac{L_p}{L_s}$, $f_o$ is the series resonant frequency, $f_o = \frac{1}{2\pi\sqrt{L_s\cdot C_s}}$, and quality factor $Q = \sqrt{\frac{L_s}{C_s}}\cdot\frac{1}{R_L}$.

Fundamental element RMS value of half bridge output voltage

$$E_{in} = \frac{\sqrt{2}}{\pi}\cdot V_{in} \quad (4)$$

Fundamental element RMS value of transformer primary side voltage

$$E_o = n\cdot\frac{2\sqrt{2}}{\pi}\cdot V_o \quad (5)$$

DC voltage gain of the converter

$$G_{dc} = \frac{V_o}{V_{in}} \quad (6)$$

Substitute (4), (5) into (6), we can derive

$$G_{dc} = \frac{1}{2n}\cdot\frac{E_o}{E_{in}} = \frac{1}{2n}\cdot\frac{1}{\sqrt{\left[1+\frac{1}{k}\cdot\left(1-\frac{f_o^2}{f^2}\right)\right]^2 + \left[\left(\frac{f}{f_o}-\frac{f_o}{f}\right)\cdot\frac{\pi^2}{8n^2}\cdot Q\right]^2}}$$

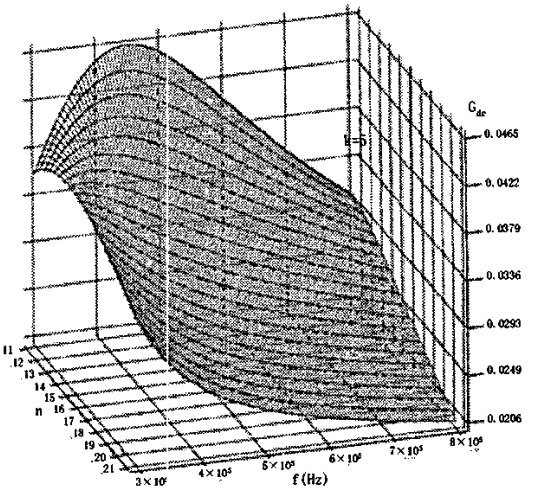
The relationship among DC voltage gain $G_{dc}$ and switching frequency f and transformer turn ratio n is shown in Fig5, where quality factor Q is a parameter and $k = 5$, $f_o = 500KHz$.

### C. Converter Design

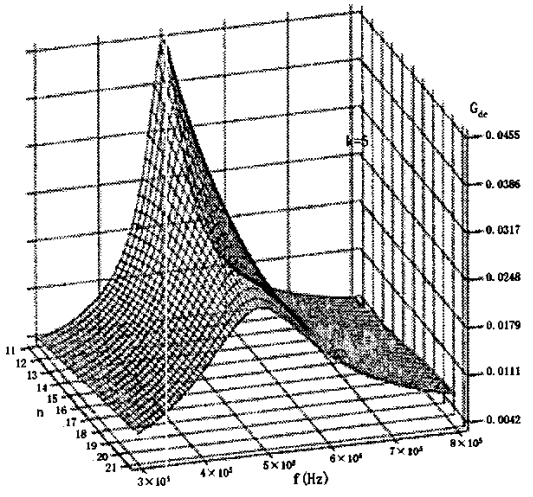
The requirement of the LLC resonant converter is shown in table 1.

TABLE I
REQUIREMENT OF THE CONVERTER

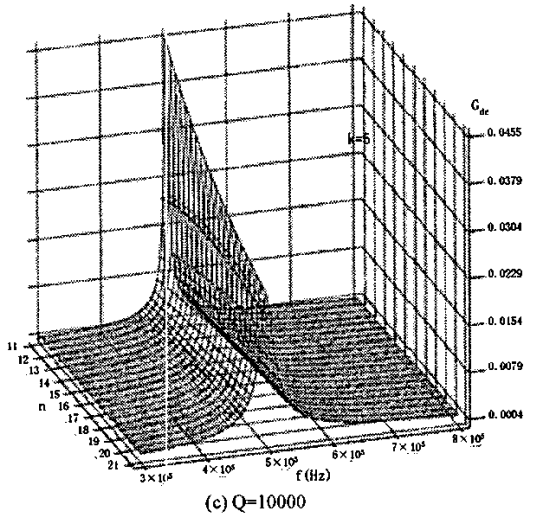
| | Input Voltage $V_{in}$ (V) | Output Voltage $V_o$ (V) | Output Current $I_o$ (A) | Switching Frequency (KHz) |
|---|---|---|---|---|
| Minimum | 36 | 0.9 | 10 | 400 |
| Maximum | 72 | 0.9 | 50 | 800 |



(a) Q=100



(b) Q=1000



(c) Q=10000

Fig. 5. DC Characteristic (k=5)

The input voltage range of the LLC resonant converter is 36V to 72V, the output voltage is 0.9V. Therefore, the DC voltage gain $G_{dc}$ should between 0.0125 and 0.025.

Too large transformer turn ratio increases the transformer design and manufacture difficulty. However, if transformer turn ratio is too small, the primary side current and conduction loss increases and efficiency is impaired.

From Fig5, when Q=100, the DC voltage gain $G_{dc}$ is higher than 0.0125 even at the maximum switching frequency, and the situation is the same when Q is below 100. Thus, quality factor Q below 100 is not considered. At the condition of Q>100 and n>20, the maximum DC voltage gain can't reach 0.025. Therefore, transformer turn ratio n>20 is discarded too.

The larger Q is, the more sensitive is the DC voltage gain to the change of switching frequency for the DC voltage gain between the range of 0.0125 and 0.025. Small change in switching frequency will induce dramatic change in DC voltage gain, which may cause the control instability of the converter.

k is also an important parameter in LLC resonant converter. Larger k means smaller current through parallel inductor $L_p$ when voltage cross $L_p$ is fixed at rated output voltage condition. Thus loss on inductor $L_p$ is reduced. However, if k is too large, the LLC resonant converter degenerates to two-order LC resonant circuit and loses output voltage regulation ability at light load condition.

The final design results are: n=13, Q=2500, k=5. Then the circuit parameters can be calculated as: $L_s$=14uH, $C_s$=7nF, $L_p$=70uH. When the circuit parameters are selected, the DC voltage gain $G_{dc}$ as function of switching frequency f can then be described as Fig6, where Q=500 and 2500 corresponds to the light load and full load condition respectively. From Fig6 we can see that the converter can satisfy the DC voltage gain requirement.

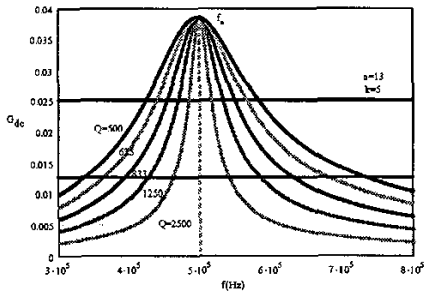



Fig. 6. DC Characteristic (n=13, k=5)

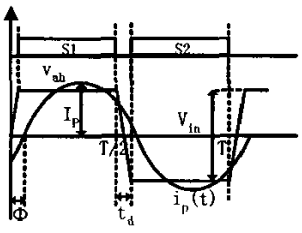



Fig. 7. Primary Voltage and Primary Current

## III. POWER FACTOR ANGLE OF PRIMARY SIDE

The half bridge output voltage $v_{ab}$ and current $i_p$ are shown in Fig7. It is assumed that resonant current $i_p$ is sinusoidal. $t_d$ is the dead time in the gate signals of the main switches in the half bridge. $V_{in}$ and $I_p$ are the input voltage and the peak value of primary current respectively. Current $i_p$ is lagging the voltage $v_{ab}$ with phase angle • : The turn-off current and turn-off loss can be reduced if • is smaller. In addition, with fixed output power the amplitude of $i_p$ is reduced with the decrease of • because reactive power is reduced. Thus the primary side conduction loss is reduced too. However, if • is close to zero, ZVS condition of the main switch is lost.

To realize ZVS for the switches of the half-bridge inverter, one capacitor parallel to the one switch should be completely charged while the other capacitor paralleled to other switch need to be discharged by resonant current $i_p$ during dead time $t_d$. The following equation can be derived from (1),

$$\sin\phi \geq \frac{2C_{oss}\cdot V_{in}}{I_p\cdot t_d} \tag{7}$$

Considering that only fundamental element of the half bridge inverter output voltage transfers active power, the input power of the converter $P_{in}$ can be written as

$$P_{in} = \frac{1}{\sqrt{2}}\cdot\frac{4}{\pi}\cdot\frac{V_{in}}{2}\cdot\frac{1}{\sqrt{2}}\cdot I_p\cdot\cos\phi \tag{8}$$

Substitute (8) to (7), the following results can then be derived,

$$\phi \geq tg^{-1}\frac{2C_{oss}\cdot V_{in}^{\ 2}}{\pi\cdot P_{in}\cdot t_d} \tag{9}$$

From (9), MOSFET with smaller $C_{oss}$ is favorable for reducing primary power factor angle while at the same time keeping ZVS condition of the main switch.

## IV. SECONDARY SIDE LEAKAGE INDUCTANCE

In LLC resonant converter for VRM, the SR MOSFET employs self-driven method ([7]-[9]), as shown in Fig8. The secondary side waveform is shown in Fig9. The secondary current waveform is approximate half sine wave. Since leakage inductance exists in the secondary side, there is overlapping time of commutation between switch SR1 and switch SR2. As a result, secondary current $i_{SR1}$ and $i_{SR2}$ conducts longer than half period. An overlapping period is produced between current $i_{SR1}$ and current $i_{SR2}$, as shown in Fig9. Assuming current is transferred from switch SR1 to switch SR2, at time t0 switch SR1 is turned off, secondary current $i_{SR1}$ flows through the parallel diode of switch SR1, therefore the voltage drop on switch SR1 is around 0.7V from time t0 to t1. Actually the synchronous rectification doesn't work and loss is increased significantly during this period. Fig10 shows the simulation results of current $i_{SR1}$, $i_{SR2}$ and the voltage drop on switch SR1. Fig11 gives the experimental waveforms of current $i_{SR1}$, $i_{SR2}$ and the voltage drop on switch SR1, and the waveforms are compared with different secondary side leakage inductance. When the leakage inductance is larger, the secondary side current overlapping

period will be longer, and the duration when the voltage on the SR switches reaches 0.7V takes a larger portion in a period. As a result, converter efficiency is decreased. Therefore, reducing the secondary side leakage inductance is required.

Leakage inductance can be reduced by properly designing the transformer winding configuration. Fig12 shows three different kinds of winding configuration (planar ER28, copper thickness 0.2mm). The transformer turn ratio is 13:1. Five primary layers (1turn the first layer, 3 turns in series for other layers) are series connected to form primary winding. Three secondary layers (1 turn for each layer) are parallel connected to form secondary winding 1, and the left three secondary layers parallel connected to form secondary winding 2. FEA method is used to simulate the transformer secondary leakage inductance, and results are given in Fig13. We can see that structure 1 seems to be the optimal choice at the consideration of reducing transformer secondary side leakage inductance.

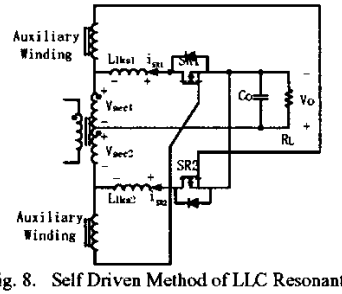



Fig. 8. Self Driven Method of LLC Resonant Converter

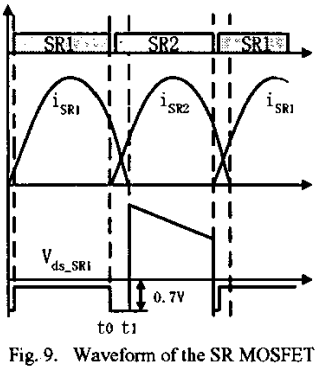



Fig. 9. Waveform of the SR MOSFET

## V. EXPERIMENTAL RESULTS

A prototype is built to study the performance of LLC resonant converter in VRM applications. Since there are differences between the experiment and the theoretical analysis, such as losses and the nonideal synchronous rectification, the final circuit parameters in experiment deviate a little from the designed values. The circuit parameters in experiment are: $L_s$: 4.2uH, $C_s$: 18.8nF, $L_p$: 12uH, transformer turn ratio: 13, main switch: Vishay Si4488• 2, SR MOSFET: Infineon IPP05N03LA• 5, output capacitor: ceramic SMD 47uF• 10. A picture of the prototype is shown in Fig14.

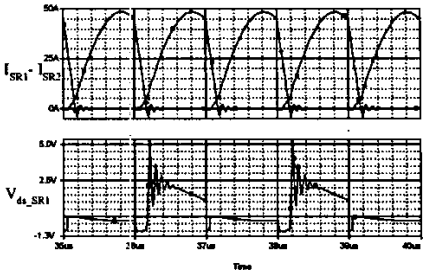
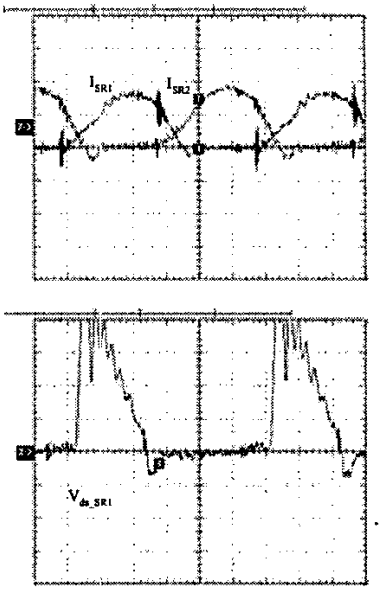
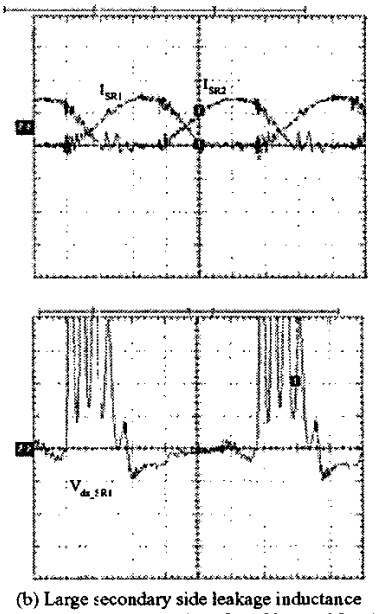



Fig. 10. Simulation waveform of $I_{SR1}$, $I_{SR2}$, $V_{ds\_SR1}$




(a) Small secondary side leakage inductance




(b) Large secondary side leakage inductance

Fig. 11. Experimental Waveform of $I_{SR1}$, $I_{SR2}$, $V_{ds\_SR1}$(25A/div, 25A/div, 1V/div, 200ns/div) (a) with small secondary side leakage inductance (b) with large secondary side leakage inductance

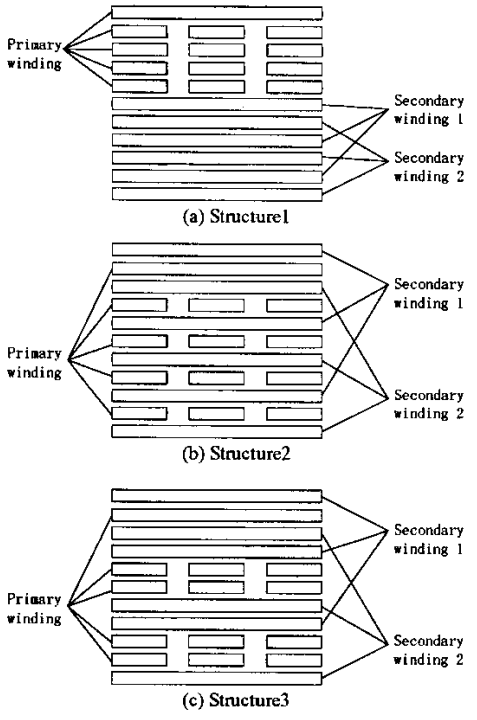



Fig. 12. Three Different Kinds of Winding Configuration

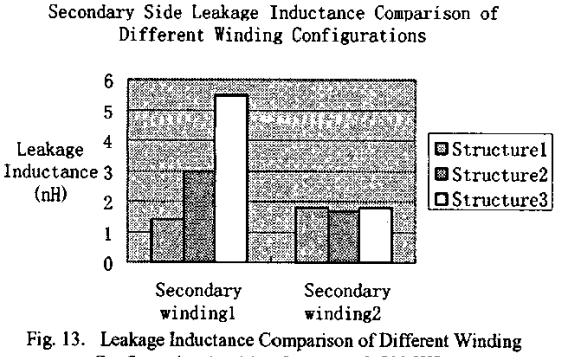



Fig. 13. Leakage Inductance Comparison of Different Winding Configuration (exciting frequency f=500 KHz)

Fig15 shows the $V_{gs}$ and $V_{ds}$ of switch S1. We can see that before $V_{ds}$ is reduced to zero, $V_{gs}$ is kept negative. After $V_{ds}$ reaches zero, $V_{gs}$ is applied. Therefore, switch S1 is turned on in ZVS condition. Fig16 shows $V_{gs}$ and $V_{ds}$ of switch S2. Switch S2 is also turned on in ZVS condition. Fig17 gives the efficiency curve at different load condition. Efficiency at the output current of 10A is rather low, which indicates that synchronous rectification is not working well at this condition. It also demonstrates that in resonant converters it's difficult to optimize the circuit parameters for full load range. When output current increases from 20A to 50A, efficiency decreased rapidly, this suggests that conduction loss takes a major portion of the total losses. Fig18 gives the switching frequency curve at different input voltage. Switching frequency increases as input voltage increases and output current decreases.

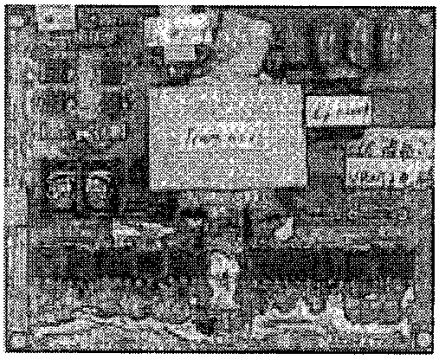
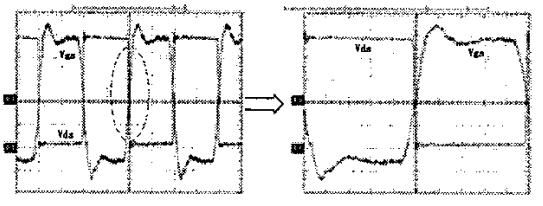
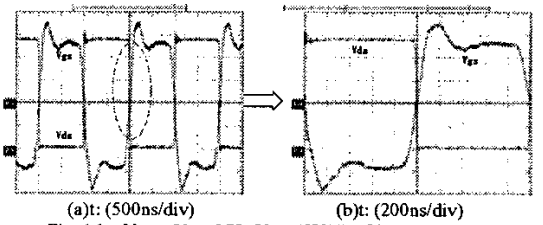


Fig. 14. Prototype of the LLC Resonant Converter for 48V to 0.9V VRM




(a)t: (500ns/div) (b)t: (200ns/div)

Fig. 15. $V_{gs}$ vs $V_{ds}$ of S1, Vgs: (5V/div) Vds: (10V/div)




(a)t: (500ns/div) (b)t: (200ns/div)

Fig. 16. $V_{gs}$ vs $V_{ds}$ of S2, Vgs: (5V/div) Vds: (10V/div)

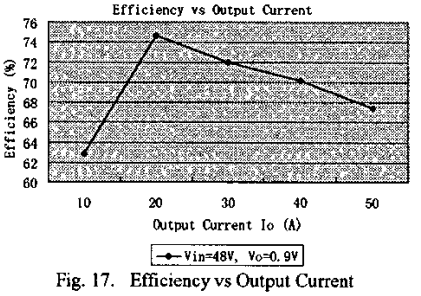



Fig. 17. Efficiency vs Output Current

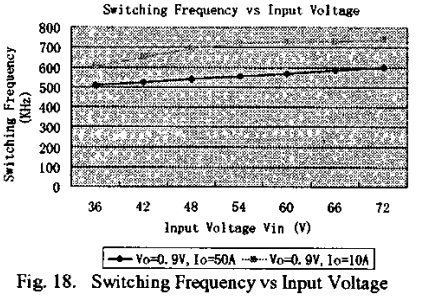



Fig. 18. Switching Frequency vs Input Voltage

## VI. CONCLUSION

48V to 0.9V VRM using LLC resonant converter is presented. The main switches work in ZVS condition. So the converter can work at higher frequency, which is helpful for the fast transient response and magnetic size reduction. How to reduce the primary current amplitude by reducing the power factor angle is investigated. The effect of secondary leakage inductance of transformer is studied, and the winding configuration design to minimize the secondary leakage inductance is presented.

## ACKNOWLEDGEMENT

This work was supported by Emerson Network Power Co., Ltd. It is also supported by National Natural Science Foundation of China with Project Number 50237030.

## REFERENCES

[1] Peng Xu, Mao Ye, Fred C. Lee, "Single Magnetic Push-Pull Forward Converter Featuring Built-in Input Filter and Coupled-Inductor Current Doubler for 48V VRM", IEEE Applied Power Electronics Conference and Exposition (APEC'02), 2002

[2] Xunwei Zhou, Xu Peng, Lee, F.C, "A high power density, high efficiency and fast transient voltage regulator module with a novel current sensing and current sharing technique", IEEE Applied Power Electronics Conference and Exposition (APEC'99), 1999

[3] Jia Wei, Peng Xu, Lee, F.C, "A high efficiency topology for 12 V VRM-push-pull buck and its integrated magnetics implementations", IEEE Applied Power Electronics Conference and Exposition (APEC'02), 2002

[4] Mao Ye, Ming Xu, Lee, F.C, "1 MHz Multi-Resonant Push-Pull 48V VRM", IEEE Applied Power Electronics Conference and Exposition (APEC'03), 2003

[5] BoYang, Fred C. Lee, Zhang, A.J., Guisong Huang, "LLC resonant converter for front end DC/DC conversion" IEEE Applied Power Electronics Conference and Exposition (APEC'02), 2002.

[6] Bo Yang, Fred C. Lee, Matthew Concannon, "Over current protection methods for LLC resonant converter", IEEE Applied Power Electronics Conference and Exposition (APEC'03), 2003.

[7] Joe C. P. Liu, Xuefei Xie, Franki N. K. Poon, Bryan M. H. Pong, "Practical Solutions to the Design of Current-driven Synchronous Rectifier with Energy Recovery from Current Sensing" IEEE Applied Power Electronics Conference and Exposition (APEC'03), 2003.

[8] Wojciech A. Tabisz, Fred C. Lee, Dan Y. Chen, "A MOSFET resonant synchronous rectifier for high-frequency DC/DC converters" IEEE Power Electronics Specialists Conference (PESC'90), 1990.

[9] J. A. Cobos, P.Alou, O.Garcia, J.Uceda, M.Rascon, "New driving scheme for self driven synchronous rectifiers" IEEE Applied Power Electronics Conference and Exposition (APEC '99), 1999.