The 33rd Annual Conference of the IEEE Industrial Electronics Society (IECON)
Nov. 5-8, 2007, Taipei, Taiwan

Active Clamp Sepic Converter with Power Factor Correction

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***Abstract*- A soft switching sepic converter with active clamp scheme is presented in this paper to achieve zero voltage switching (ZVS) on the power switches. The active clamp topology is used in the circuit to limit the voltage stresses of power semiconductors. When main switch is turned off, the positive resonant inductor current flows through the anti-parallel diode of auxiliary switch so that the auxiliary switch can be turned on at ZVS. When auxiliary switch is turned off, the negative resonant inductor current will discharge the output capacitor of main switch so that the ZVS turn-on of main switch can be achieved. Finally, experiments based on a laboratory prototype rated at 300W are presented to verify the effectiveness of the proposed converter.**

I. INTRODUCTION

Switching mode power supplies are widely used in modern industrial applications. The hard switching techniques of dc converters result in low efficiency and high voltage and current stresses of power semiconductors. Soft switching topologies with variable switching frequency have been proposed in [1-2] to achieve zero voltage switching (ZVS) turn-on or zero current switching (ZCS) turn-off. However, these techniques have large voltage and current stresses on the circuit components. Active clamp converter techniques [3-5] have been proposed to achieve ZVS operation during the commutation stage of a pair of complementary active switches. High quality of power supply converters with power factor correction (PFC) is increasingly required in industry. PFC techniques [6-11] based on diode bridge rectifier and pulse-width modulation (PWM) converters are designed to increase power factor at the utility side. The boost type topology [6] is generally used to achieve power factor correction. In boost type PFC converter, the high dc-link voltage may cause over voltage stresses on the switching devices. The generalized feedforward current control scheme was presented in [7] for single phase PFC. In [8] the nonlinear current control scheme is provided to sepic converter for power factor correction (PFC).

This paper presents a new soft switching sepic converter with active clamp topology to achieve ZVS turn-on for all power switches. The active clamp circuit can limit the voltage stresses of the power switches. The resonance based on the resonant inductor and resonant capacitor takes place during the commutation interval between two switches. Before the switch is turned on, the output capacitor across the power switch is discharged to zero voltage. Therefore the switch can be turned on at ZVS. The circuit configuration, principles of operation and design consideration of the proposed converter are presented in detail. The application of the proposed converter in power factor correction is implemented in this paper to draw a clean and sinusoidal line current from the ac source. Finally, experiments conducted on a laboratory prototype rated at 300W are presented to verify the effectiveness of the proposed converter in power factor correction.

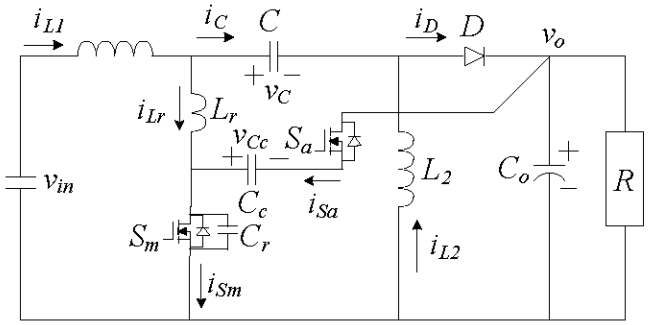


Fig. 1 Circuit configuration of the proposed ZVS sepic converter.

II. CIRCUIT CONFIGURATION AND SYSTEM ANALYSIS

Fig. 1 gives the circuit configuration of the proposed soft switching sepic converter. The basic sepic converter includes the components of L_1, L_2, S_m, D, C and C_o. The resonant inductor L_r, clamp capacitor C_c and auxiliary switch S_a are connected between the input inductor and the output capacitor. When main switch S_m is turned off. The positive inductor current i_{Lr} will flow through clamp capacitor C_c and the anti-parallel diode of the auxiliary switch S_a. At this instant the auxiliary switch can be turned on at ZVS. The circuit components L_r and C_c are at resonance. The inductor current i_{Lr} will decrease from positive value to negative value. When the auxiliary switch S_a is turned off, the negative inductor current i_{Lr} will discharge capacitor C_r. The capacitor voltage v_{Cr} decreases from positive value to zero so that the anti-parallel diode of main switch S_m is turned on. At this instant the main switch S_m can be turned on at ZVS. Based on the active clamp circuit, the voltage stresses of the power switches equal $v_{Cc}+v_o$.

Before the system analysis of the proposed converter, some

assumptions are made as follows:

- Capacitance C_o and C_c are larger than C_r so that the voltages v_o and v_{Cc} are constant during one switching period.
- The inductances L_1 and L_2 are larger than the resonant inductance L_r.
- The energy stored in the resonant inductor L_r is greater than energy stored in the resonant capacitor C_r in order to achieve ZVS for main switch.

In the proposed converter, there are six operating stages in one switching cycle of operation. Fig. 2 illustrates the time sequence of key waveforms in one switching cycle. Fig. 3 shows the equivalent circuits of six operating stages in one switching cycle.

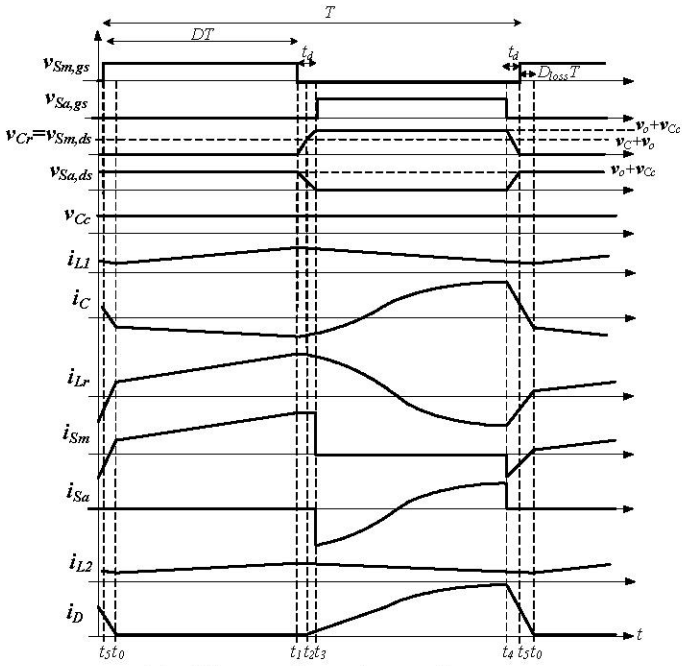


Fig. 2 Key waveforms of proposed converter.

***Stage 1* [$t_0<t<t_1$]:** In this stage, S_m is turned on and S_a is turned off. The voltage across on the input inductor L_1 and resonant inductor L_r equals the input voltage, $v_{L1}+v_{Lr}=v_{in}$. The capacitor voltage $v_C=v_{L2}+v_{Lr}$. The diode D is turned off. The input inductor current i_{L1} and output inductor current i_{L2} increase linearly in this stage. The switch currents $i_{Sm}=i_{Lr}=i_{L1}+i_{L2}$ and $i_{Sa}=0$. The load current discharges the output capacitor C_o. This stage ends at time $t=t_1$ when S is turned off.

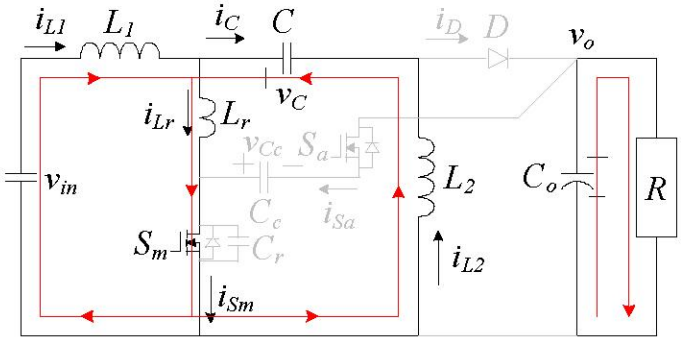
***Stage 2* [$t_1<t<t_2$]:** This stage starts at t_2 when S is turned off. Since $C>>C_r$, the capacitor voltage v_C is almost constant. The currents i_{L1}, i_{L2} and i_{Lr} are almost constant in this stage. Capacitor C_r is charged linearly from zero voltage to v_C+v_o-$v_{Lr}\approx v_C+v_o$. The output diode D is still turned off. This stage ends at t_2 when resonant capacitor voltage $v_{Cr}=v_C+v_o$.

***Stage 3* [$t_2<t<t_3$]:** This stage starts at t_2 when $v_{Cr}=v_C+v_o$ and ends at t_3 when $v_{Cr}=v_{Cc}+v_o$. At t_3, the output diode D starts conducting. The input inductor voltage $v_{L1}=v_{in}$-v_C-v_o and output inductor voltage v_{L2}= -v_o. The input and output inductor currents i_{L1} and i_{L2} decrease. In this stage, the resonant tank includes inductor L_r and capacitor C_r. The output diode current $i_D=i_{L1}+i_{L2}-i_{Lr}$. At t_4, the resonant capacitor voltage $v_{Cr}=v_{Cc}+v_o$ so that the anti-parallel diode of switch S_a is turned on.

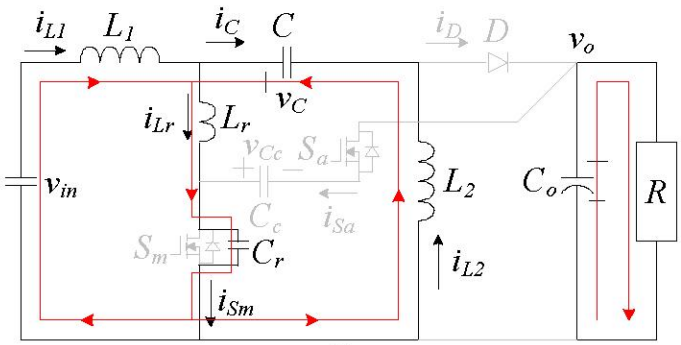
***Stage 4* [$t_3<t<t_4$]:** This stage starts at t_3 when the capacitor voltage $v_{Cr}=v_o+v_{Cc}$ and ends at t_4 when S_a is turned off. The resonant current i_{Lr} flows through capacitor C_c and anti-parallel diode of S_a. Since the clamp capacitor is large enough so that the clamp capacitor voltage is constant in this stage. Since v_{in}-v_C-v_o<0 and v_C-v_{Cc}<0, the inductor currents i_{L1}, i_{L2} and i_{Lr} all decrease in this stage. Before the inductor current i_{Lr} is negative, the switch S_a should be turned on to achieve ZVS.

***Stage 5* [$t_4<t<t_5$]:** This stage starts at t_4 when switch S_a is turned off. The inductor current i_{Lr} is negative value so that the capacitor C_r is discharged by the inductor current i_{Lr}. The input and output inductor currents i_{L1} and i_{L2} decrease in this stage. In this stage, the components L_r and C_r are resonant. If the capacitor voltage v_{Cr} can reach zero or negative value, the main switch S_m can achieve ZVS turn-on. To achieve this ZVS condition, the energy stored in the resonant inductor L_r must be greater than the energy stored in the resonant capacitor C_r, i.e. $L_r \geq C_r(v_{Cc}+v_o)^2 / i_{Lr}(t_4)^2$. This stage ends at t_5 when voltage v_{Cr} equals zero. The anti-parallel diode of switch S_m starts conducting.

***Stage 6* [$t_5<t<t_0$]:** This stage starts at t_5 when the capacitor voltage v_{Cr}=0 and the anti-parallel diode of switch S_m is turned on. The output diode D is still on. The inductor currents i_{L1} and i_{L2} decrease. The inductor current i_{Lr} and switch current i_S increase from negative value to positive value in this stage. Before switch current i_{Sm} is positive, switch S_m should be turned on to achieve ZVS. This stage ends at t_0 when the diode current i_D=0.



(a)



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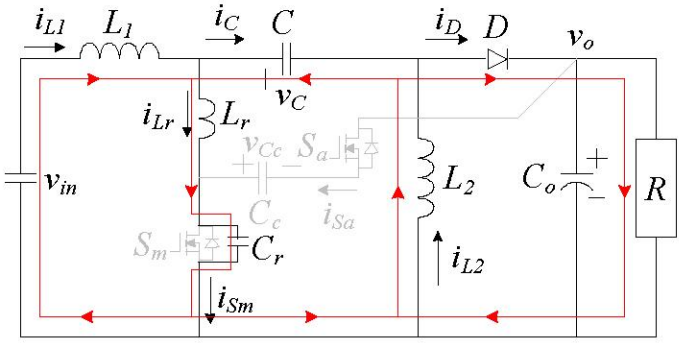

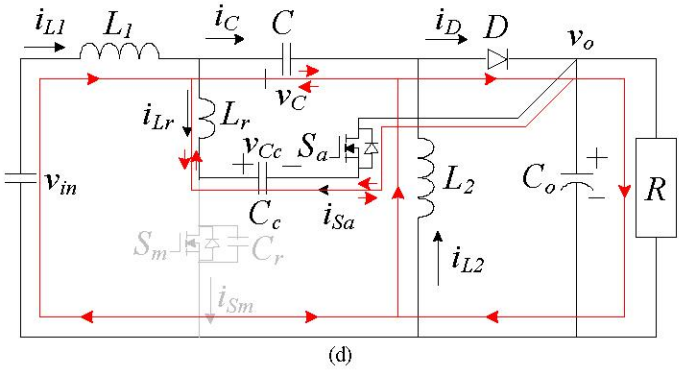

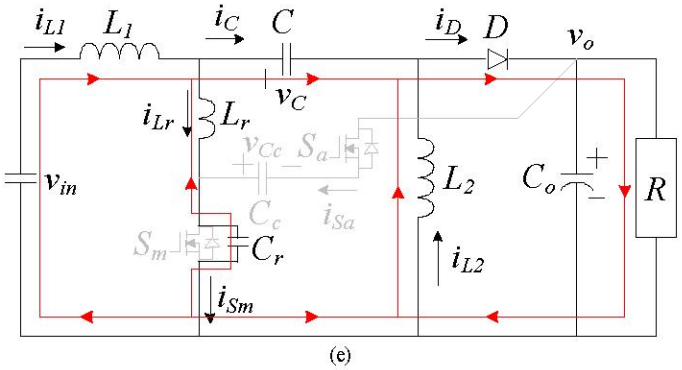

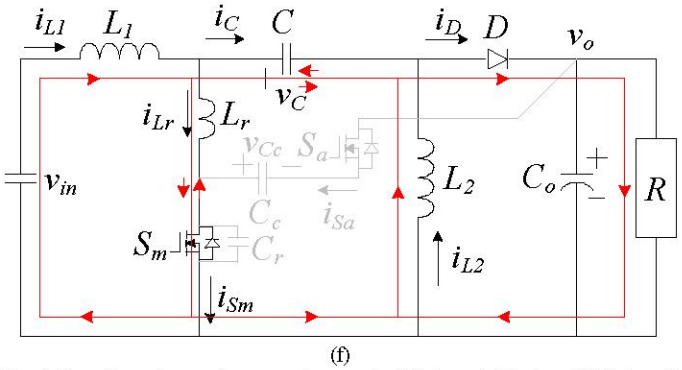

Fig. 3 Operation stages of proposed converter (a) stage 1 (b) stage 2 (c) stage 3 (d) stage 4 (e) stage 5 (f) stage 6.

III. Steady State and Design Consideration

Based on key waveforms shown in Fig. 2, the delay time t_d at stages 2, 3 and 5 during the transition interval between both switches is less than the turn-on time DT. We can ignore the delay time in the steady state analysis. The voltage-second product across the inductors during one switching cycle can be used to obtain the steady state equations of the proposed converter. The input inductor voltage $v_{L1}\approx V_{in}L_1/(L_r+L_1)$ in stage 1 and $v_{L1}=V_{in}-V_C-V_o$ in stages 4 and 6. The resonant inductor voltage $v_{Lr}\approx L_rV_{in}/(L_r+L_1)$ in stage 1, $v_{Lr}=V_C-V_{Cc}$ in stage 4, and $v_{Lr}=V_C+V_o$ in stage 6. The output inductor voltage $v_{L2}\approx V_C$ in stage 1 and $v_{L2}=-V_o$ in stages 4 and 6. Based on the voltage-second balance across the input inductor L_1, resonant inductor L_r and output inductor L_2 respectively, we can obtain the following equations.

$$\frac{V_{in}L_1}{L_1+L_r}(D-D_{loss})+(V_{in}-V_C-V_o)(1-D+D_{loss})=0 \quad (1)$$

$$\frac{V_{in}L_r}{L_1+L_r}(D-D_{loss})+(V_C-V_{Cc})(1-D)+(V_C+V_o)D_{loss}=0 \quad (2)$$

$$V_C(D-D_{loss})-V_o(1-D+D_{loss})=0 \quad (3)$$

where D is the duty cycle of main switch S_m and D_{loss} is the duty cycle loss of the proposed converter at stage 6. From (1)-(3), we can obtain the clamp capacitor voltage V_{Cc}, capacitor voltage V_C and output voltage V_o.

$$V_{Cc}=\frac{V_{in}}{1-D}-V_{in}\frac{D_{eff}}{1-D_{eff}}\left(1-\frac{L_rD_{eff}}{L_1+L_r}\right) \quad (4)$$

$$V_C=V_{in}\left(1-\frac{L_rD_{eff}}{L_1+L_r}\right) \quad (5)$$

$$V_o=V_{in}\frac{D_{eff}}{1-D_{eff}}\left(1-\frac{L_rD_{eff}}{L_1+L_r}\right) \quad (6)$$

where $D_{eff}=D-D_{loss}$. If the ripple current Δi_{L1} on the input inductor is given, the input inductance can be obtained as:

$$L_1\approx DTV_{in}/\Delta i_{L1} \quad (7)$$

The root-mean-square (rms) current on the input inductor is expressed as:

$$I_{L1,rms}\approx I_{L1}\sqrt{1+\left(\frac{\Delta i_{L1}}{I_{L1}}\right)^2/12} \quad (8)$$

where $I_{L1}=V_oI_o/V_{in}$. The maximum input inductor current is given as:

$$I_{L1,\max}\approx I_{L1}+\frac{\Delta i_{L1}}{2} \quad (9)$$

If the ripple current Δi_{L2} on the output inductor is given, the output inductance can be obtained as:

$$L_2\approx(1-D)TV_o/\Delta i_{L2} \quad (10)$$

The rms current $I_{L2,rms}$ and maximum current $I_{L2,max}$ on the output inductor are expressed as:

$$I_{L2,rms}\approx I_{L2}\sqrt{1+\left(\frac{\Delta i_{L2}}{I_{L2}}\right)^2/12},\quad I_{L2,\max}\approx I_{L2}+\frac{\Delta i_{L2}}{2} \quad (11)$$

where $I_{L2}=I_o$. The average current of main switch S_m is

$$I_{Sm}\approx D(I_{L1}+I_{L2})=\frac{DI_o}{1-D} \quad (12)$$

The maximum switch current $I_{Sm,max}$ and rms switch current $I_{Sm,rms}$ are given as:

$$I_{Sm,\max} = I_{L1} + I_{L2} + \frac{\Delta i_{L1} + \Delta i_{L2}}{2}$$

$$I_{Sm,rms} \approx \sqrt{D[(I_{L1} + I_{L2})^2 + \frac{(\Delta i_{L1} + \Delta i_{L2})^2}{12}]} \quad (13)$$

The peak switch current of auxiliary switch $I_{Sa,max} \approx I_{S,max}$. The voltage stresses of switches S_m and S_a are given as:

$$V_{Sm,stress} = V_{Sa,stress} \approx V_o + V_{Cc} = \frac{V_{in}}{(1-D)} \quad (14)$$

The average and maximum current of output diode are expressed as:

$$I_D \approx I_o,\ I_{D,\max} \approx \frac{2I_o}{(1-D_{eff})} \quad (15)$$

The voltage stress of output diode is given as:

$$V_{D,stress} \approx V_C + V_o = \frac{V_o}{D_{eff}} \quad (16)$$

If the ripple voltage Δv_C is given, the capacitance C is given as:

$$C \approx I_{L2} DT / \Delta v_C \quad (17)$$

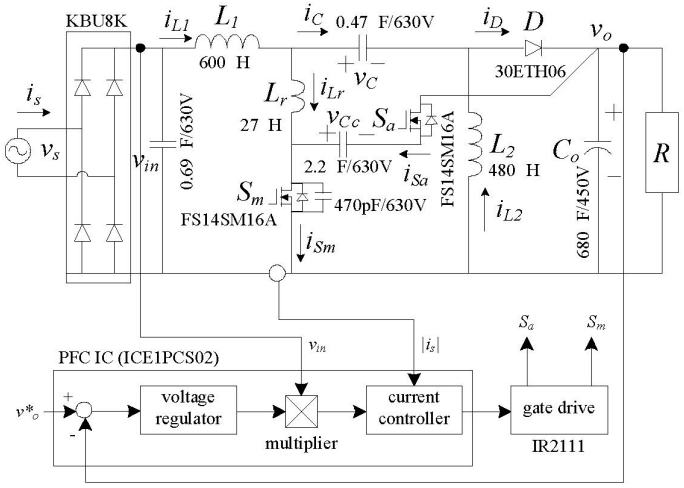

Fig. 4 Proposed ZVS sepic converter in PFC application.

The voltage stress of clamp capacitor C is $V_C+\Delta v_C/2$. To achieve ZVS condition of main switch S_m in stage 5, the energy stored in inductor L_r must be greater than the energy stored in capacitor C_r, i.e. $L_r \geq C_r(v_{Cc} + v_o)^2 / i_{Lr}(t_4)^2$. The clamp capacitor C_c and resonant inductor L_r are resonant about half of the resonant period in stage 4. The clamp capacitance C_c is expressed as $C_c \geq [(1-D)T]^2/(\pi^2 L_r)$. Fig. 4 gives the prototype circuit configuration of the proposed converter in power factor correction. The ac source current is controlled to be a sinusoidal waveform with nearly unity power factor. The general power factor correction IC such as UC3854 or ICE1PCS02 is used to regulate output voltage and track line current. Two control loops are used in the control circuit. The inner one is designed to track line current command with unity displacement power factor and unity distortion factor. The average current control scheme with carrier-based PWM is used to track current command. The outer loop is designed to regulate the dc-link voltage and keep it at the desired value.

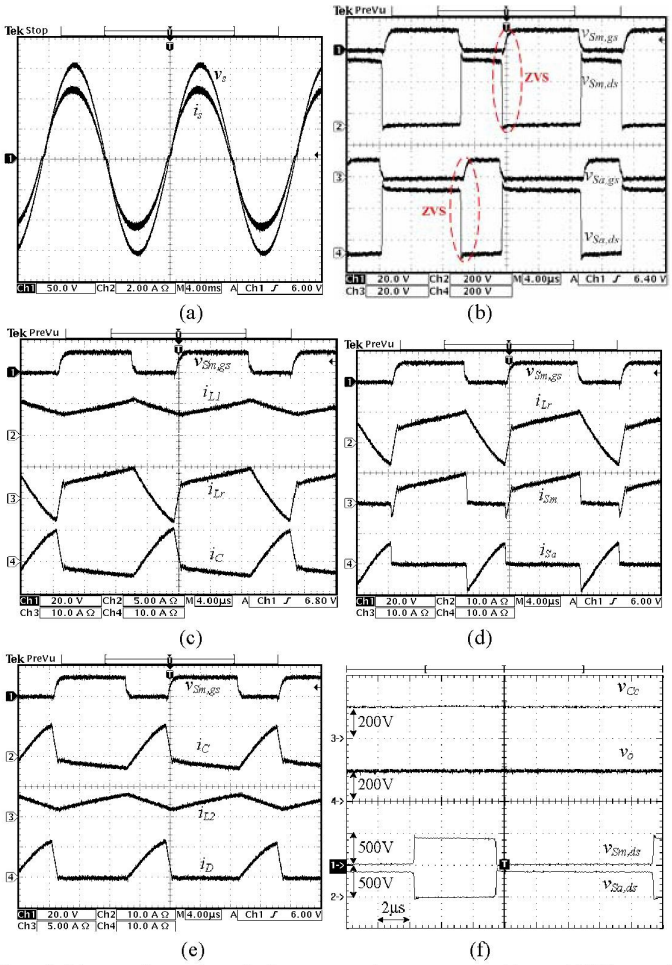

Fig. 5 Measured results of the proposed converter with v_s=110V$_{rms}$ and P_o=300W.

IV. Experimental Results

The circuit performance is verified by the experimental results based on a laboratory prototype. The circuit specifications of the prototype circuit are: output power P_o=300W; input voltage v_{ac}=110V$_{rms}$; output voltage v_o=200V; and switching frequency f_s=65kHz. Fig. 5 shows the measured results of the proposed converter at the rated output power. Fig. 5(a) shows the measured waveforms of ac source voltage and line current. The line current is a sinusoidal waveform in phase with source voltage. The measured power factor is 0.99 and the total harmonic distortion is 3.88%. Fig. 5(b) shows the measured waveforms of gate and drain voltages of both switches. Before the main and auxiliary switches are turned on, the drain voltages $v_{Sm,ds}$ and $v_{Sa,ds}$ have been decreased to zero voltage. Therefore the ZVS operations of both switches are achieved. Fig. 5(c) gives the measured waveforms of gate

voltages $v_{Sm,gs}$, inductor currents i_{L1} and i_{Lr} and capacitor current i_C. It is clear that the input inductor current $i_{L1}=i_{Lr}+i_C$. Fig. 5(d) illustrates the measured waveforms of gate voltage $v_{Sm,gs}$, switch currents i_{Sm} and i_{Sa} and inductor current i_{Lr}. When S_m is turned on, the inductor current $i_{Lr}=i_{Sm}$ and $i_{Sa}=0$. When S_m is turned off and S_a is turned on, the inductor current $i_{Lr}=-i_{Sa}$ and $i_{Sm}=0$. Fig. 5(e) shows the measured waveforms of gate voltage $v_{Sm,gs}$, diode current i_D, output inductor current i_{L2} and capacitor current i_C. When S_m is turned on, the diode current $i_D=0$ and $i_C=-i_{L2}$. When S_m is turned off, the diode current $i_D=i_C+i_{L2}$. Fig. 5(f) gives the measured results of drain voltages $v_{Sm,ds}$ and $v_{Sa,ds}$, output voltage v_o and clamp capacitor voltage v_{Cc}. In these measured waveforms, it is clear that $v_{Sm,ds}+v_{Sa,ds}=v_o+v_{Cc}$. Fig. 6 gives the measured waveforms of ac source voltage and line current at the $220V_{rms}$ ac input voltage. The output voltage is still controlled at 200V. When ac input voltage is less than 200V, the proposed converter is operated at the boost type. When ac input voltage is greater than 200V, the converter is operated at the buck type. Table 1 gives the measured current harmonics of the proposed converter at rated output power. The proposed converter can be operated at wide ac input voltage range with power factor correction. Fig. 7 gives the measured output voltage, input ac source voltage and line current under the load variation. The line current and dc bus voltage are at steady state after one or two line cycle. Based on the experimental results, the sinusoidal line current with nearly unity power factor is generated from the proposed converter. The switches are operated at ZVS turn-on.

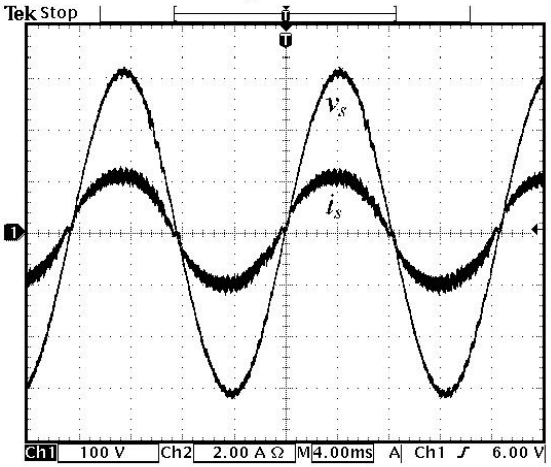

Fig. 6 Measured waveforms of ac source voltage and line current of the proposed converter at $220V_{rms}$ input voltage and P_o=300W.

Table 1: Measured current harmonics (% of the fundamental current).

harmonic	proposed converter at v_s=110V	proposed converter at v_s=220V
3	2.91%	3.58%
5	1.31%	1.30%
7	1.16%	0.92%
9	1.12%	1.10%
11	0.77%	1.01%
13	0.59%	0.67%
15	0.50%	0.51%
17	0.53%	0.50%
19	0.51%	0.49%
THD (%)	3.88%	4.68%

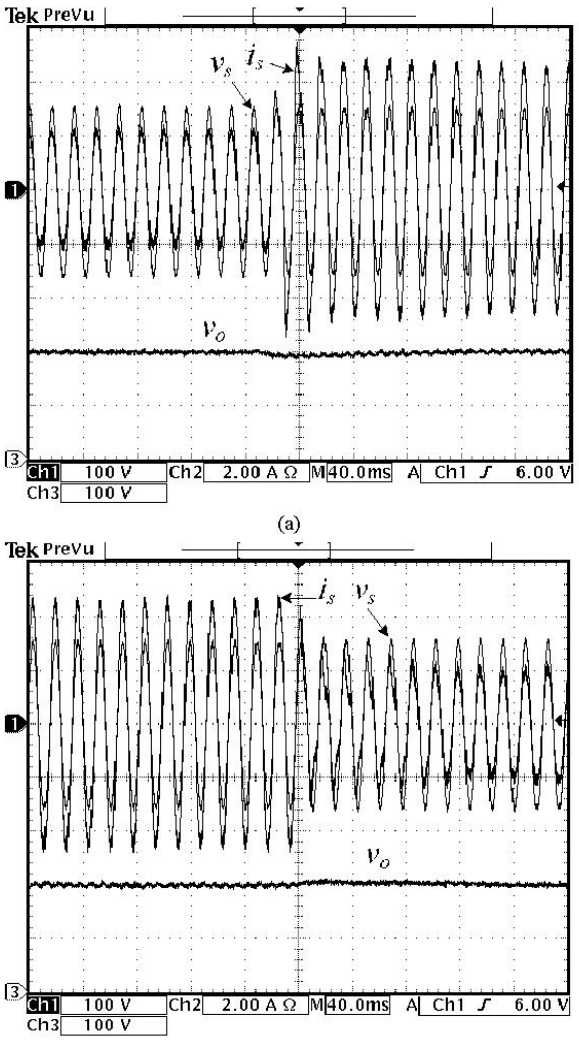

Fig. 7 Measured output voltage, ac source voltage and line current under the load variation (a) from P_o=150W to P_o=300W (b) from P_o=300W to P_o=150W

V. Conclusion

A soft switching sepic converter with active clamp topology is presented to achieve ZVS operation of the switching devices. The active clamp circuit can limit the voltage stress on power switches and achieve ZVS turn-on so that the switching losses on the switches can be reduced. System analysis and circuit design consideration are presented in detail. The application of the proposed converter in power factor correction was tested and shown in this paper to draw a clean sinusoidal line current from the ac source and obtain a nearly unity power factor. The proposed converter can be implemented by a commercial PFC IC and a gate drive to reduce current harmonics and increase power factor. Based on the experimental results, the high power factor, low total harmonic distortion, and high circuit efficiency were obtained in the proposed ZVS converter.

Acknowledgment

This project is supported by the National Science Council of Taiwan under Grant NSC96-ET-7-224-002-ET.

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