HIGH EFFICIENCY DC-DC CONVERTER

Ionel Dan Jitaru

ROMPOWER
2378 N. Sun Lake Pl. Tucson AZ 85749
Tel (602) 749-2033
Fax (602) 749-8430

ABSTRACT

A family of converter topologies employing two complementary switches in the primary and two MOSFET synchronous rectifiers in the secondary is presented. The use of two complementary switches in the primary leads to soft transitions across the switching elements, and the complementary square waveforms reflected in the secondary offers a simple and efficient driving waveform for the synchronous rectifiers. Employing one of these topological configuration, a very high efficiency and high power density 100W converter was implemented. The converter operates from an input voltage of 35V to 72V, providing 5V at 20A, with an efficiency above 90% at full load. High efficiency combined with the use of a full integrated multilayers PCB magnetic technology has allowed a power density of 52W/inc3.

INTRODUCTION

The continuous quest for higher power density and higher efficiency DC-DC converters is accelerated by the telecommunication market, which requires a saving in space and energy. By utilizing very creative packaging techniques the power density of the DC-DC converters has exceeded 50W/inc3 and is going towards 100W/inc3. However the average efficiency of 81% to 86% for 5V output voltage, has moved the problem of the power density towards a thermal management problem at the system level. For an effective volumetric efficiency at the system level the high power density of the DC-DC converters has to be associated with a higher efficiency. An increase in efficiency from 83% to 90.7% will double the output power for the same heat dissipation. This paper presents a family of converter topologies which are compatible with a simple MOSFET synchronous rectification circuit, sometimes referred to as self-driven implementation.

FORWARD CONVERTER WITH CONVENTIONAL RESET AND SYNCHRONOUS RECTIFIERS

The performances of self-driven synchronous rectification is dependent of the resetting technique of the transformer, since the synchronous rectifiers are driven by the voltage reflected to the secondary winding.

In a conventional resetting technique which employs a third wire resetting means, the driving waveforms for the synchronous rectifiers exhibit a dead time as is presented in figure 1. During the dead time period the body diode of the freewheeling synchronous rectifier is forced into conduction. This will impact the efficiency of the converter through two mechanisms. The forward voltage drop of the body diode is larger than that of a schottky rectifiers. The second mechanism which impacts the efficiency especially at high frequency is the reverse recovery losses when the freewheeling rectifier is turned off. To minimize the effect of reverse recovery losses the switching frequency has to be held low which will conflict with the initial goal of high power density. An obvious solution is to add a supplementary schottky rectifier in

parallel with freewheeling synchronous rectifier. In this way the loss in efficiency due to the forward voltage drop of the body diode is eliminated. The reverse recovery losses due to the body diode conduction will be also minimized [1].

For topologies in which the secondary voltage is not suitable for a self-driven implementation such as conventional forward with third wire reset, a control driven approach is suggested. In this method, which is described in figure 2, the transistors Q2 and Q3 are driven by gate-drive signals derived form the primary-switch gate drive. In this case the conduction time of the rectifiers are independent of the transformer resetting method. However, in order to prevent cross conduction phenomenon, in which both synchronous rectifiers would conduct, a dead time between the gate drive signal must be introduced. During the dead time the body diode of the synchronous rectifier may conduct, which will increase the reverse recovery losses. Therefore the performance of the converter using control driven synchronous rectifiers are highly dependent of the gate drive timing.

TOPOLOGIES COMPATIBLE WITH SELF-DRIVEN SYNCHRONOUS RECTIFIERS

In order to minimize the conduction time of the body diode in the synchronous rectifiers, the gate drive signal for the sincro-MOSFETs have to be complementary with a small dead time in between. In the same time the amplitude of these signals have to be suitable for a proper control of the MOSFET. As is presented in [2] a large family of soft transition, constant frequency topologies can be derived by employing two complementary switches with a small dead time in between. The soft transitions occurs during the dead time period. In some of these topologies, however, the amplitude of the signal reflected in the secondary is highly dependent of the duty cycle. As is mentioned in [2], this will affect the amplitude of the drive gate signal, and as result these topologies in spite of complementary square waveforms across the secondary winding are not suitable for self-driven synchronous rectification.

Another important consideration is the amplitude of the gate signal versus input voltage. This will limit the input voltage range and also the turn

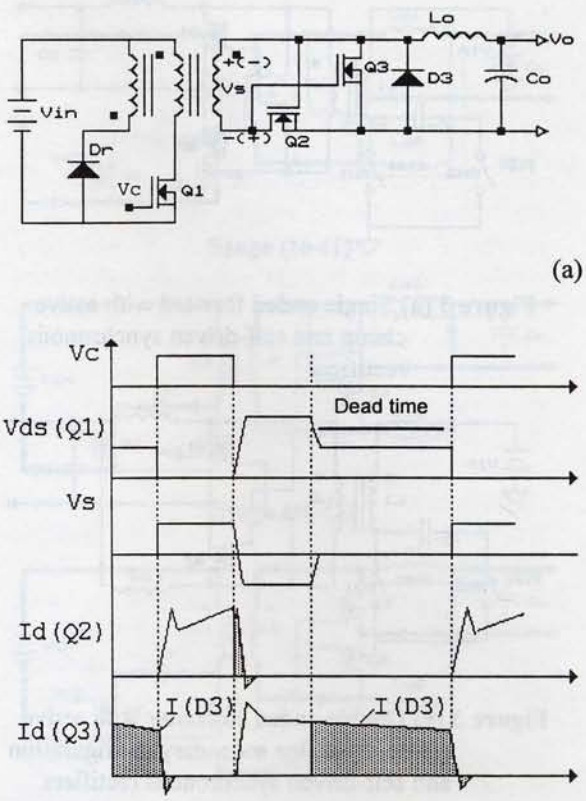


Figure 1 Forward converter with self-driven synchronous rectifiers
(a) circuit diagram
(b) typical waveforms

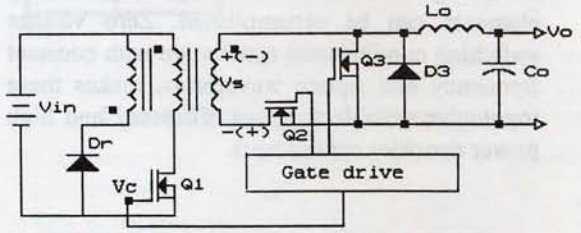


Figure 2 Forward converter with control-driven synchronous rectifiers

ratio of the transformer. For an input voltage range of 2:1 and output voltage of 5V and even 3.3V the self-driven synchronous is a simple and economical choice. However for applications which require a large input voltage range such as those which have to comply with military specifications, the control driven synchronous rectification is the preferable choice.

In figure 3 are presented four topological configuration which are employing self-driven synchronous rectification means. In the primary

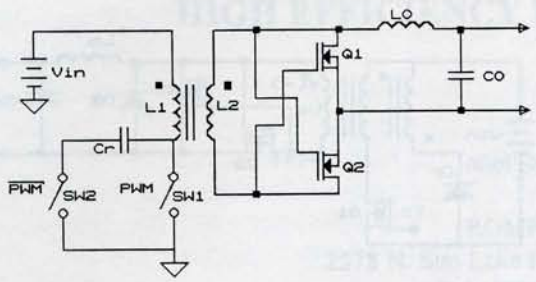


Figure 3 (a) Single ended forward with active clamp and self-driven synchronous rectifiers

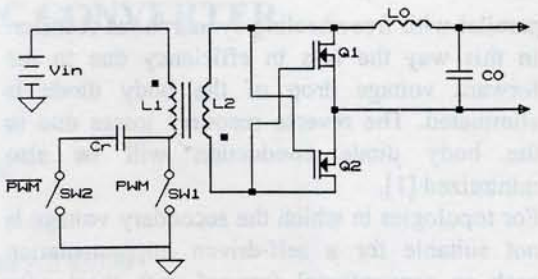


Figure 3 (b) "Modified" flyback with active clamp and self-driven synchronous rectifiers

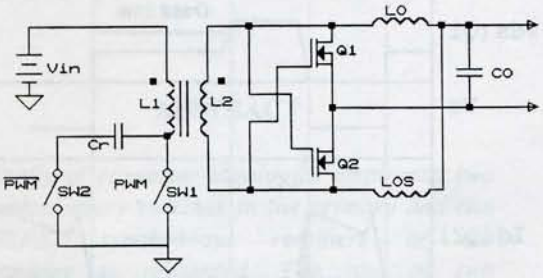


Figure 3 (c) Double ended converter with active clamp, hybridge secondary configuration and self-driven synchronous rectifiers

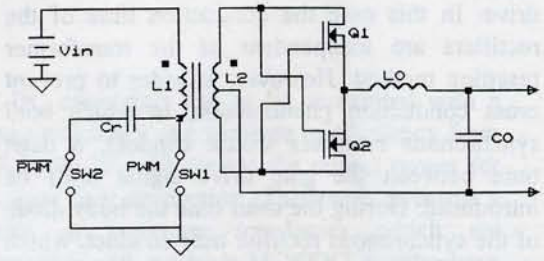


Figure 3 (d) Double ended converter with active clamp, secondary center tap and self-driven synchronous rectifiers

section there are two complementary switching elements. By employing some of the techniques presented in [2], [6] [3] and [7], zero voltage switching conditions across the switching elements can be accomplished. Zero voltage switching conditions in association with constant frequency and square waveforms, makes these topologies suitable for high efficiency and high power densities applications.

DOUBLE ENDED CONVERTER WITH ACTIVE CLAMP AND SYNCHRONOUS RECTIFICATION

The design goal was to implement a very high efficiency (>90%) 100W 5V@20A DC-DC converter operating from an input voltage range of 35V to 72V, with a power density target of 50W/inc.

The high power density requirements demands the use of a topology in which the size of the magnetic is minimized. In the double ended converter with and without center tap depicted in figure 3d and 3c, the transfer of energy from the primary to secondary is continuous, which reduces considerably the size of the output filter. Another common method for the size reduction of the output filter is by increasing the operation frequency. The operation frequency is a trade between the converter efficiency and the power density. During the dead time between the conduction of the synchronous rectifiers the body diode become active, and as result there are always losses due to reverse recovery. Adding schottky diode in parallel with the synchronous MOSFET does not impact significantly the reverse recovery losses. This is due to the non ideal characteristics of the circuit, such as stray inductance and due to non ideal dynamic characteristics of the schottky rectifier.

The switching frequency at which I got the best compromise, of power density and efficiency was 300Khz. Another consideration which limits the switching frequency was the driving losses for the power switch, reset switch and the gate drive losses for the synchronous rectifiers.

The topology employed in the experimental evaluation is depicted in figure 3 (c).

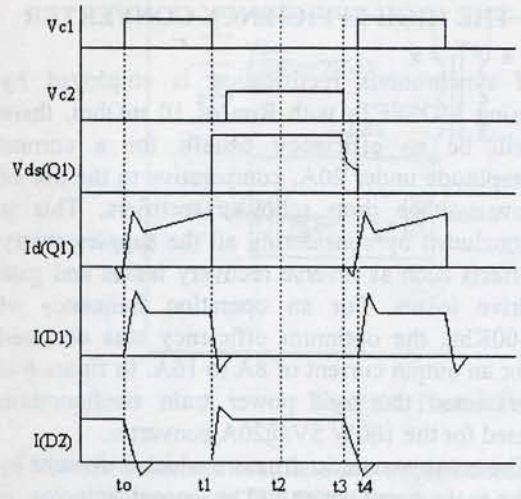
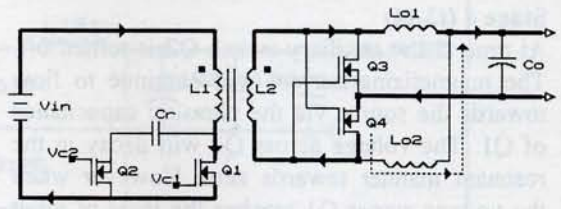
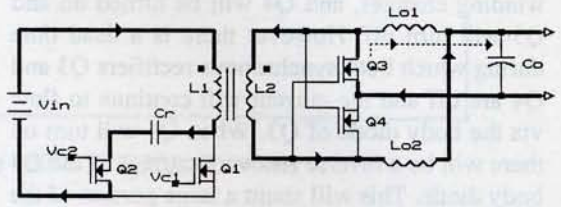


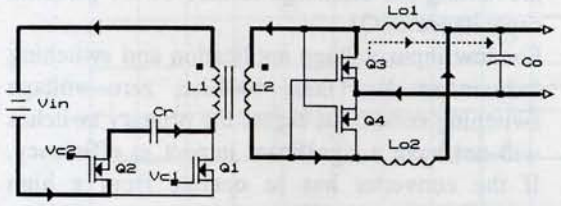
Figure 4 Ideal waveforms of the double ended converter with hybridge secondary configuration and synchronous rectifiers



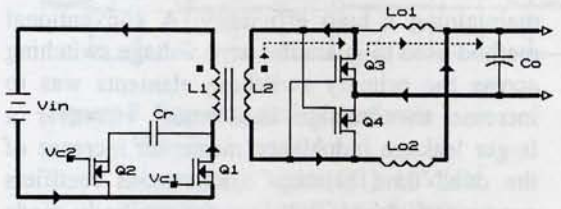
Stage (to-t1)



Stage (t1-t2)



Stage (t2-t3)



Stage (t3-t4)

Figure 5 Four Stages of Operation

The operation of this circuit can be divided into four operating modes depicted in figure 4 and 5.

STAGE 1 (to-t1)

At the moment "to", the power switch Q1 turns on and the current is flowing from the input source through primary winding. There will be a voltage across the secondary winding which will turn on Q4 and the current in secondary will flow through Lo1, and the secondary winding L2. The output choke Lo2 will maintain its current via Q4 and output load.

STAGE 2 (t1-t2)

At the moment t1 the power switch Q1 will turn off, and the current will continue to flow into the primary section via Cr and Q2. Initially current will flow through the body of Q2 until Q2 will be turned on. For better efficiency a diode will be connected in parallel to the body diode of Q2. The resonant frequency created by the primary winding and Cr has to be much lower than the operation frequency. As a result the voltage across Cr will not change during a cycle period. The voltage across Cr after several cycles will reach a steady level of Vin/(1-D)

Stage 3 (t2-t3)

During the second half of the reset cycle the current through Cr and L1 is mirrored back towards the input source. This time via Q2 which was turned on sometime in between t1 and t2. It is important to mention that at the moment when Q2 turns on, its body diode or possible a supplementary diode in parallel with the MOSFET was conducting. As a result the auxiliary switch Q2 turns on at zero voltage conditions. The polarity in the secondary did not change, and the secondary current flow is the same as during t1-t2 interval.

Stage 4 (t3-t4)

At time t3 the auxiliary switch Q2 is turned off. The magnetizing current will continue to flow towards the source via the parasitic capacitance of Q1. The voltage across Q1 will decay in the resonant manner towards zero. However when the voltage across Q1 reaches the level of input voltage , the polarity across the secondary winding changes, and Q4 will be turned on and Q3 will turn off. However there is a dead time during which both synchronous rectifiers Q3 and Q4 are off and the current will continue to flow via the body diode of Q3. When Q4 will turn on there will be a reverse recovery current of the Q3 body diode. This will shunt a large portion of the magnetizing current into the secondary preventing the discharge to zero of the parasitic capacitance of Q1.

For low input voltage application and switching frequencies less than 400Khz, zero voltage switching conditions across the primary switches will not have a significant impact in efficiency. If the converter has to operate from a high voltage bus such as 200V to 420Vdc, minimizing the voltage across the primary switches at turn on is a very important factor for maintaining a high efficiency. A conventional method used to guarantee zero voltage switching across the primary switching elements was to increase the leakage inductance. However a larger leakage inductance means an increase of the dead time between synchronous rectifiers conduction, which will increase the body diode conduction time. A larger leakage inductance will also increase the circulating currents from the secondary to primary which will have a negative impact on the efficiency, especially for low input voltage converters. However, by increasing the leakage inductance there is also a positive effect due to the decrease of dI/dt through the body diode at turn off. This will decrease the amplitude of reverse recovery current and reduce the reverse recovery losses. In conclusion the effect of larger leakage inductance on the converter efficiency is relatively complex, but for a 48V input converter the experimental results have shown that minimizing the leakage inductance will maximize the efficiency. Different solution for obtaining zero voltage switching across the primary switching elements, without increasing the leakage inductance are suggested in [2], [7].

EXPERIMENTAL IMPLEMENTATION OF THE HIGH EFFICIENCY CONVERTER

If synchronous rectification is employed by using MOSFETs with Ron of 10 mOhm, there will be an efficiency benefit for a current amplitude under 20A, comparative to the use of low voltage drop schottky rectifiers. This is concluded by considering all the supplementary effects such as reverse recovery losses and gate drive losses. For an operation frequency of 300Khz, the optimum efficiency was obtained for an output current of 8A to 16A. In figure 6 is presented the base power train configuration used for the 100W 5V@20A converter.

The entire magnetic structure which is formed by the main transformer and an output inductor, is implemented on the same multilayers PCB structure. The primary winding of the transformer has four turns, in one turn per layer implementation, and the secondary has only one turn implemented by paralleling two layers of one turn. The primary and secondary were interleaved to minimize the inter winding magnetic field strength. By using a multilayers PCB of 3oz copper , the dc resistance of the primary winding is 47 mOhm and the dc resistance of the secondary winding is reduced to 2.5 mOhm. Only six layers were employed for the main transformer from the eight layers board. The remaining two layers one on the top and one on the bottom, allow the transformer winding to be buried in order to increase the power density, by utilizing the space in top of the winding area.

The output inductor has one turn, half turn for the positive bus and half turn for the return bus. The total loss in the output choke is approximately 0.4W. The winding structure of the choke is also buried in the multilayers board. The fact that all the magnetic elements are integrated on the same PCB minimizes the interconnection impedance and by burring the windings will allow a high power density implementation. The footprint of the multilayers PCB is 3" x 1.6". The height of the magnetic and base plate is .4". This would allow a power density of 52 W/inc3.

The main transformer and the output choke utilizes the same type of low profile EE core, # 43618-E&E from Magnetics. The total power loss in the transformer is 1.2W wherein .2W is core loss and 1W is copper loss.

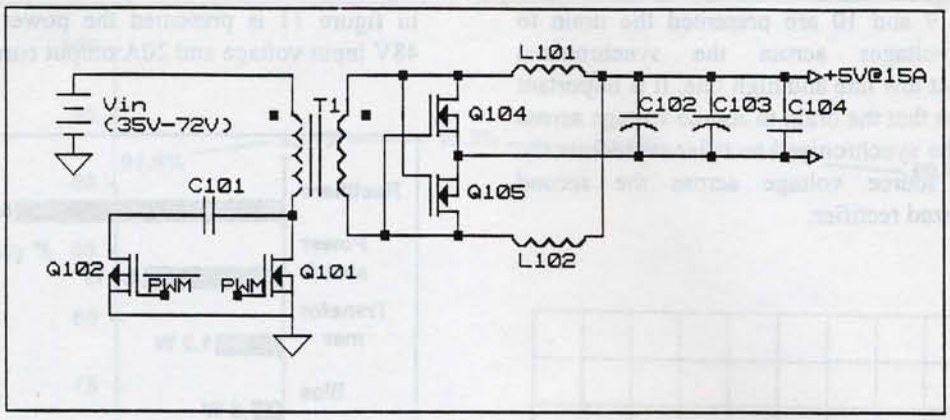


Figure 6 Power Train of the 100W 5V@20A Converter

The synchronized rectifiers are implemented by using Motorola's MTB75N05HD which are 50V, 9.5 mOhm MOSFETs in HDTMOS technology. The power dissipation on the synchronous rectifiers has two components. On component is due to forward voltage drop of Io*Ron and the second component is due to the reverse recovery losses of the body diode.

The losses due to reverse recovery of the body diode were calculated based on the current and voltage waveforms. The peak reverse recovery current is function of the temperature and dI/dt. By monitoring the current using a current probe a supplementary inductor element is added in the circuit, which may impact the measurement accuracy. At full load and nominal line the power dissipation on both synchronous rectifiers were predicted to be 5.2W. The experimental and calculated results of the overall efficiency were very close, which showed that the predictions were accurate. The losses due to reverse recovery of the body diode were approximately 20 % from the total losses of the synchronous rectifiers. The prototype was implemented by using IRF640 for the main switching element and one P channel IRFD9220 for the reset switch.

In figure 7 is presented the gate and drain voltage on the main switch Q1 at low line Vin=36V. The same waveforms are also presented in figure 8, at high line, Vin=72V. It is noticeable that the voltage across the switching element does not change too much from low line to high line, maintaining a value around 100V. The duty cycle at low line is larger that 50%, in this case reaching 65%.

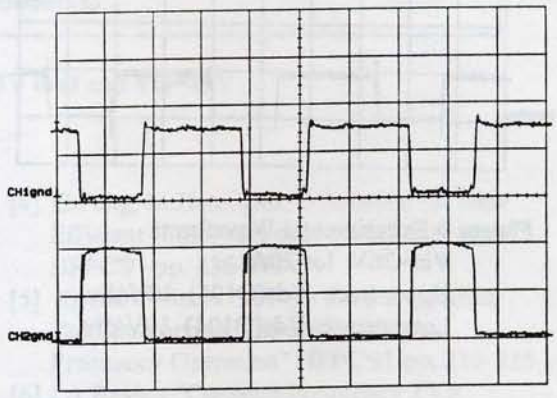


Figure 7 Experimental Waveforms
Vin=36V Io=20A
Upper trace Vgate(Q1) 10V/div
Lower trace Vds(Q1) 50V/div

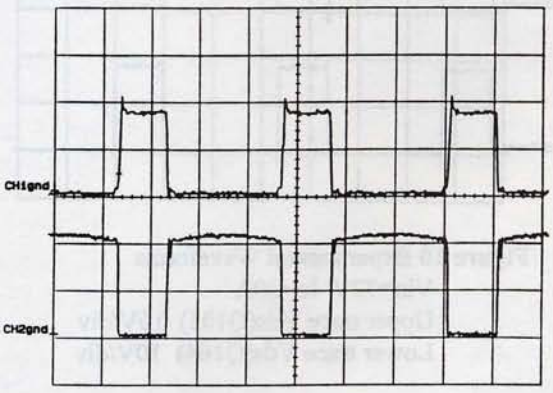


Figure 8 Experimental Waveforms
Vin=72V Io=20A
Upper trace Vgate(Q1) 10V/div
Lower trace Vds(Q1) 50V/div

In figure 9 and 10 are presented the drain to source voltages across the synchronized rectifiers at low line and high line. It is important to mention that the drain to source voltage across each of the synchronized rectifier represents the gate to source voltage across the second synchronized rectifier.

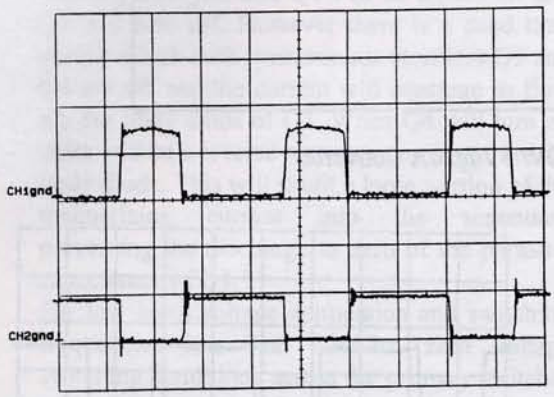


Figure 9 Experimental Waveforms
Vin=36V Io=20A
Upper trace Vds(Q105) 10V/div
Lower trace Vds(Q104) 10V/div

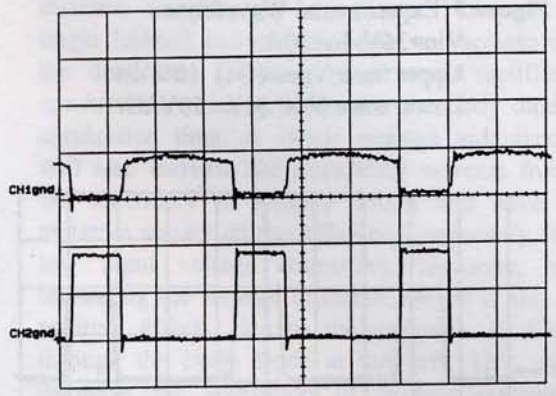


Figure 10 Experimental Waveforms
Vin=72V Io=20A
Upper trace Vds(Q105) 10V/div
Lower trace Vds(Q104) 10V/div

The efficiency displayed in figure 12 is obtained by using a conservative voltage derating for the switching elements (200%), standard magnetic cores, and conventional components.

In figure 11 is presented the power budget at 48V input voltage and 20A output current.

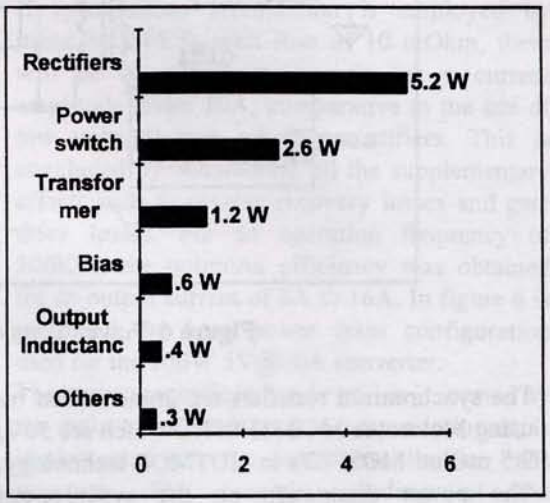


Figure 11 Power Dissipation Budget
Vin=48V Io=20A

CONCLUSION

A family of converter topologies combining two complementary switching elements in the primary with two synchronous rectifiers in secondary has been presented. An experimental 100W DC-DC converter using one of these topological configuration has been evaluated. The converter is able to provide efficiency above 90% at full load for 5V output. The experimental implementation in which the main transformer and the output choke are implemented by using multilayers board transformer technology, leads to a projected power density above 52W/inc3. The power dissipated by this 100W converter at full load is equal with the power dissipated by a 50W converter at full load with a efficiency of 83%. These results show that synchronized rectification can be employed successfully for power levels under 100W and by interleaving power trains high efficiency can be extended to higher power converters. The market niche in which the high efficiency converters will excel is board mounted converters with no supplementary cooling means. In these applications the efficiency is the only avenue for a smaller foot print and a higher power density. The high efficiency power conversion technologies will successfully apply to higher

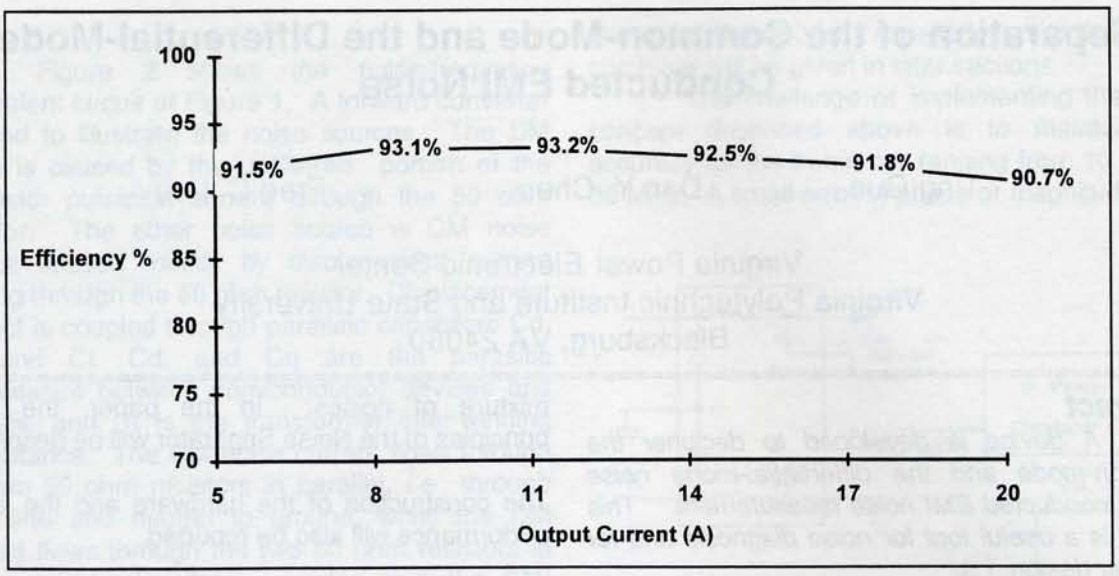


Figure 12 Efficiency at 20A@5V load and Vin=48V

power DC-DC converters, minimizing the cooling requirements at the system level. The recent improvements in components technology allows the synchronized rectifiers to compete favorably with schottky rectifiers, on a large spectrum of applications.

ACKNOWLEDGMENTS

The author gratefully acknowledge the support provided by Professor R. Zaciu from Polytechnic Institute of Bucharest. Some of the concepts presented in this paper are subject to granted patents and patent pending.

REFERENCES

[1] Millan M. Jovanovic, Jen-Ching Lin,Chen Zhou,Michael Zhang, Fred C.Lee "Design Considerations for Forward Converter With Synchronous Rectifiers" PCIM'93 Irvine, CA. pp.340-349

[2] I.D.Jitaru "New Trends in Power Conversion Technology" seminar notes HFPC'93, PAC1

[3] I.D.Jitaru "Fixed Frequency Single Ended Forward Converter Switching at Zero Voltage" U.S.Patent 5,126,931

[4] C.Peng, M.Hannigan, O.Seiersen "A New Efficient High Frequency Rectifier Circuit" HFPC'91 pp. 236-243

[5] Kevan O'Meara "A New Output Rectifier Configuration Optimized For High Frequency Operation" HFPC'91 pp. 219-225

[6] J.A.Bassett "Constant Frequency ZVS Converter with Integrated Magnetic" APEC'92 pp. 709-716

[7] Ionel Dan Jitaru "High Frequency, Soft Transition Converter" APEC'93 pp. 880-887