## BM309 Series

## 3/4 cell Li Battery Protectors

## General Description

The BM309 Series are highly integrated protection ICs for lithium-ion and lithium polymer rechargeable battery packs in notebook PCs, power tools, electric bicycles and UPS applications.
The BM309s work constantly to monitor each cell's voltage, the charge/discharge current and the environment temperature to provide overcharge, over-discharge, excess current, short circuit, abnormal charge, overheat safety protections, etc. Particularly for excess current and overheat, it provides an easy way to adjust the threshold, internal/external selectably. It also supports external bleeding for cell-capacity balance function to avoid unbalanced capacity between each cell. Thus, the battery can work for longer.
Extended function module embedded in the BM309s can make themself work for battery packs with multiple BM309s.

## Features

- Supports $3 / 4$ Series Lithium-ion and Lithium polymer rechargeable Battery or 6-20 Series if used in the extended condition
- Built-in auto-fit between $3 / 4$ cells (without any peripheral circuit added)
- Built-in protections included:
- Overcharge
- Over-discharge
- Excess current
- Short circuit
- Abnormal charge
- Over temperature
- Supports external bleeding for balance
- Supports different charge and discharge loops
- Supports external excess current
- Lower power consumption
- Package: TSSOP24


## Applications

- Notebook PC
- Power Tool
- UPS backup battery
- Electric bicycle


## Block Diagram



## - Selection Guide

## - Type Number

## BM309XXXX

- Type Number Option

The first $X$ stands for Overcharge detection threshold voltage (Vdet1)
The second $X$ stands for Over-discharge detection threshold voltage (Vdet2)
The third X stands for Excess current 1 detection threshold voltage (Vdet3)
The fourth X stands for other parameters or versions

| Type <br> Number | Vdet1 | Vdet2 | Vdet3 | Vbal1 | Vbal2 | Package |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| BM309MHFA | $4.300 \pm 0.050 \mathrm{~V}$ | $2.500 \pm 0.100 \mathrm{~V}$ | $($ Vcc -0.20$) \pm 0.030 \mathrm{~V}$ | $3.980 \pm 0.100 \mathrm{~V}$ | $2.750 \pm 0.100 \mathrm{~V}$ | TSSOP24 |
| BM309LHFA | $4.275 \pm 0.050 \mathrm{~V}$ | $2.500 \pm 0.100 \mathrm{~V}$ | $($ Vcc- 0.20$) \pm 0.030 \mathrm{~V}$ | $3.970 \pm 0.100 \mathrm{~V}$ | $2.730 \pm 0.100 \mathrm{~V}$ | TSSOP24 |
|  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |

## Pin Configuration



## Pin Description :

| Name | Pin NO. | I/O | Description |
| :---: | :---: | :---: | :--- |
| Vm | 1 | I | Voltage detection |
| Do | 2 | 0 | Discharge power Mosfet control |
| Co | 3 | O | Charge power Mosfet control |
| UP_in | 4 | I | Cell balance 1 among chips |
| Out_up | 5 | O | Cell balance 3 among chips |
| Exa | 6 | I | Excess current adjustment connected to Vcc |
| Exs | 7 | I | Excess current adjustment connected to Vss |
| Down_in | 8 | I | Cell balance 2 among chips |
| Out_down | 9 | O | Cell balance 4 among chips |
| Down_co | 10 | I | CO from under chip |
| Down_do | 11 | I | DO from under chip |
| Vin | 12 | I | Discharge current detection |
| Vp | 13 | Power | LDO output |
| K_Dp | 14 | I | Spread \& TRIM control |
| Vss | 15 | Ground | Chip ground |
| Bal4 | 16 | O | Cell4 external bleeding control |
| Vd | 17 | I | Cell4 positive input |
| Bal3 | 18 | O | Cell3 external bleeding control |
| Vc | 19 | I | Cell3 positive input |
| Bal2 | 20 | O | Cell2 external bleeding control |
| Vb | 21 | I | Cell2 positive input |
| Bal1 | 22 | O | Cell1 external bleeding control |
| Va | 23 | I | Cell1 positive input |
| Vcc | 24 | Power | Power supply |
|  |  |  |  |

## Typical Application Circuits

## Used as a single chip



Application in 3-cell battery pack
Recommended value of the resistors and capacitors is as followed:

| symbol | TYP | Range | Unit |
| :---: | :---: | :---: | :---: |
| R1 | 100 | $100 \sim 1000$ | $\Omega$ |
| R2, R3, R4 | 200 | $100 \sim 1000$ | $\Omega$ |
| R5, R6, R7 | 100 | $10 \sim$ | $\Omega$ |
| R8, R9, R10 | 100 | $10 \sim$ | $\Omega$ |
| R11, R12, R13 | 100 | $10 \sim$ | $\Omega$ |
| R14 | 2 | $1 \sim 10$ | $\mathrm{~K} \Omega$ |
| R15 | 200 | $10 \sim 1000$ | $\mathrm{~K} \Omega$ |
| R_Exa | 60 | $10 \sim 100$ | $\mathrm{~K} \Omega$ |
| R_Exs | 80 | $70 \sim 85$ | $\mathrm{~m} \Omega$ |
| R16 | - | $0 \sim 100$ | uF |
| C1, C2, C3, | 0.1 | $0.01 \sim 2.2$ |  |
| C4, C5 |  |  |  |

NOTE:
(1) Pin Down_co, Down_do can be used to control Co and Do, the priority is higher than protection circuits.
(2) Pin Vin and Vm have the same priority in the state as Excess current 1, so either can be selected to realize the Excess current 1 protect .
(3) The serial number of resistors and capacitors in the table is only applicable to 3-cell application circuit .


Recommended value of the resistors and capacitors is as followed:

| symbol | TYP | Range | Unit |
| :---: | :---: | :---: | :---: |
| R1 | 100 | $100 \sim 1000$ | $\Omega$ |
| R2, R3, R4, R5 | 200 | $100 \sim 1000$ | $\Omega$ |
| R6, R7, R8 | 100 | $10 \sim$ | $\Omega$ |
| R9, R10, R11 | 100 | $10 \sim$ | $\Omega$ |
| R12, R13, R14 | 100 | $10 \sim$ | $\Omega$ |
| R15, R16, R17 | 100 | $10 \sim$ | $\mathrm{~K} \Omega$ |
| R18 | 2 | $1 \sim 10$ | $\mathrm{~K} \Omega$ |
| R19 | 200 | $10 \sim 10001$ | $\mathrm{~K} \Omega$ |
| R_Exa | 60 | $10 \sim 100$ | $\mathrm{~m} \Omega$ |
| R_Exs | 80 | $70 \sim 85$ | KF |
| R20 | - | $0 \sim 100$ | $\Omega$ |
| C1, C2, C3, | 0.1 | $0.01 \sim 2.2$ |  |
| C4, C5, C6 |  |  |  |

## NOTE:

(1) Pin Down_co, Down_do can be used to control Co and Do, the priority is higher than protection circuits.
(2) Pin Vin and Vm have the same priority in the state as Excess current 1, so either can be selected to realize the Excess current 1 protect .
(3) The serial number of resistors and capacitors in the table is only applicable to 4-cell application circuit .

## used in extended condition



Application in 8-cell battery pack

Recommended value of the resistors and capacitors is as followed:

| symbol | TYP | Range | Unit |
| :---: | :---: | :---: | :---: |
| R1, R6 | 100 | $100 \sim 1000$ | $\Omega$ |
| R2, R3, R4, R5 | 200 | $100 \sim 1000$ | $\Omega$ |
| R7, R8, R9, R10 | 200 | $100 \sim 1000$ | $\Omega$ |
| R11, R12, R13 | 100 | $10 \sim$ | $\Omega$ |
| R14, R15, R16 | 100 | $10 \sim$ | $\Omega$ |
| R17, R18, R19 | 100 | $10 \sim$ | $\Omega$ |
| R20, R21, R22 | 100 | $10 \sim$ | $\Omega$ |
| R23, R24, R25 | 100 | $10 \sim$ | $\Omega$ |
| R26, R27, R28 | 100 | $10 \sim$ | $\Omega$ |
| R29, R30, R31 | 100 | $10 \sim$ | $\Omega$ |
| R32, R33, R34 | 100 | $10 \sim$ | $\Omega$ |
| R35 | 200 | $10 \sim 1000$ | $\mathrm{~K} \Omega$ |
| R36 | 2 | $1 \sim 10$ | $\mathrm{~K} \Omega$ |
| R37 | 1 | $0.5 \sim 2$ | $\mathrm{M} \Omega$ |
| R_Exa | 60 | $10 \sim 100$ | $\mathrm{~K} \Omega$ |
| R_Exs | 80 | $70 \sim 85$ | $\mathrm{~K} \Omega$ |
| R38 | 2 | $1 \sim 10$ | $\mathrm{~m} \Omega$ |
| R39 | - | $0 \sim 100$ |  |
| C1, C2, C3, |  |  | uF |
| C4, C5, C6 | 0.1 | $0.01 \sim 2.2$ |  |
| C7, C8, C9, |  |  |  |
| C10, C11, C12 |  |  |  |

## NOTE:

(1) Must pay attention to the proper ratio between R35 and R36, recommend value of R35:R36=100:1; D1 and D2 are used to protect P-MOSFET, recommend value of inverting breakdown voltage is 18 V .
(2) Pin Down_co, Down_do can be used to control Co and Do , the priority is higher than protection circuits.
(3) Pin Vin and Vm have the same priority in the state as Excess current 1, so either can be selected to realize the Excess current 1 protect .
(4) The serial number of resistors and capacitors in the table is only applicable to 8 -cell application circuit .

## Absolute Maximum Ratings

| symbol | Description | Range | Unit |
| :---: | :---: | :---: | :---: |
| Vcc | Power supply voltage | $5.5-40$ | V |
| V_charger | Charger input voltage | max.Vcc +40 | V |
| Vpins | Pins' high level and low level | Vss-0.3~Vdd +0.3 | V |
| Topr | Operation ambient temperature | $-40 \sim 85$ | ${ }^{\circ} \mathrm{C}$ |
| Tstg | Storage temperature | $-40 \sim 125$ | ${ }^{\circ} \mathrm{C}$ |

NOTE: The value of Vcc must higher than 5.5 V , or else the chip can not work normally.

## Electrical Characteristics ${ }^{1^{*}}\left(25{ }^{\circ} \mathrm{C}\right)$

( $\mathrm{TOPT}=25^{\circ} \mathrm{C}$ unless otherwise specified)

| Power Supply(Test circuit1) |  |  |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Symbol | Item | Test conditions | MIN | TYP | MAX | Unit |
| Vcc | Supply Voltage |  | 5.5 |  | 40 | V |
| Vp |  | $\mathrm{V} 1=\mathrm{V} 2=\mathrm{V} 3=\mathrm{V} 4=3.70 \mathrm{~V}$ | 3.0 | 3.4 | 3.7 | V |
| lope | Supply Current | $\mathrm{V} 1=\mathrm{V} 2=\mathrm{V} 3=\mathrm{V} 4=3.70 \mathrm{~V}$ |  | 40 | 70 | uA |
| Istandby |  | $\mathrm{V} 1=\mathrm{V} 2=\mathrm{V} 3=\mathrm{V} 4=2.20 \mathrm{~V}$ |  | 10 | 15 | uA |


| Overcharge(OC) And Over-discharge(OD) Protection(Test circuit2) |  |  |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Symbol | Item | Test conditions | MIN | TYP | MAX | Unit |
| Vdet1 ${ }^{2 *}$ | OC Threshold | $\begin{aligned} & \mathrm{V} 2=\mathrm{V} 3=\mathrm{V} 4=3.70 \mathrm{~V}, \\ & \mathrm{~V} 1=3.70 \mathrm{~V} \rightarrow 4.40 \mathrm{~V} \end{aligned}$ | Vdet1-0.050 | Vdet1 | Vdet1+0.050 | V |
| Tdet1 | OC Delay | $\begin{aligned} & \mathrm{V} 2=\mathrm{V} 3=\mathrm{V} 4=3.70 \mathrm{~V}, \\ & \mathrm{~V} 1=3.70 \mathrm{~V} \rightarrow 4.40 \mathrm{~V} \end{aligned}$ | 0.6 | 1.2 | 2.4 | s |
| Treset | OC Reset Delay | $\begin{gathered} \mathrm{V} 2=\mathrm{V} 3=\mathrm{V} 4=3.70 \mathrm{~V}, \\ \mathrm{~V} 1=3.70 \mathrm{~V} \rightarrow 4.40 \mathrm{~V} \rightarrow 3.70 \mathrm{~V} \end{gathered}$ | 8 | 15 | 30 | ms |
| Vrel1 ${ }^{3 *}$ | OC Release Threshold | $\begin{aligned} & \mathrm{V} 2=\mathrm{V} 3=\mathrm{V} 4=3.70 \mathrm{~V}, \\ & \mathrm{~V} 1=4.40 \mathrm{~V} \rightarrow 3.70 \mathrm{~V} \end{aligned}$ | VDET1-0.300 | VDET1-0.200 | VDET1-0.100 | V |
| Trel1 | OC Release Delay | $\begin{aligned} & \mathrm{V} 2=\mathrm{V} 3=\mathrm{V} 4=3.70 \mathrm{~V}, \\ & \mathrm{~V} 1=4.40 \mathrm{~V} \rightarrow 3.70 \mathrm{~V} \end{aligned}$ | 12 | 21 | 40 | ms |
| Vdet2 ${ }^{2 *}$ | OD Threshold | $\begin{aligned} & \mathrm{V} 2=\mathrm{V} 3=\mathrm{V} 4=3.70 \mathrm{~V}, \\ & \mathrm{~V} 1=3.30 \mathrm{~V} \rightarrow 2.20 \mathrm{~V} \end{aligned}$ | Vdet2-0.100 | Vdet2 | Vdet2+0.100 | V |
| Tdet2 | OD Delay | $\begin{aligned} & \mathrm{V} 2=\mathrm{V} 3=\mathrm{V} 4=3.70 \mathrm{~V}, \\ & \mathrm{~V} 1=3.30 \mathrm{~V} \rightarrow 2.20 \mathrm{~V} \end{aligned}$ | 18 | 36 | 72 | ms |
| Vrel2 ${ }^{3 *}$ | OD Release <br> Threshold | $\begin{aligned} & \mathrm{V} 2=\mathrm{V} 3=\mathrm{V} 4=3.70 \mathrm{~V}, \\ & \mathrm{~V} 1=2.20 \mathrm{~V} \rightarrow 3.30 \mathrm{~V} \end{aligned}$ | VDET2+0.300 | VDET2+0.500 | VDET2+0.700 | V |
| Trel2 | OD Release Delay | $\begin{aligned} & \mathrm{V} 2=\mathrm{V} 3=\mathrm{V} 4=3.70 \mathrm{~V}, \\ & \mathrm{~V} 1=2.20 \mathrm{~V} \rightarrow 3.30 \mathrm{~V} \end{aligned}$ | 2 | 6 | 12 | ms |

Excess Current(EX) \& Short Circuit(SC) And Abnormal Charge(AB) Protection(Test circuit3)

| Symbol | Item | Test conditions | MIN | TYP | MAX | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| $\mathrm{Vdet3}^{4^{*}}$ | EX1 Threshold | $\mathrm{V} 1=\mathrm{V} 2=\mathrm{V} 3=\mathrm{V} 4=3.70 \mathrm{~V}$ | $\mathrm{Vcc}-0.170$ | $\mathrm{Vcc}-0.200$ | $\mathrm{Vcc}-0.230$ | V |
| Tdet3 | EX1 Delay | $\mathrm{V} 1=\mathrm{V} 2=\mathrm{V} 3=\mathrm{V} 4=3.70 \mathrm{~V}$ | 13 | 27 | 54 | ms |


| $V \operatorname{det} 44^{*}$ | EX2 Threshold | $\mathrm{V} 1=\mathrm{V} 2=\mathrm{V} 3=\mathrm{V} 4=3.70 \mathrm{~V}$ | Vcc-0.500 | Vcc-0.600 | Vcc-0.700 | V |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Tdet4 | EX2 Delay | $\mathrm{V} 1=\mathrm{V} 2=\mathrm{V} 3=\mathrm{V} 4=3.70 \mathrm{~V}$ | 5 | 9 | 18 | ms |
| Vshort | SC Threshold | $\mathrm{V} 1=\mathrm{V} 2=\mathrm{V} 3=\mathrm{V} 4=3.70 \mathrm{~V}$ | Vcc-1.200 | Vcc-1.800 | Vcc-2.400 | V |
| Tshort | SC Delay | $\mathrm{V} 1=\mathrm{V} 2=\mathrm{V} 3=\mathrm{V} 4=3.70 \mathrm{~V}$ |  |  | 0.4 | ms |
| Trex | EX \& SC Release Delay | $\mathrm{V} 1=\mathrm{V} 2=\mathrm{V} 3=\mathrm{V} 4=3.70 \mathrm{~V}$ | 2 | 4 | 8 | ms |
| Vab | AB Threshold | $\mathrm{V} 1=\mathrm{V} 2=\mathrm{V} 3=\mathrm{V} 4=3.70 \mathrm{~V}$ | Vcc+0.170 | Vcc+0.200 | Vcc+0.230 | V |
| Tab | AB Delay | $\mathrm{V} 1=\mathrm{V} 2=\mathrm{V} 3=\mathrm{V} 4=3.70 \mathrm{~V}$ | 9 | 18 | 36 | ms |
| Vcha | Charger detection threshold | $\begin{gathered} \mathrm{V} 1=\mathrm{V} 2=\mathrm{V} 3=3.70 \mathrm{~V} \\ \mathrm{~V} 4=2.20 \mathrm{~V} \end{gathered}$ | Vcc+0.170 | Vcc+0.200 | Vcc+0.230 | V |
| Vin ${ }^{\text { }}$ | Discharge current detection threshold | $\mathrm{V} 1=\mathrm{V} 2=\mathrm{V} 3=\mathrm{V} 4=3.70 \mathrm{~V}$ | 0.170 | 0.200 | 0.230 | V |


| Cell Balance And OV Charge(Test circuit4) |  |  |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Symbol | Item | Test conditions | MIN | TYP | MAX | Unit |
| Vbal1 | Cell Balance threshold1 | $\begin{aligned} & \mathrm{V} 2=\mathrm{V} 3=\mathrm{V} 4=3.70 \mathrm{~V} \\ & \mathrm{~V} 1=3.70 \mathrm{~V} \rightarrow 4.20 \mathrm{~V} \end{aligned}$ | Vbal1-0.100 | Vbal1 | Vbal1+0.100 | V |
| Vbal2 | Cell Balance threshold2 | $\begin{aligned} & \mathrm{V} 2=\mathrm{V} 3=\mathrm{V} 4=3.70 \mathrm{~V} \\ & \mathrm{~V} 1=3.70 \mathrm{~V} \rightarrow 2.60 \mathrm{~V} \end{aligned}$ | Vbal2-0.100 | Vbal2 | Vbal2+0.100 | V |


| Over Temperature(OT) Protection |  |  |  |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Symbol | Item | Test conditions | MIN | TYP | MAX | Unit |  |
| Tot | OT Threshold | $\mathrm{V} 1=\mathrm{V} 2=\mathrm{V} 3=\mathrm{V} 4=3.70 \mathrm{~V}$ | 105 | 115 | 125 | ${ }^{\circ} \mathrm{C}$ |  |
| Totr | OT Release Threshold | $\mathrm{V} 1=\mathrm{V} 2=\mathrm{V} 3=\mathrm{V} 4=3.70 \mathrm{~V}$ | 85 | 95 | 105 | ${ }^{\circ} \mathrm{C}$ |  |

Pin drive capacity(Test circuit5, 6, 7, 8)

| Symbol | Item | Test conditions | MIN | TYP | MAX | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| RCo | Co output resistance | normal state, Co"L" | 0.8 | 1.5 | 2.2 | $\mathrm{k} \Omega$ |
|  |  | protection state, Co"H" | 0.8 | 1.5 | 2.2 | $\mathrm{k} \Omega$ |


| RDo | Do output resistance | normal state, Do"L" | 0.8 | 1.5 | 2.2 | k $\Omega$ |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | protection state, Do"H" | 0.8 | 1.5 | 2.2 | k $\Omega$ |
| RBal1 | RBleed1 output resistance | on state,"H" | 1.3 | 2.7 | 4.1 | k $\Omega$ |
|  |  | off state,"L" | 1.5 | 3.0 | 4.5 | k $\Omega$ |
| RBal2 | RBleed2 output resistance | on state, "H" | 1.5 | 3.0 | 4.5 | k $\Omega$ |
|  |  | off state,"L" | 1.0 | 2.0 | 3.0 | k $\Omega$ |
| RBal3 | RBleed3 output resistance | on state,"H" | 1.5 | 3.0 | 4.5 | k $\Omega$ |
|  |  | off state,"L" | 1.0 | 2.0 | 3.0 | k $\Omega$ |
| RBal4 | RBleed4 output resistance | on state, "H" | 0.9 | 1.7 | 2.5 | k $\Omega$ |
|  |  | off state,"L" | 0.4 | 0.7 | 1.0 | k $\Omega$ |
| Idrive | Current drive capacity of Vp | $\mathrm{V} 1=\mathrm{V} 2=\mathrm{V} 3=\mathrm{V} 4=3.70 \mathrm{~V}$ | 200 | 400 | 600 | uA |
| RVMC | Resistance between Vm and VCC | $\mathrm{V} 1=\mathrm{V} 2=\mathrm{V} 3=\mathrm{V} 4=3.70 \mathrm{~V}$ | 200 | 500 | 1000 | $\mathrm{K} \Omega$ |
| RVMS | Resistance between Vm and VSS | $\mathrm{V} 1=\mathrm{V} 2=\mathrm{V} 3=\mathrm{V} 4=2.20 \mathrm{~V}$ | 200 | 400 | 800 | $\mathrm{K} \Omega$ |
| Down_co | Co from under chip | $\mathrm{V} 1=\mathrm{V} 2=\mathrm{V} 3=\mathrm{V} 4=3.70 \mathrm{~V}$ | 500 | 900 | 2000 | nA |
| Down_do | Do from under chip | $\mathrm{V} 1=\mathrm{V} 2=\mathrm{V} 3=\mathrm{V} 4=3.70 \mathrm{~V}$ | 500 | 900 | 2000 | nA |
| Down_in | Cell balance 2 among chips | $\mathrm{V} 1=\mathrm{V} 2=\mathrm{V} 3=\mathrm{V} 4=3.70 \mathrm{~V}$ | 40 | 80 | 200 | nA |
| Out_down | Cell balance 4 among chips | $\mathrm{V} 1=\mathrm{V} 2=\mathrm{V} 3=\mathrm{V} 4=3.70 \mathrm{~V}$ | 10 | 20 | 30 | $K \Omega$ |
| Up_in | Cell balance 1 among chips | $\mathrm{V} 1=\mathrm{V} 2=\mathrm{V} 3=\mathrm{V} 4=3.70 \mathrm{~V}$ | 40 | 80 | 200 | $n \mathrm{~A}$ |
| Out_up | Cell balance 3 among chips | $\mathrm{V} 1=\mathrm{V} 2=\mathrm{V} 3=\mathrm{V} 4=3.70 \mathrm{~V}$ | 12 | 24 | 36 | $K \Omega$ |
| K_Dp | Spread \& TRIM control | $\mathrm{V} 1=\mathrm{V} 2=\mathrm{V} 3=\mathrm{V} 4=3.70 \mathrm{~V}$ |  | 1.6 | 2 | uA |

1* The Electrical parameters for this temperature range is guaranteed by design, not tested in production.
2* See "Selection Guide" section.
3* VDET1 and VDET2 are the overcharge and over-discharge threshold voltage of actual testing.
4* In the condition of R_Exa=60 K $\Omega$, R_Exs $=80 \mathrm{~K} \Omega, V D E T 3$ and VDET4 are guaranteed by design.
5* Vin is used to detect Excess current 1 by the sense-resistor which connected between B- and P-.

## Function Description

## BM309 Series Power Up Sequence

Fig. 1 shows the BM309 Series' power up sequence. When the power supply is applied to Vcc, the bias and the reference circuit start first, followed by the 3.4 V LDO. Then 8 KHz oscillator works and initializes the digital section. Sampling circuits collect each battery's information and send it out for further processing. Finally BM309 Series can work normally.


## Battery Protection

## 1. Overcharge

During charging, Vdet3<Vm<Vab, when (Va-Vb), (Vb-Vc), (Vc-Vd) or Vd increases to Overcharge Threshold Voltage (Vdet1) or higher and stays longer than Overcharge Delay Time (Tdet1), BM309 Series turn off the charge FET. If, within Tdet1, every cell's voltage becomes lower than Vdet1 and stays shorter than Overcharge Reset Delay Time (Treset) before rising up over Vdet1 again, this type of instantaneous falling of battery voltage will be ignored. Otherwise, the timing related to Tdet1 will be reset.

The overcharge protection state will be released when:
(1) All cells' voltage is less than the Overcharge release threshold Vrel1 and stays for Trel1, or
(2) $\mathrm{Vm}<\mathrm{V}$ det 3 and battery voltage is lower than Vdet 1 .

Make sure $\mathrm{Vm}>\mathrm{V}$ det3 in the overcharge threshold test with a single chip or extended condition, otherwise, abnormal condition will occur.

## 2. Over-discharge

During discharging, V det $3<\mathrm{Vm}<\mathrm{Vab}$, when ( $\mathrm{Va}-\mathrm{Vb}$ ), ( $\mathrm{Vb}-\mathrm{Vc}$ ), ( $\mathrm{Vc} \mathrm{C}-\mathrm{Vd}$ ) or Vd decreases to Over-discharge Threshold Voltage (Vdet2) or lower and stays longer than Over-discharge Delay Time (Tdet2), BM309 Series turn off the discharge FET. Thus, the chip enters sleep mode.
The Over-discharge protection state will be released in the following conditions:
(1) A charger is connected to the battery pack, and the battery supply voltage becomes higher than Vdet2 and stays longer than Trel2, and Vm is higher than the Charger Detection Threshold Voltage (Vcha); or
(2) Every cell's voltage becomes higher than the Over-discharge Release Voltage (Vrel2) and stays longer than Trel2, and Vm is between Vcha and Vdet3.

Make sure $\mathrm{Vm}<\mathrm{V}$ cha in the overcharge threshold test with a single chip or extended condition, otherwise, abnormal condition will occur.

## 3. Excess current

When discharging, the current varies with the load, and Vm decreases with the discharging current increasing. Once Vm drops down to Excess Current 1 Threshold Voltage (Vdet3) or lower and stays longer than the Excess Current 1 Delay Time (Tdet3), Do pad switches to high, turning off the discharge FET. The excess current protection state will be released when Vm $>\mathrm{V}$ det3 and it stays longer than EX \& SC Release Delay (Trex).
When discharging, the current varies with the load, and Vm decreases when the discharging current increases. Once Vm drops down to Excess Current 2 Threshold Voltage (Vdet4) or lower and stays longer than the Excess Current 2 Delay Time (Tdet4), Do pad switches to high, turning off the discharge FET. The excess current protection state will be released when Vm $>$ Vdet3 and it stays longer than EX \& SC Release Delay (Trex). The Excess Current 2 Threshold Voltage (Vdet4) is lower than the Excess Current 1 Threshold Voltage (Vdet3), and the Excess Current 2 Delay Time (Tdet4) is also shorter than the Excess Current 1 Delay Time (Tdet3).

Another way to detect discharge current is placing a small value sense-resistor between Vss and Vin. Vin takes the same priority and delay as Vm in the Excess current 1 state. The Excess Current 1 Threshold Voltage is 0.2 V , and the excess current can be changed by sense-resistor with different values.

## 4. Short circuit

The principle of this function is just the same as the excess current protection. But, the delay time Tshort is much shorter than Tdet3 and Tdet4, and the threshold Vshort is much lower than Vdet3 and Vdet4. When the circuit is shorted, Vm decreases rapidly. Once $\mathrm{Vm}<\mathrm{V}$ short, Do pad switches to high, turning off the discharge FET. The Short circuit release condition is as same as Excess current, the current of short peak value is related to Vshort and discharge/charge FET by Ohm's law.

## 5. Abnormal charge and charger detection

When charging, if charging current exceeds pre-set threshold, $\mathrm{Vm}>$ Vab, charge FET will be turned off after abnormal charge delay Tab. But for battery packs in over-discharge state, abnormal charge detection doesn't work. Instead, if Vm $>$ Vab due to voltage difference between battery and charger, charger detection works to turn on discharge FET as battery voltage goes up to Vdet2, not Vrel2. Abnormal charge state and charger detection is released when the Vm becomes lower than Vab.

## 6. External Bleeding

Cell balance is to balance the cells' capacity in a pack. When the $(\mathrm{Va}-\mathrm{Vb}),(\mathrm{Vb}-\mathrm{Vc}),(\mathrm{Vc}-\mathrm{Vd})$ and Vd all in t of the three ranges $A, B, C$,or at least one of them is in range $D$, cell balance will not work. Otherwise there will be at least one bypass bleeding for cell balance. If four batteries' voltage separate in two of the three ranges $A, B, C$, external bleeding of those who is in range with higher voltage will be switched on. Else if $A, B, C$ areas all have their own distributions, cells in area $A, B$, turn on their cell balance.
When charging, if one of the four cells enters overcharge state, charge FET will be turned off. Bleeding current makes the battery voltage falling down to overcharge release voltage Vrel1, charger detection stops for a while, turning on Co for continuing charging. Thus the voltage of all cells locate will reach to range $A$ just in a cycle .


NOTE: D means over-discharge area.
Vbal2 means cell balance threshold2; Vbal1 means cell balance threshold1.

## Excess current threshold adjustment

Adjustment of excess current threshold is available by external resistors R_Exa and R_Exs. Different values have their corresponding excess current threshold, R_Exs=80K. Small resistance can acquire high accuracy of excess current threshold at the price of power dissipation. Large resistance can reduce power dissipation, but the accuracy is not ideal.

| Preset value |  | Real value |  |  |
| :---: | :---: | :---: | :---: | :---: |
| Vcc-Vdet3 | Vcc-Vdet4 | R_Exa (ohms) | Vcc-Vdet3 | accuracy |
| 0.10 V | 0.30 V | 30 K | 0.102 V | $\pm 15 \%$ |
| 0.15 V | 0.45 V | 45 K | 0.151 V | $\pm 15 \%$ |
| 0.20 V | 0.60 V | 60 K | 0.200 V | $\pm 15 \%$ |


| 0.25 V | 0.75 V | 75 K | 0.247 V | $\pm 15 \%$ |
| :---: | :---: | :---: | :---: | :---: |
| 0.30 V | 0.90 V | 90 K | 0.294 V | $\pm 15 \%$ |
| 0.35 V | 1.05 V | 105 K | 0.340 V | $\pm 15 \%$ |
| 0.40 V | 0.20 V | 120 K | 0.385 V | $\pm 15 \%$ |
| 0.45 V | 1.35 V | 135 K | 0.430 V | $\pm 15 \%$ |
| 0.50 V | 1.80 V | 150 K | 0.475 V | $\pm 15 \%$ |

The Excess current 1 threshold calculate: Vdet $3 \approx$ Vcc- $\frac{0.8}{3} \times \frac{\text { R_Exa }}{\text { R_Exs }}$, Vdet $4=$ Vcc-3(Vcc-Vdet 3 )

## Power MOSFET Drive Control

In BM309 Series application circuit, two P-MOSFETs control on/off of charge and discharge current. Do and Co are CMOS outputs. BM309 Series utilize several buffers to level up the output drive capacity.
Two P-MOSFETs in series is only one pattern of the control of charge and discharge loops. BM309 Series also support different charge and discharge loops.

## Auto-fit between 3/4 cell

BM309 Series can be used in either a three-cell or a four-cell pack. In a three-cell pack's application, the Vc must be shorted to Vd. Built-in circuits can distinguish this condition from four-cell application.

## Extended Application

As mentioned above, BM309 Series provide an easy way for extended application in more-cell-packs' protection.by additional module..
When used in extended condition, each IC transfers Do and Co information upward. For example as 8 -cell, the information from Co and Do of the nether one will be transferred to Down_co and Down_do, then the upper one will get this information.By analogy the top IC collects all ICs' information and sends proper instructions to final Co and Do, controlling external MOSFETs. Once one of the ICs enters abnormal state, the whole system enters abnormal state, the protection is performed. Apparently, the top IC differes from the others. Pin K_DP is used to distinguish them. When K_DP is " 0 ", outputs of the corresponding IC's Do and Co are " 0 " and " X " (high resistance), when K_Dp is floating, the outputs of the corresponding IC's Do and Co are CMOS level.
Cell balance function goes on working in extended condition. To assure cell balance between ICs, BM309 Series use Down_in, Up_in, Out_down, Out_up to transfer each IC's balance information upward and downward. Each IC will get other ICs' balance information and choose whether to open its balance function or not. The upward and downward transmission of balance information forms a loop.
The sleep mode is unavailable in extended condition. After over-discharge protection occurs, discharge FET will turn off but control circuits won't enter sleep mode.
A steady current source are embedded in K_Dp, the output is 1.6 uA .
A steady current source are embedded in Down_do, Down_co, the output is 0.8 uA .
A steady current source are embedded in Down_in, Up_in, the output is 80 nA.
Out_down pin is Nch open-drain output, the output resistance is 20 K .
Out_up pin is Pch open-drain output, the output resistance is 24 K .

## Operation Timing Charts

Overcharge/Over-discharge
Detection



(1) Charger connected
(2) Overcharge Detection Delay Time (Tdet1)
(3) Load connected
(4) Over-discharge Detection Delay Time (Tdet2)
(5) Normal charging

## Excess Current and Short Protection





(1) Normal condition
(2) Load connection
(3) Excess Current 1 Delay Time (Tdet3)
(4) Excess Current 2 Delay Time (Tdet4)

## Test Circuits

1. Normal and standby current consumption

## Test circuit 1

(1) Set $\mathrm{V} 1=\mathrm{V} 2=\mathrm{V} 3=\mathrm{V} 4=3.70 \mathrm{~V}, \mathrm{~K} 1$ on, the current flowing to Vss is the normal operating current consumption.
(2) Set $\mathrm{V} 1=\mathrm{V} 2=\mathrm{V} 3=\mathrm{V} 4=3.70 \mathrm{~V}, \mathrm{~K} 1$ on, then set $\mathrm{V} 1=\mathrm{V} 2=\mathrm{V} 3=\mathrm{V} 4=2.20 \mathrm{~V}$, K 1 off, the current flowing to Vss is the standby current consumption.
2. Overcharge threshold (Vdet1) and Overcharge release threshold (Vrel1) Test circuit 2
Set $\mathrm{V} 1=\mathrm{V} 2=\mathrm{V} 3=\mathrm{V} 4=3.70 \mathrm{~V}$, make sure Do and Co are " L ". Increase V 1 gradually, monitor Co voltage and keep the condition not shorter than Tdet1, the V 1 , when Co turns from " L " to " H ", is the overcharge threshold voltage. Decrease V 1 , the V 1 , when Co returns to " L " again, is the overcharge release threshold.
3. Over-discharge threshold (Vdet2) and Over-discharge release threshold (Vrel2) Test circuit 2
Set $\mathrm{V} 1=\mathrm{V} 2=\mathrm{V} 3=\mathrm{V} 4=3.70 \mathrm{~V}$, make sure Do and Co are " L ". Decrease V 1 gradually, monitor Do voltage and keep the condition not shorter than Tdet2, the V 1 , when Do turns from " L " to " H ", is the over-discharge threshold voltage. Increase V 1 , the V 1 when Do returns to "L" again, is the over-discharge release threshold.
4. Balance threshold (Vbal1, Vbal2)

Test circuit 4
(1) Set $\mathrm{V} 1=\mathrm{V} 2=\mathrm{V} 3=\mathrm{V} 4=3.70 \mathrm{~V}$, make sure Bal4 is 0 V and Bal3 is 3.70 V . Increase V 4 gradually, monitor Bal4 voltage, when Bal4 turns from 0 V to V 4 , the value of V 4 is the balance threshold voltage (Vbal1).
(2) Set $\mathrm{V} 1=\mathrm{V} 2=\mathrm{V} 3=\mathrm{V} 4=3.70 \mathrm{~V}$, make sure Bal 4 is 0 V and Bal 3 is 3.70 V . Decrease V 4 gradually, monitor Bal3 voltage, when Bal3 turns from V 4 to $\mathrm{V} 4+3.70 \mathrm{~V}$, the value of V 4 is the balance threshold voltage (Vbal2).

## 5. Excess current threshold (Vin, Vdet3, Vdet4) ,short circuit threshold (Vshort)

 Test circuit 3(1) Set $\mathrm{V} 1=\mathrm{V} 2=\mathrm{V} 3=\mathrm{V} 4=3.70 \mathrm{~V}, \mathrm{~V} 5=14.80 \mathrm{~V}, \mathrm{~V} 6=0 \mathrm{~V}, \mathrm{KI}, \mathrm{K} 2$ on, $\mathrm{R} \_\mathrm{Exa}=60 \mathrm{~K} \Omega$, R_Exs $=80 \mathrm{~K} \Omega$, make sure Do and Co are "L". Decrease V5 gradually, monitor Do voltage and keep the condition for some time, the V5, when Do turns from "L" to " H ", is the excess current 1 threshold (Vdet3). Increase V5, the excess current 1 will be released. Vdet4 and Vshort can also be tested, but V5 has a larger change.
(2) Set $\mathrm{V} 1=\mathrm{V} 2=\mathrm{V} 3=\mathrm{V} 4=3.70 \mathrm{~V}, \mathrm{~V} 5=14.80 \mathrm{~V}, \mathrm{~V} 6=0 \mathrm{~V}, \mathrm{KI}$, K 2 off, make sure Do and Co are " L ". Increase V 6 gradually, monitor Do voltage and keep the condition for some time, the V6, when Do turns from " L " to " H ", is discharge current detection threshold.
6. Charger detection threshold (Vcha) and abnormal charge threshold (Vab) Test circuit 3
(1) Set $\mathrm{V} 1=\mathrm{V} 2=\mathrm{V} 3=3.70 \mathrm{~V}, \mathrm{~V} 4=2.20, \mathrm{~V} 5=13.30 \mathrm{~V}, \mathrm{~V} 6=0 \mathrm{~V}, \mathrm{KI}, \mathrm{K} 2$ off, BM 309 Series enter the over-discharge condition. Increase V4 gradually until it is between Vdet2 and Vrel2. Increase V5 gradually, the V5, when Do changes from " H " to "L", is the Charger Detection threshold (Vcha).
(2) Set $\mathrm{V} 1=\mathrm{V} 2=\mathrm{V} 3=\mathrm{V} 4=3.70 \mathrm{~V}, \mathrm{~V} 5=14.80 \mathrm{~V}, \mathrm{~V} 6=0 \mathrm{~V}, \mathrm{KI}, \mathrm{K} 2$ off, make sure Do and Co are " L ", increase V 5 , the V 5 , when Co changes from "L" to "H", is the abnormal charge threshold (Vab).

## 7. Delay parameters

## (1) Overcharge detection delay(Tdet1)

## Test circuit 2

Set $\mathrm{V} 1=\mathrm{V} 2=\mathrm{V} 3=\mathrm{V} 4=3.70 \mathrm{~V}$, make sure Do and Co are "L". Increase V 1 transiently to 4.40 V , monitor Co voltage, and
keep the condition for some time. If Co changes to " H ", the "some time" is the overcharge detection delay (Tdet1).

## (2) Over-discharge detection delay(Tdet2)

## Test circuit 2

Set $\mathrm{V} 1=\mathrm{V} 2=\mathrm{V} 3=\mathrm{V} 4=3.70 \mathrm{~V}$, make sure Do and Co are " L ", decrease V 1 transiently to 2.20 V , monitor Do voltage, and keep the condition for some time. If Do changes to " H ", the "some time" is the over-discharge detection delay (Tdet2).

## (3) Excess current detection delay(Tdet3,Tdet4)

## Test circuit 3

Set $\mathrm{V} 1=\mathrm{V} 2=\mathrm{V} 3=\mathrm{V} 4=3.70 \mathrm{~V}, \mathrm{~V} 5=14.80 \mathrm{~V}, \mathrm{KI}$, K 2 on, make sure Do and Co are " L ", decrease V 5 transiently to14V, monitor Do voltage, and keep the condition for some time. If Do changes to " H ", the "some time" is the excess current 1 detection delay (Tdet3). Increase V5, the excess current 1 will be released. Excess current 2 detection delay (Tdet4) can be tested using the same method. But V5 should decrease more and the delay is shorter.

## 8. Output/Input resistor drive capacity

### 8.1 Co, Do output resistor

## Test Circuit 5

(1) Set $\mathrm{V} 1=\mathrm{V} 2=\mathrm{V} 3=\mathrm{V} 4=3.70 \mathrm{~V}, \mathrm{~V} 5=0 \mathrm{~V}, \mathrm{~V} 6=0 \mathrm{~V}, \mathrm{~K} 1$ on, increase V 6 from 0 V gradually, the V 6 voltage, when $\mathrm{A} 2=50 \mathrm{uA}$, is the CO 'L' voltage.
(2) Set $\mathrm{V} 1=\mathrm{V} 2=\mathrm{V} 3=\mathrm{V} 4=4.40 \mathrm{~V}, \mathrm{~V} 5=0 \mathrm{~V}, \mathrm{~V} 6=17.60 \mathrm{~V}, \mathrm{~K} 1$ on, decrease V 6 from 17.60 V gradually, the V 6 voltage, when A2 $=-50 u A$, is the CO ' H ' voltage.
(3) Set $\mathrm{V} 1=\mathrm{V} 2=\mathrm{V} 3=\mathrm{V} 4=3.70 \mathrm{~V}, \mathrm{~V} 5=0 \mathrm{~V}, \mathrm{~V} 6=0 \mathrm{~V}, \mathrm{~K} 2$ on, increase V 5 from 0 V gradually, the V 5 voltage, when $\mathrm{A} 1=50 \mathrm{uA}$, is the DO 'L' voltage
(4) Set $\mathrm{V} 1=\mathrm{V} 2=\mathrm{V} 3=\mathrm{V} 4=2.20 \mathrm{~V}, \mathrm{~V} 5=0 \mathrm{~V}, \mathrm{~V} 6=8.80 \mathrm{~V}$, and K 2 on, decrease V 5 from 8.80 V gradually, the V 5 voltage, when A2 =-50uA, is the DO 'H' voltage.

### 8.2 Vm resistance <br> Test Circuit 6

Test beginning condition: Set $\mathrm{V} 1=\mathrm{V} 2=\mathrm{V} 3=\mathrm{V} 4=3.70 \mathrm{~V}, \mathrm{~V} 5=14.80 \mathrm{~V}$, make sure Do and Co are " L ",
(1) Set $\mathrm{V} 1=\mathrm{V} 2=\mathrm{V} 3=\mathrm{V} 4=3.70 \mathrm{~V}, \mathrm{~V} 5=12.10 \mathrm{~V}$, the $(14.80-\mathrm{V} 5) / / 5$ is the internal resistance RVMC which between VCC and $V \mathrm{~m}$.
(2) Set $\mathrm{V} 1=\mathrm{V} 2=\mathrm{V} 3=\mathrm{V} 4=2.20 \mathrm{~V}, \mathrm{~V} 5=3.70 \mathrm{~V}$, the $\mathrm{V} 5 / / 5$ is the internal resistance RVMS which between Vm and Vss .

### 8.3 Bleed1, Bleed2, Bleed3, Bleed4 resistance

## Test Circuit 7

(1) Set $\mathrm{V} 1=4.20$, $\mathrm{V} 2=\mathrm{V} 3=\mathrm{V} 4=3.70 \mathrm{~V}, \mathrm{~V} 5=15.30 \mathrm{~V}, \mathrm{~K} 1$ on, $\mathrm{K} 2, \mathrm{~K} 3$, K 4 off, decrease V 5 gradually from 15.30 V , the V 5 , when $\mathrm{A}=-50 \mathrm{uA}$, is the Bal1 ' H ' voltage.
(2) Set $\mathrm{V} 1=\mathrm{V} 2=\mathrm{V} 3=\mathrm{V} 4=3.70 \mathrm{~V}, \mathrm{~V} 5=11.10 \mathrm{~V}, \mathrm{~K} 1$ on, $\mathrm{K} 2, \mathrm{~K} 3, \mathrm{~K} 4$ off, increase V 5 gradually from 11.10 V , the V 5 , when $A=-50 u A$, is the Bal1 'L' voltage.
(3) Set $\mathrm{V} 2=4.20 \mathrm{~V}, \mathrm{~V} 1=\mathrm{V} 3=\mathrm{V} 4=3.70 \mathrm{~V}, \mathrm{~V} 5=11.60 \mathrm{~V}, \mathrm{~K} 2$ on, $\mathrm{K} 1, \mathrm{~K} 3$, K 4 off, decrease V 5 gradually from 11.60 V , the V 5 , when $\mathrm{A}=-50 \mathrm{uA}$, is the $\mathrm{Bal2}$ ' H ' voltage.
(4) Set $\mathrm{V} 1=\mathrm{V} 2=\mathrm{V} 3=\mathrm{V} 4=3.70 \mathrm{~V}, \mathrm{~V} 5=7.40 \mathrm{~V}$, K 2 on, $\mathrm{K} 1, \mathrm{~K} 3$, K 4 off, increase V 5 gradually from 7.40 V , the V 5 , when $A=50 \mathrm{uA}$, is the Bal 2 ' L ' voltage.
(5) Set $\mathrm{V} 3=4.20 \mathrm{~V}, \mathrm{~V} 1=\mathrm{V} 2=\mathrm{V} 4=3.70 \mathrm{~V}, \mathrm{~V} 5=7.90 \mathrm{~V}$, K 3 on, $\mathrm{K} 1, \mathrm{~K} 2$, K 4 off, decrease V 5 gradually from 7.90 V , the V 5 , when $\mathrm{A}=-50 \mathrm{uA}$, is the Bal3 ' H ' voltage.
(6) Set $\mathrm{V} 1=\mathrm{V} 2=\mathrm{V} 3=\mathrm{V} 4=3.70 \mathrm{~V}, \mathrm{~V} 5=3.70 \mathrm{~V}$, K 3 on, K 1 , K 2 , K 4 off, increase V 5 gradually from 3.70 V , the V 5 , when $A=50 u A$, is the Bal3 'L' voltage.
(7) Set $\mathrm{V} 4=4.20 \mathrm{~V}, \mathrm{~V} 1=\mathrm{V} 2=\mathrm{V} 3=3.70 \mathrm{~V}, \mathrm{~V} 5=4.20 \mathrm{~V}, \mathrm{~K} 4$ on, $\mathrm{K} 1, \mathrm{~K} 2, \mathrm{~K} 3$ off, decrease V 5 gradually from 4.20 V , the V 5 ,
when $\mathrm{A}=-50 \mathrm{uA}$, is the $\mathrm{Bal4}$ ' H ' voltage.
(8) Set $\mathrm{V} 1=\mathrm{V} 2=\mathrm{V} 3=\mathrm{V} 4=3.70 \mathrm{~V}, \mathrm{~V} 5=0 \mathrm{~V}, \mathrm{~K} 4$ on, $\mathrm{K} 1, \mathrm{~K} 2, \mathrm{~K} 3$ off, increase V 5 gradually from 0 V , the V 5 , when $\mathrm{A}=50 \mathrm{uA}$, is the Bal4 'L' voltage.

### 8.4 The output pin with extended application

## Test circuit 8

(1) Set $\mathrm{V} 1=\mathrm{V} 2=\mathrm{V} 3=\mathrm{V} 4=3.70 \mathrm{~V}, \mathrm{~V} 5=1.00 \mathrm{~V}, \mathrm{~K} 1$ on, $\mathrm{K} 2, \mathrm{~K} 3, \mathrm{~K} 4, \mathrm{~K} 5, \mathrm{~K} 6, \mathrm{~K} 7$ off, the reading of A 1 is the output of $\mathrm{K} \_\mathrm{Dp}$.
(2) Set $\mathrm{V} 1=\mathrm{V} 2=\mathrm{V} 3=\mathrm{V} 4=3.70 \mathrm{~V}, \mathrm{~V} 7=1.00 \mathrm{~V}, \mathrm{~K} 4$ on, $\mathrm{K} 1, \mathrm{~K} 2, \mathrm{~K} 3, \mathrm{~K} 5, \mathrm{~K} 6, \mathrm{~K} 7$ off, the reading of A 2 is the output of Up_in.
(3) Set $\mathrm{V} 1=\mathrm{V} 2=\mathrm{V} 3=\mathrm{V} 4=3.70 \mathrm{~V}, \mathrm{~V} 7=1.00 \mathrm{~V}, \mathrm{~K} 5$ on, $\mathrm{K} 1, \mathrm{~K} 2, \mathrm{~K} 3, \mathrm{~K} 4, \mathrm{~K} 6, \mathrm{~K} 7$ off, the reading of A 2 is the output of Down_in.
(4) Set $\mathrm{V} 1=\mathrm{V} 2=\mathrm{V} 3=\mathrm{V} 4=3.70 \mathrm{~V}, \mathrm{~V} 7=1.00 \mathrm{~V}, \mathrm{~K} 6$ on, $\mathrm{K} 1, \mathrm{~K} 2, \mathrm{~K} 3, \mathrm{~K} 4, \mathrm{~K} 5, \mathrm{~K} 7$ off, the reading of A 2 is the output of Down_co.
(5) Set $\mathrm{V} 1=\mathrm{V} 2=\mathrm{V} 3=\mathrm{V} 4=3.70 \mathrm{~V}, \mathrm{~V} 7=1.00 \mathrm{~V}, \mathrm{~K} 7$ on, $\mathrm{K} 1, \mathrm{~K} 2, \mathrm{~K} 3, \mathrm{~K} 4, \mathrm{~K} 5, \mathrm{~K} 6$ off, the reading of A 2 is the output of Down_do.
(6) Set $\mathrm{V} 1=\mathrm{V} 2=\mathrm{V} 3=\mathrm{V} 4=3.70 \mathrm{~V}, \mathrm{~V} 6=0 \mathrm{~V}, \mathrm{~K} 2$ on, $\mathrm{K} 1, \mathrm{~K} 3, \mathrm{~K} 4, \mathrm{~K} 5, \mathrm{~K} 6, \mathrm{~K} 7$ off, increase V 6 gradually from 0 V , the V 6 , when the reading of A 3 is 50 uA , is the output of Out_up.
(7) Set $\mathrm{V} 1=\mathrm{V} 2=\mathrm{V} 3=\mathrm{V} 4=3.70 \mathrm{~V}, \mathrm{~V} 6=3.40 \mathrm{~V}, \mathrm{~K} 3$ on, $\mathrm{K} 1, \mathrm{~K} 2, \mathrm{~K} 4, \mathrm{~K} 5$, $\mathrm{K} 6, \mathrm{~K} 7$ off, decrease V 6 gradually from 3.40 V , the V 6 , when the reading of A 3 is -50 uA , is the output of Out_down.





## Package Information

- Package: TSSOP24


| Symbol | Dimensions In Millimeters |  | Dimensions In Inches |  |
| :---: | :---: | :---: | :---: | :---: |
|  | Min | Max | Min | Max |
| D | 7.700 | 7. 900 | 0. 303 | 0. 311 |
| E | 4. 300 | 4. 500 | 0. 169 | 0. 177 |
| b | 0.190 | 0. 300 | 0.007 | 0.012 |
| c | 0. 090 | 0. 200 | 0. 004 | 0.008 |
| E1 | 6. 250 | 6.550 | 0. 246 | 0. 258 |
| A |  | 1. 100 |  | 0.043 |
| A2 | 0.800 | 1. 000 | 0.031 | 0.039 |
| A1 | 0.020 | 0. 150 | 0. 001 | 0. 006 |
| e | 0.65 (BSC) |  | 0.026 (BSC) |  |
| L | 0.500 | 0.700 | 0.02 | 0.028 |
| H | 0.25 (T YP) |  | 0.01 (TYP) |  |
| $\theta$ | $1^{\circ}$ | $7^{\circ}$ | $1^{\circ}$ | $7^{\circ}$ |

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