DESCRIPTION

The SS1203 is a current mode PWM switching power supply controller that specifically designed for AC/DC converter with high performance versus cost ratio. It provides continuous output power up to 12W in the broad voltage range of 85V – 265V.Its optimized and highly reasonable circuit design has made it possible to minimize the total cost of the product. This power supply controller could be used in typical flyback circuit topology to constitute simple AC/DC converter. The internal initiating circuit of SS1203 has been designed with a unique means of current sink to complete the startup using the amplifying function of the power switching tube. This will significantly reduce the power consumption of the start-up resistor; and when the output power becomes smaller, SS1203 will automatically lower its operating frequency to enable very low standby power consumption.

When the power tube stops, the internal circuit will turn the power tube reverse bias to greatly raise the voltage resistant capacity of OC pin. This will ensure the safety of the power tube. The internal design of the SS1203 is also provided with over-load and saturation preventive function capable of preventing disorders such as overload, transformer saturation and output short-circuit, so as to increase the reliability of the power supply. A voltage reference of 2.5V is also integrated in the SS1203 to provide accurate power supply to the clock circuit, and the clock frequency may be set by external timing capacitance. Presently, standard DIP8 package and environmental friendly lead-free package in compliance with European standard can be supplied.

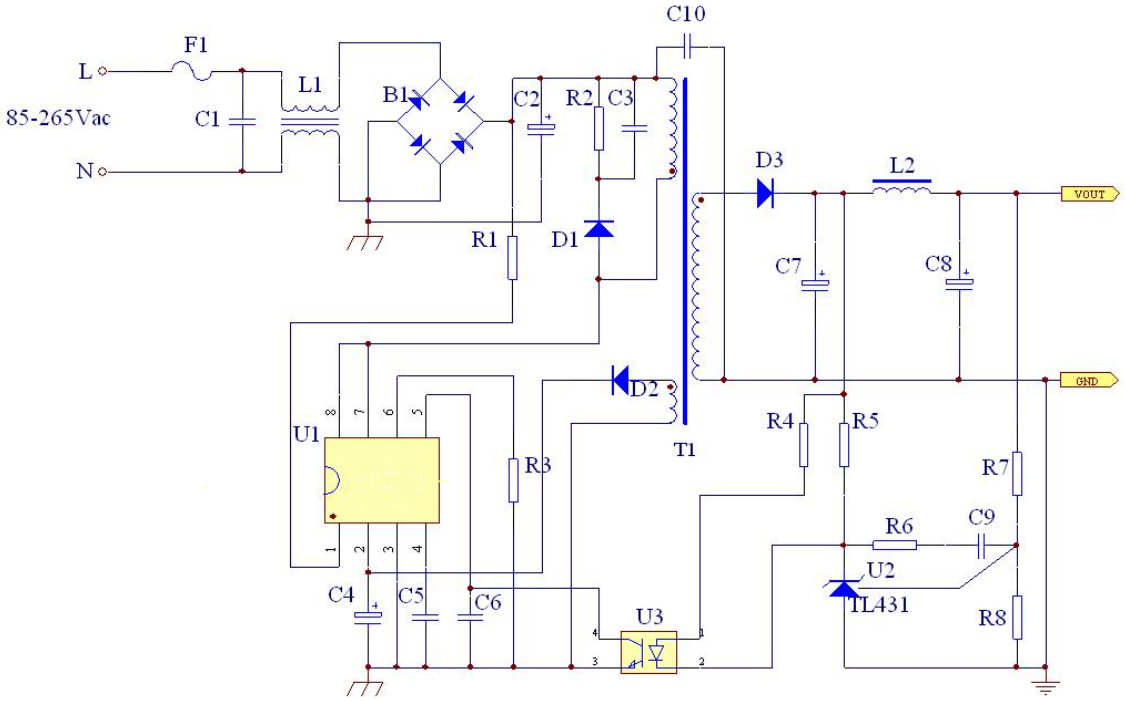
FEATURES

- Built-in 700V high voltage power switching tube with minimal external parts count
- Latched PWM and pulse-by-pulse current limiting inspection
- Reduced frequency at low output with standby power consumption below 0.25W
- Built-in slope and feedback compensation function
- Separate upper limit current inspection controller to handle timely the over-current and overload of the controller
- Turn off periodic bias output of the emitter to improve the voltage resistance of the power tube
- Built-in thermal protective circuit
- Complete start-up using amplification of the switching power tube to reduce the power consumption of the start-up resistor more than ten times
- Automatic VCC over-voltage limit
- Broad voltage output power up to 5W and narrow voltage output power up to 8W

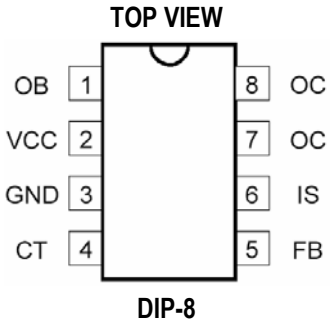
Applications

- Power Adaptors(traveling chargers ,stand-alone power set)
- Internal power supply for Energy-Saving Appliances (such as electromagnetic oven, microwave oven and etc.)

TYPICAL APPLICATION



PACKAGE INFORMATION



PIN FUNCTIONS

Pin	Symbol	Function Description
1	OB	Base Pin of the Power Tube.(Enabling current input and connect to initiating resistance)
2	VCC	Power Supply Pin
3	GND	Ground Pin
4	CT	Oscillation Capacitance Pin.(Connect to timing capacitance)
5	FB	Feedback Pin
6	IS	Current Inspection Pin
7、8	OC	Output Pin(Connect to switching transformer)

ABSOLUTE MAXIMUM RATINGS(Note 1)

Supply Voltage VCC..... 18V
OC Voltage..... -0.3-700V
Total Dissipation Power..... 1000mW
Storage Temperature Range..... -40 - 150℃
Pin Input Voltage..... VCC+0.3V
Switching Current..... 800mA
Operating Temperature Range..... 0-75℃
Welding Temperature..... +260℃，10S

ELECTRICAL CHARACTERISTICS

The specifications are applied at T=25℃, VCC=5.5-7.5V, Ct=680PF, RS=1Ω, unless otherwise noted.(Note 2)

Parameter		Symbol	Conditions	Min	Typ	Max	Units
Output Section							
Max. Withstanding Voltage of the Switching Tube			I_{OC}=10mA	700			V
Saturation Voltage		V_{SAT}	Ioc=250mA			1	V
Output Rise Time		T_R	CL=1nF			75	ns
Output Fall Time		T_F	CL=1nF			75	ns
Output Limiting Current			Tj=0-100℃	250	270	290	mA
Reference Section							
Reference Output Voltage		V_{REF}	Io=1.0mA	2.4	2.5	2.6	V
Line Regulation			Vcc=5.5-9V		2	20	mV
Load Regulation			Io=0.1-1.2mA			3	%
Temperature Stability					0.2		mV/℃
Output Noise Voltage			F=10Hz-10KHz			50	uV
Long Term Stability			1000 hours@85℃		5		mV
Oscillator Section							
Oscillating Frequency		F_{OSC}	Ct=680PF	55	61	67	KHz
Voltage Stability			Vcc=5.5-9V			1	%
Temperature Stability			Ta=0-85℃			1	%
Oscillator Amplitude (Vp - p)					2.2		V
Feedback Section							
Input Impedance	Pull-up Current		FB=2.5V, IS=0V	0.55	0.6	0.65	mA
	Pull-Down Resistor				30		KΩ
Power Supply Suppression Ratio			Vcc=5.5-9V		60	70	dB
Current Sampling Section							
Current Sampling Threshold		V_{CS}		0.55	0.60	0.65	V
Anti-Upper Limit Current		I_L		0.25	0.27	0.29	A
Power Supply Suppression Ratio					60	70	dB
PWM Section							
Maximum Duty Ratio		D_{MAX}		53	57	61	%
Minimum Duty Ratio		D_{MIN}				3.5	%
Power Supply Current Section							
Initiating Reception Current				1.6	2.4	3.2	mA
Initiating Static Current					55	80	uA
Static Current		I_Q	Vcc=8V		2.8		mA
Start-up voltage				8.6	8.8	9.0	V
Oscillator Turn-off Voltage				4.4	4.6	4.8	V

ELECTRICAL CHARACTERISTICS

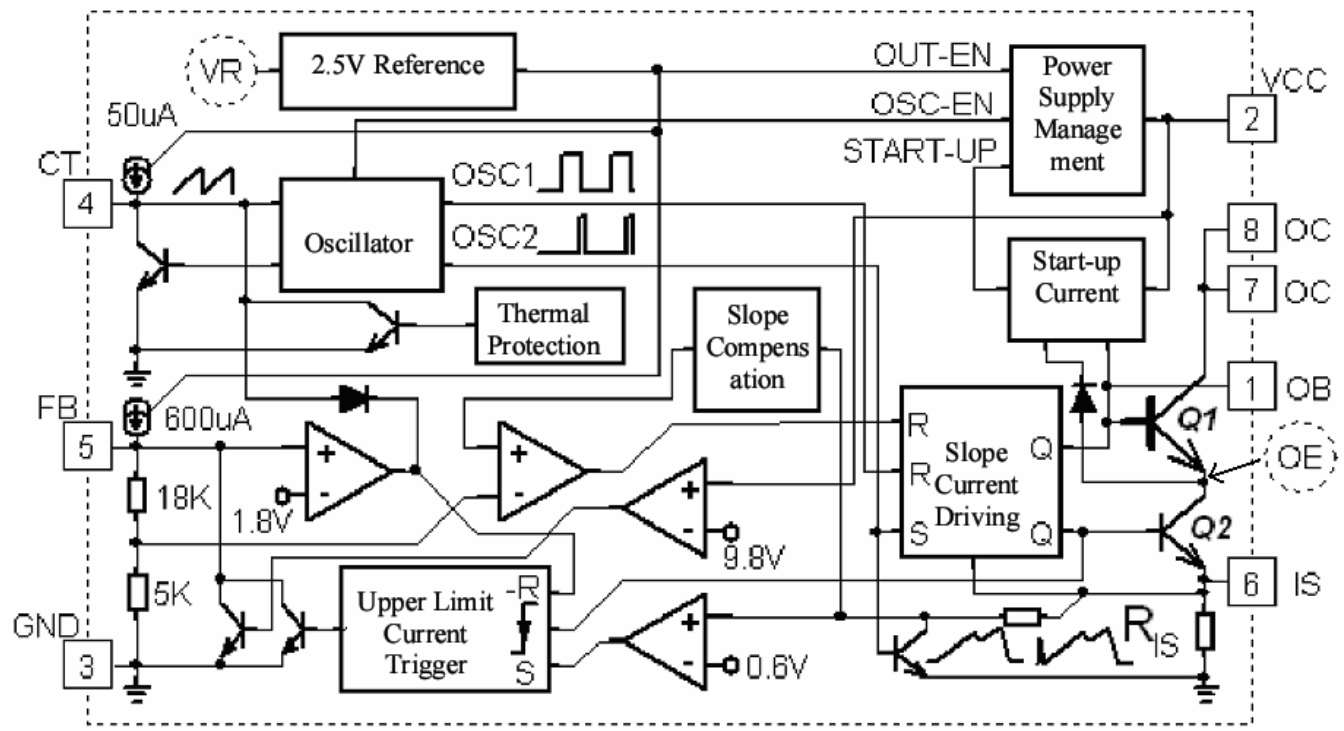
The specifications are applied at T=25℃, VCC=5.5-7.5V, Ct=680PF, RS=1Ω, unless otherwise noted.(Note 2)(continued)

Re-enabling voltage				4.2		V
Over-Voltage Limiting Threshold			9.2	9.6	10	V

Note1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note2: TheSS1203 is guaranteed to meet performance specifications from 0℃ to 70℃. Specifications over the -40℃ to 85℃ operating temperature range are assured by design, characterization and correlation with statistical process controls.

BLOCK DIAGRAM



OPERATION (Refer to Block Diagram)

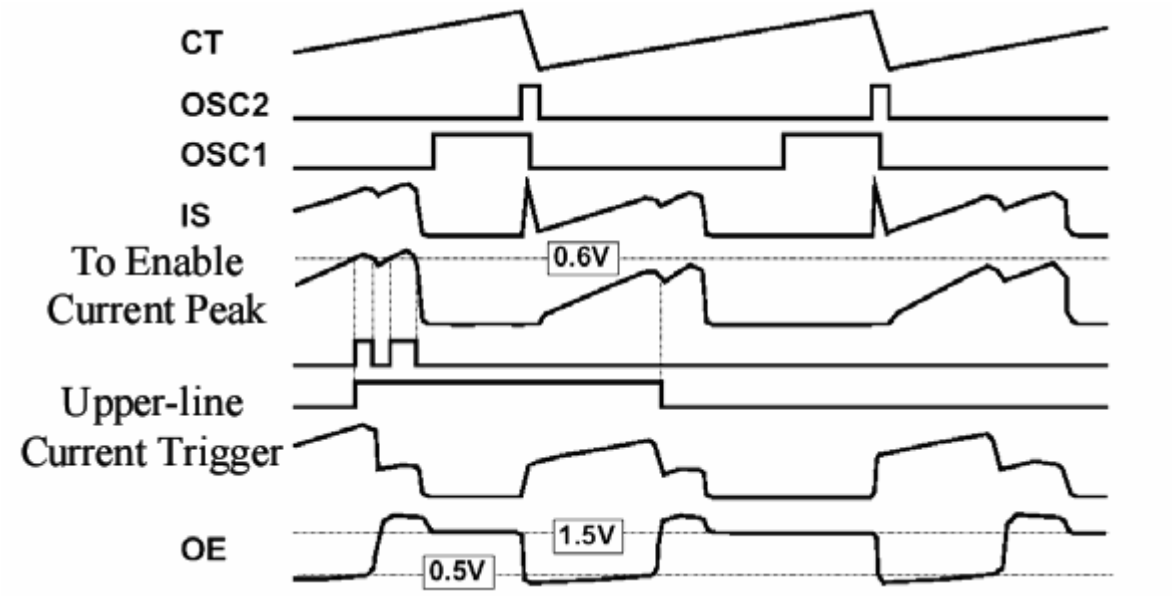
In the enabling stage, when power is on, VR is closed; the pull-up current source FB is closed; OE inputs enabling current from power tube to VCC; OB controls the base current of the power tube, limits the collector current of the power tube (i.e. SS1203 initiates the reception current), so as to ensure the safety of the power tube; when VCC voltage raises up to 7.8 V, the enabling stage ends and it goes into the normal stage.

In the normal stage, VCC voltage should be maintained at 4.8V to 9.0V, VR outputs 2.5V reference; FB pull-up current source is opened; the oscillator output OSC1 decides the maximum duty ratio, output OSC2 tries to trigger the power into open period, and the screened power tube turns on the current peak; if FB is below 1.8V (approximately between 1.2V and 1.8V), the oscillator period will then be increased, the smaller the FB is, the wider the oscillator period will be, until the stop of the oscillator (this feature will lower the stand-by power consumption of the switch power source); if the external feedback intends to make VCC higher than 10V, the internal circuit feedback to FB will stabilize VCC at 9.8V (with this feature, the internal circuit rather than the external feedback circuit will be used to stabilize the output voltage, but the stabilizing accuracy may be low); in the open period, OB supplies base current to power tube, OE pulls down the emitter of the power tube to IS, and the OB uses the slope current driving (i.e. the OB open current is the function of IS, when IS = 0V, OB open current is approximately 40mA, then the OB

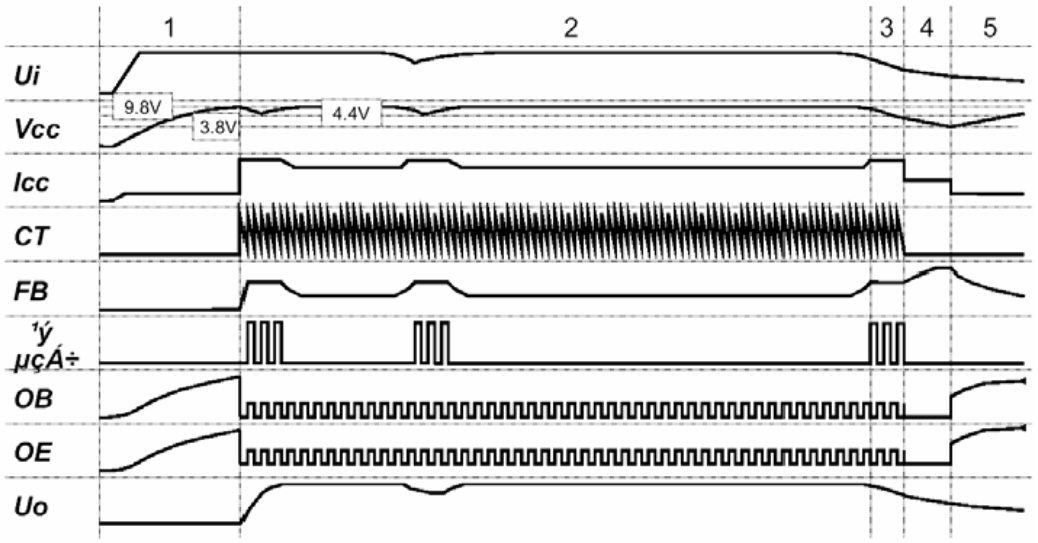
open current will increase along with IS linearly, when IS raises to 0.6V, the OB open current is approximately 100mA, this feature will effectively utilize the output current of OB and lower the power consumption of SS1203), if IS detects the specified current of FB, it goes into close period; in the close period, OB pulls down, the power tube may not be turned off immediately, but OE clamps on 2.0V (after the power tube turns off, the base will be reverse bias and the voltage withstanding capacity is increased); in the open or close period, if it detects the current exceeding upper limit of the power tube, then the upper limit flip-flop will be put at the preferential position, forcing FB to decrease and the duty ratio will turn smaller, so that the power tube and transformer will be protected; at the beginning of next close period edge or if FB is below 1.8V, the upper limit flip-flop will reset. Besides, the built-in heat protection of SS1203 will widen the oscillator period when the internal temperature is above 125℃ to ensure the temperature of SS1203 will not exceed 135℃; the built-in slope compensation will stabilize the open/close period when SS1203 is at high duty ratio or in continuous current mode.

When VCC lowers to about 4.4V, the oscillator will be closed, OSC1 and OSC2 will be at low level, and the power source will be maintained at close period; when VCC goes on lowering to about 3.8V, SS1203 will enter the enabling stage again.

Normal Stage Switching Cycle Oscillogram



Global Oscillogram



Coponnt Slct Inoation

Step-1、Determine DC link capacitor (C_{DC}) and the DC link voltage range.

It is typical to select the DC link capacitor as 2-3uF per watt of input power for universal input range (85-265Vrms) and 1uF per watt of input power for European input range (195V-265Vrms). With the DC link capacitor chosen, the minimum link voltage is obtained as

$$V_{DC}^{MIN} = \sqrt{2\left(V_{line}^{\min}\right)^2 - \frac{P_{IN} \times (1 - D_{ch})}{C_{DC} \times f_L}}$$

where Dch is the DC link capacitor charging duty ratio which is typically about 0.2 and f_L is Line frequency.

The maximum DC link voltage is given as

$$V_{DC}^{MAX} = \sqrt{2} \times V_{line}^{MAX}$$

Where $V_{line}^{\min}$ and $V_{line}^{\max}$ Line voltage range.

Step-2、Determine the transformer primary side inductance (L_m).

The operation changes between CCM and DCM as the load condition and input voltage vary. For both operation modes, the worst case in designing the inductance of the transformer primary side (Lm) is full load and minimum input voltage condition. Therefore, Lm is obtained in this condition as

$$L_m = \frac{(V_{DC}^{MIN} \times D_{MAX})^2}{2 \times P_{IN} \times f_s \times K_{RF}}$$

where f_s is the switching frequency and K_{RF} is the ripple factor in full load and minimum input voltage condition, For DCM operation, K_{RF} = 1 and for CCM operation K_{RF} < 1. The ripple factor is closely related with the transformer size and the RMS value of the MOSFET current. Even though the conduction loss in the MOSFET can be reduced through reducing the ripple factor, too small a ripple factor forces an increase in transformer size. When designing the flyback converter to operate in CCM, it is reasonable to set K_{RF} = 0.25-0.5 for the universal input range and K_{RF} = 0.4-0.8 for the European input range.

Once L_m is determined, the maximum peak current and RMS current of the MOSFET in normal operation are obtained as

$$I_{ds}^{peak} = I_{DEC} + \frac{\Delta I}{2}$$

$$I_{ds}^{rms} = \sqrt{\left[3\left(I_{DEC}\right)^2 + \left(\frac{\Delta I}{2}\right)^2\right] \times \frac{D_{\max}}{3}}$$

Where

$$I_{DEC} = \frac{P_{in}}{V_{DC}^{\min} \times D_{MAX}}$$

$$\Delta I = \frac{V_{DC}^{\min} \times D_{MAX}}{L_m \times f_s}$$

The flyback converter designed for CCM at the minimum input voltage and full load condition may enter into DCM as the input voltage increases. The maximum input voltage guaranteeing CCM in the full load condition is obtained as

$$V_{DC}^{CCM} = \left(\frac{1}{\sqrt{2L_m \times f_s \times P_{in}}} - \frac{1}{V_{RO}}\right)^{-1}$$

If the result of above equation has a negative value, the converter is always in CCM under the full load condition regardless of the input voltage variation.

Step-3、Determine the proper core and the minimum primary turns.

Actually, the initial selection of the core is bound to be crude since there are too many variables. One way to select the proper core is to refer to the manufacture's core selection guide. If there is no proper reference, use the table 1 as a starting point. The core recommended in table 1 is typical for the universal input range,56kHz switching frequency and single output application. When the input voltage range is 195-265 Vac or the switching frequency is higher than 56kHz, a smaller core can be used. For an application with multiple outputs, usually a larger core should be used than recommended in the table.

With the chosen core, the minimum number of turns for the

transformer primary side to avoid the core saturation is given by

$$N_P^{\min} = \frac{L_m \times I_{over}}{B_{sat} \times A_e} \times 10^6$$

where I_{over} is pulseby-pulse current limit level, Ae is the cross-sectional area of the core and Bsat is the saturation flux density in tesla. Since the saturation flux density (Bsat) decreases as the temperature goes high, the high temperature characteristics should be considered. If there is no reference data, use Bsat =0.3~0.35 T. Since the MOSFET drain current exceeds I_{ds}^{peak} and reaches lover in a transition or fault condition, lover is instead of I_{ds}^{peak} to prevent core saturation during transition.

Output Power	EI core	EE core	EPC core	EER core
0-10W	EI12.5 EI16 EI19	EE8 EE10 EE13 EE16	EPC10 EPC13 EPC17	
10-20W	EI22	EE19	EPC19	
20-30W	EI25	EE22	EPC25	EER25.5
30-50W	EI28 EI30	EE25	EPC30	EER28

Table1.Core quick selection table

Step-4、Determine the number of turns for each output

First, We must determine the turns ratio (n) between the primary side and the feedback controlled secondary side as a reference

$$n = \frac{N_P}{N_{S1}} = \frac{V_{RO}}{V_{O1} + V_{F1}}$$

where N_P and N_{S1} are the number of turns for primary side and reference output, respectively, V_{O1} is the output voltage and V_{F1} is the diode (D_{R1}) forward voltage drop of the reference output.

The number of turns for the other output (n-th output) is determined as

$$N_{S(n)} = \frac{V_{o(n)} + V_{F(n)}}{V_{o1} + V_{F1}} \times N_{s1} \quad \text{(turns)}$$

The number of turns for Vcc winding is determined as

$$N_a = \frac{V_{CC}^{'} + V_{Fa}}{V_{O1} + V_{F1}} \times N_{s1} \quad \text{(turns)}$$

where $V_{CC}^{'}$ is the nominal value of the supply voltage .and V_{Fa} is the forward voltage drop of Da as defined in figure 1 . Since Vcc increases as the output load increases, it is proper to set $V_{CC}^{'}$ as Vcc start voltage (refer to the data sheet) to avoid the over voltage protection condition during normal operation.

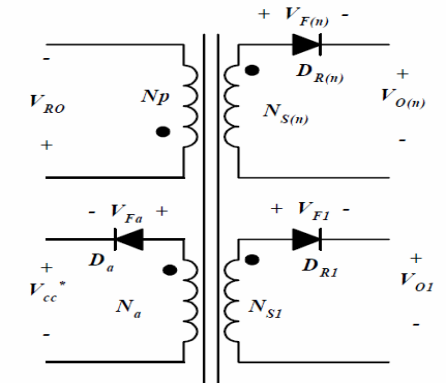


Figure 1 Simplified diagram of the transformer

With the determined turns of the primary side, the gap length of the core is obtained as

$$G = 40\pi A_e \left(\frac{N_P^{\,2}}{1000 L_m} - \frac{1}{A_L} \right) \quad \text{(mm)}$$

where A_L is the AL-value with no gap in nH/turns2, A_e is the cross sectional area of the core, N_P is the number of turns for the primary side of the transformer

Step-5、Determine the wire diameter for each winding based on the rms current of each output.

The rms current of the n-th secondary winding is obtained as

$$I_{SEC(n)} = I_{ds}^{rms} \sqrt{\frac{1 - D_{\max}}{D_{\max}}} \times \frac{V_{RO} \times K_{L(n)}}{\left(V_{O(n)} + V_{F(n)}\right)}$$

where $V_{O(n)}$ is the output voltage of the n-th output, $V_{F(n)}$ is the diode forward voltage drop, The current density is typically $5A/mm^2$ when the wire is long (>1m). When the wire is short with a small number of turns, a current density of

6-10 A/mm^2 is also acceptable. Avoid using wire with a diameter larger than 1 mm to avoid severe eddy current losses as well as to make winding easier.For high current output, it is better to use parallel windings with multiple strands of thinner wire to minimize skin effect. Check if the winding window area of the core, Aw is enough to accommodate the wires. The required winding window area (A_{wr}) is given by

$$A_{wr} = A_C / K_F$$

where A_C is the actual conductor area and K_F is the fill factor.Typically the fill factor is 0.2~0.25 for single output application and 0.15~0.2 for multiple outputs application.If the required window (A_{wr}) is larger than the actual window area (Aw), go back to the step-3 and change the core to a bigger one. Sometimes it is impossible to change the core due to cost or size constraints. If the converter is designed for CCM and the winding window (Aw) is slightly insufficient, go back to step-2 and reduce L_m by increasing the ripple factor (K_{RF}). Then, the minimum number of turns for the primary ($N_P^{\min}$) will decrease, which results in the reduced required winding window area (A_{wr}).

Step-6、Choose the rectifier diode in the secondary side based on the voltage and current ratings.

The maximum reverse voltage and the rms current of the rectifier diode ($D_{R(n)}$) of the n-th output are obtained as

$$V_{D(n)} = V_{O(n)} + \frac{V_{DC}^{MAX} \times (V_{O(n)} + V_{F(n)})}{V_{RO}}$$

where $V_{O(n)}$ is the output voltage of the n-th output and $V_{F(n)}$ is the diode ($D_{R(n)}$) forward voltage. The typical voltage and current margins for the rectifier diode are as follows

$$V_{RRM} > 1.3 V_{D(n)}$$

$$I_F > 1.5 \times I_{D(n)}^{rms}$$

where $I_{D(n)}^{rms}$ is the maximum reverse voltage and I_F is the average forward current of the diode.

Step-7、Determine the output capacitor considering the voltage and current ripple

The ripple current of the n-th output capacitor ($C_{O(n)}$) is obtained as

$$I_{cap(n)}^{rms} = \sqrt{(I_{D(n)}^{rms})^2 - I_{o(n)}^2}$$

The ripple current should be smaller than the ripple current specification of the capacitor. The voltage ripple on the n-th output is given by

$$\Delta V_{o(n)} = \frac{I_{o(n)} \times D_{\max}}{C_{o(n)} \times f_s} + \frac{I_{ds}^{peak} \times V_{RO} \times R_{C(n)} \times K_{L(n)}}{(V_{O(n)} + V_{F(n)})}$$

where $C_{o(n)}$ is the capacitance, $R_{C(n)}$ is the effective series resistance (ESR) of the n-th output capacitor, $I_{o(n)}$ and $V_{o(n)}$ are the load current and output voltage of the n-th output, respectively and $V_{F(n)}$ is the diode ($D_{R(n)}$) forward voltage.

Sometimes it is impossible to meet the ripple specification with a single output capacitor due to the high ESR of the electrolytic capacitor. Then, additional LC filter stages (post filter) can be used. When using the post filters, be careful not to place the corner frequency too low. Too low a corner frequency may make the system unstable or limit the control bandwidth. It is typical to set the corner frequency of the post filter at around 1/10~1/5 of the switching frequency.

Step-8、Design the RCD snubber.

When the power MOSFET is turned off, there is a high voltage spike on the drain due to the transformer leakage inductance. This excessive voltage on the MOSFET may lead to an avalanche breakdown and eventually failure. Therefore, it is necessary to use an additional network to clamp the voltage.The RCD snubber circuit and MOSFET drain voltage waveform are shown in figure 10 and 11, respectively. The RCD snubber network absorbs the current in the leakage inductance by turning on the snubber diode ($D_{S(n)}$) once the MOSFET drain voltage exceeds the voltage of node X as

depicted in figure 10. In the analysis of snubber network, it is assumed that the snubber capacitor is large enough that its voltage does not change significantly during one switching cycle.The first step in designing the snubber circuit is to determine the snubber capacitor voltage at the minimum input voltage and full load condition (V_{sn}). Once V_{sn} is determined, the power dissipated in the nubber network at the minimum input voltage and full load condition is obtained as

$$P_{sn}=\frac{(V_{sn})^2}{R_{sn}}=\frac{1}{2}f_s L_{lk}(I_{ds}{}^{peak})^2\times\frac{V_{sn}}{V_{sn}-V_{RO}}$$

where Llk is the leakage inductance, Vsn is the snubber capacitor voltage at the minimum input voltage and full load condition, V_{RO} is the reflected output voltage and Rsn is the snubber resistor. V_{sn} should be larger than V_{RO} and it is typical to set V_{sn} to be 2~2.5 times of V_{RO} . Too small a Vsn results in a severe loss in the snubber network. The leakage inductance is measured at the switching frequency on the primary winding with all other windings shorted.Then, the snubber resistor with proper rated wattage should be chosen based on the power loss. The maximum ripple of the snubber capacitor voltage is obtained as

$$\Delta V_{sn}=\frac{V_{sn1}}{C_{sn}\times R_{sn}\times f_s}$$

where fs is switching frequency. In general, 5~10% ripple is reasonable.The snubber capacitor voltage (V_{sn}) is for the minimum input voltage and full load condition. When the converter is designed to operate in CCM, the peak drain current together with the snubber capacitor voltage decrease as the input voltage increases. The snubber capacitor voltage under maximum input voltage and full load condition is obtained as

$$V_{sn2}=\frac{V_{RO}+\sqrt{(V_{RO})^2+2R_{sn}L_{lk}f_s(I_{ds2})^2}}{2}$$

where f_s is switching frequency, L_{lk} is the primary side leakage inductance, V_{RO} is the reflected output voltage, R_{sn} is the snubber resistor and I_{ds2} is the peak drain current at the maximum input voltage and full load condition. When the converter operates in CCM at the maximum input voltage and full load condition, the Ids2 is obtained as

$$I_{ds2}=\frac{P_{in}\times(V_{DC}{}^{MAX}+V_{RO})}{V_{DC}{}^{MAX}\times V_{RO}}+\frac{V_{DC}{}^{MAX}\times V_{RO}}{2L_m\times f_s\times(V_{DC}{}^{MAX}+V_{RO})}$$

When the converter operates in DCM at the maximum input voltage and full load condition, the I_{ds2} is obtained as

$$I_{ds2}=\sqrt{\frac{2\times P_{in}}{f_S\times L_m}}$$

the maximum voltage stress on the internal MOSFET is given by

$$V_{ds}{}^{\max}=V_{DC}{}^{\max}+V_{sn2}$$

Check if $V_{ds}{}^{\max}$ is below 90% of the rated voltage of the MOSFET (BVdss) as shown in figure 2. The voltage rating of the snubber diode should be higher than BVdss. Usually, an ultra fast diode with 1A current rating is used for the snubber network.In the snubber design in this section, neither the lossy discharge of the inductor nor stray capacitance is considered. In the actual converter, the loss in the snubber network is less than the designed value due to this effects.

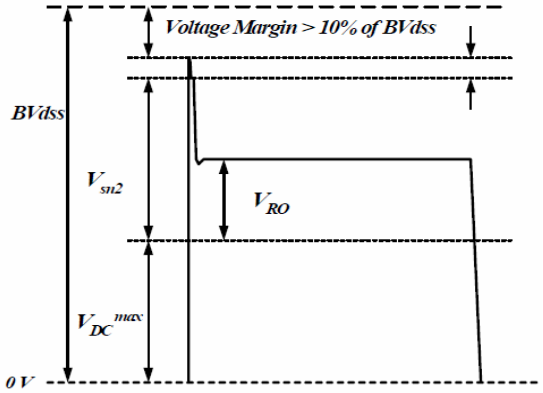


Figure2.MOSFET drain voltage and snubber capacitor voltage

TEST DATA

SS1203(12V)

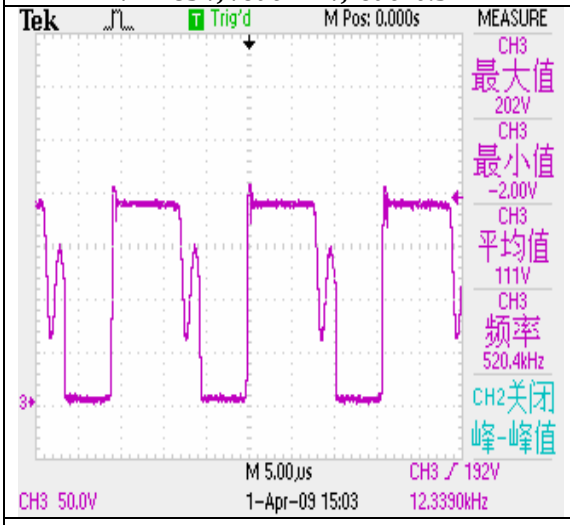
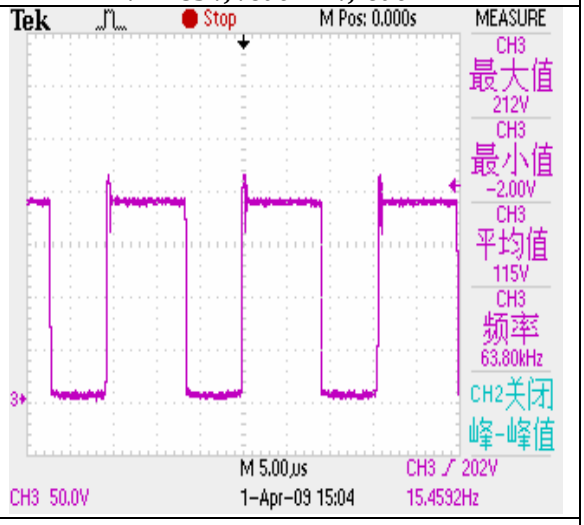
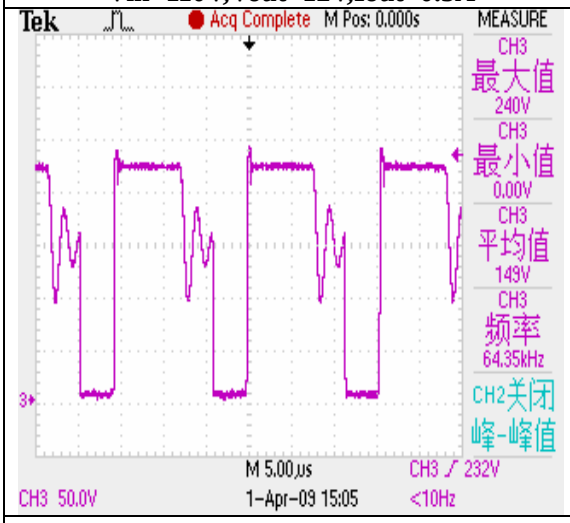
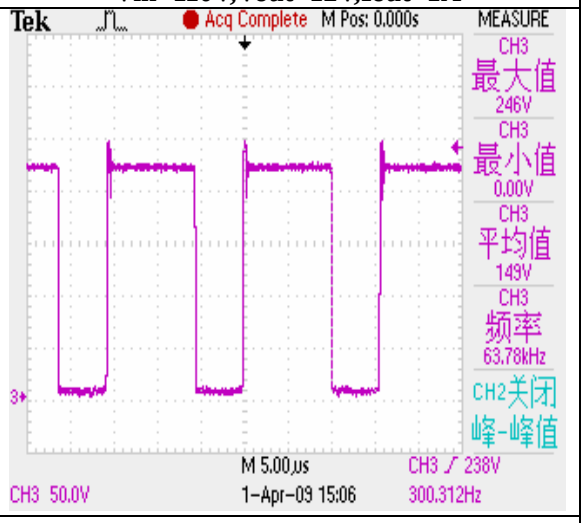
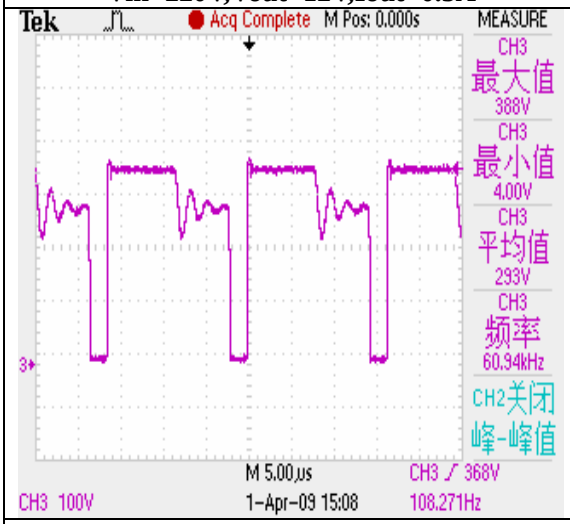
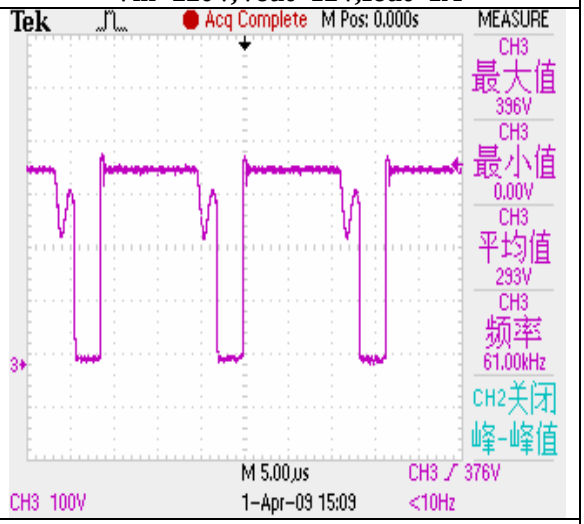
V_{IN} (V_{AC})	P_{IN} (W)	V_{OUT} (V)	I_{OUT} (A)	V_{CC} (V)	V_{OR} (mVp-p)	P_{OUT} (W)	η (%)	OCP (A)	OPP (A)	Average η(%)	CEC Standerd η(%)
90Vac	0.1	12.1	0	5.36		0		1.07	1.36	79.05	
	3.2	12.1	0.2	6.64		2.4	75.0				
	7.6	12.1	0.5	6.64		6.1	80.3				
	12.0	12.1	0.8	6.64		9.7	80.8				
	15.1	12.1	1.0	6.64		12.1	80.1				
100Vac	0.1	12.1	0	5.28		0		1.13	1.45	80.35	
	3.1	12.1	0.2	6.70		2.4	77.4				
	7.5	12.1	0.5	6.70		6.1	81.3				
	11.9	12.1	0.8	6.70		9.7	81.5				
	14.9	12.1	1.0	6.70		12.1	81.2				
240Vac	0.1	12.1	0	4.96		0		1.69	2.13	82.95	
	3.0	12.1	0.2	6.96		2.4	80.0				
	7.3	12.1	0.5	6.96		6.1	83.5				
	11.5	12.1	0.8	6.96		9.7	84.3				
	14.4	12.1	1.0	6.96		12.1	84.0				
265Vac	0.1	12.1	0	4.88		0		1.72	2.17	82.35	
	3.0	12.1	0.2	7.04		2.4	80.0				
	7.4	12.1	0.5	7.04		6.1	82.4				
	11.6	12.1	0.8	7.04		9.7	83.6				
	14.5	12.1	1.0	7.04		12.1	83.4				

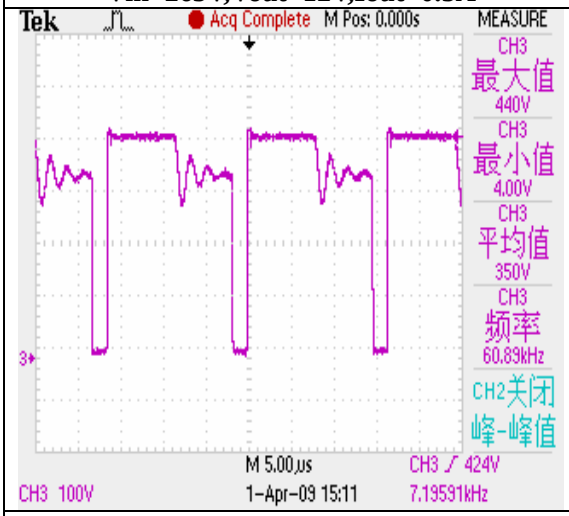
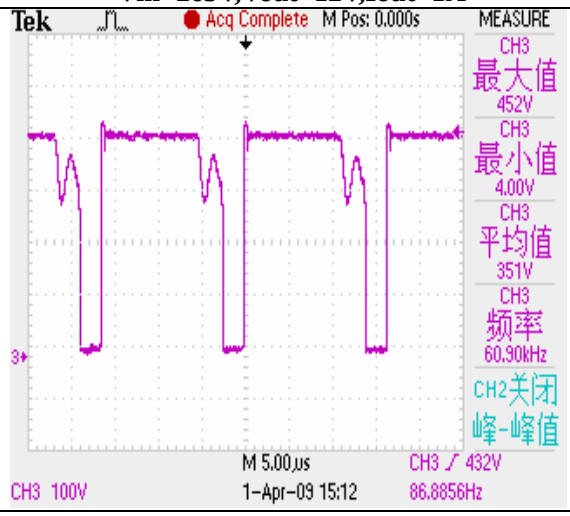
Output Voltage and Output Ripple Voltage

Vin(V) / Iout(A)	85V		110V		135V	
	Vout(V)	Vripple(mV)	Vout(V)	Vripple(mV)	Vout(V)	Vripple(mV)
0.25	12.18	5.00	12.18	3.52	12.18	3.76
0.50	12.18	9.00	12.18	5.36	12.18	5.84
0.75	12.18	14.00	12.18	8.00	12.18	7.68
1.00	12.18	31.20	12.18	11.60	12.18	8.40
Vin(V) / Iout(A)	180V		220V		265V	
	Vout(V)	Vripple(mV)	Vout(V)	Vripple(mV)	Vout(V)	Vripple(mV)
0.25	12.18	4.32	12.18	5.12	12.18	5.36
0.50	12.18	6.40	12.18	6.16	12.18	5.92
0.75	12.18	7.00	12.18	7.28	12.18	6.40
1.00	12.18	9.00	12.18	8.48	12.18	7.76

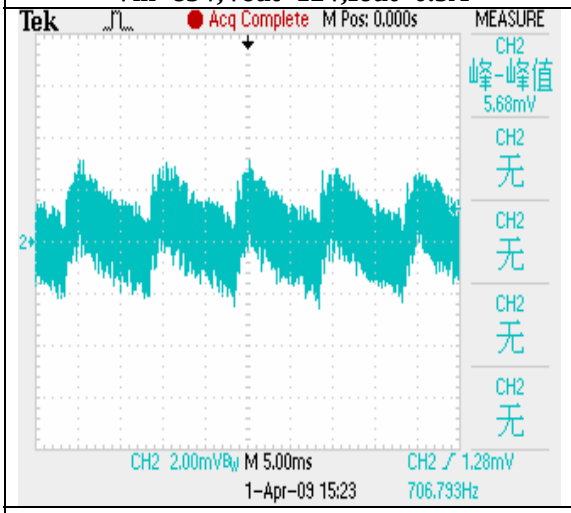
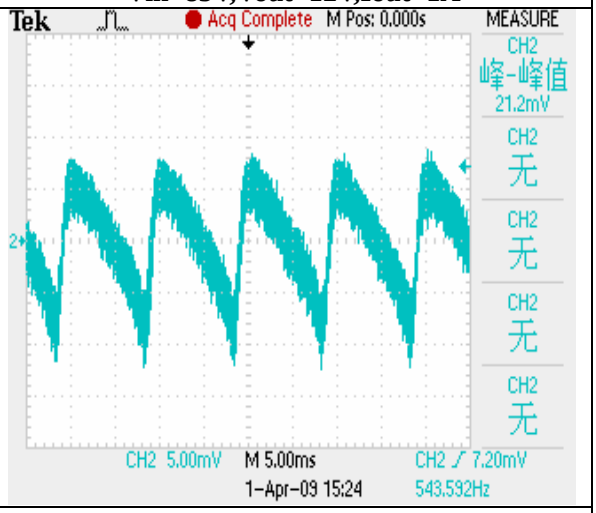
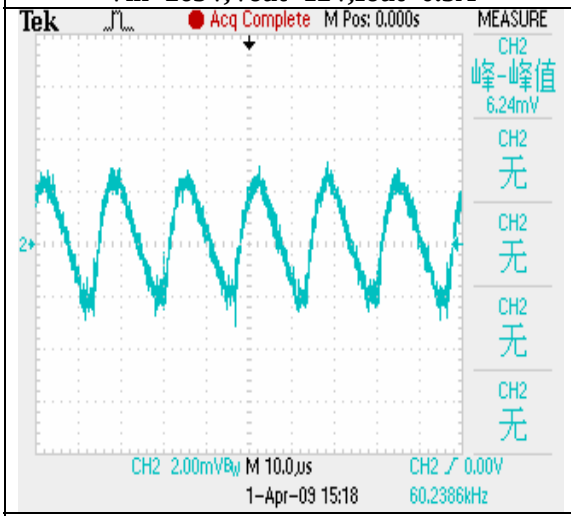
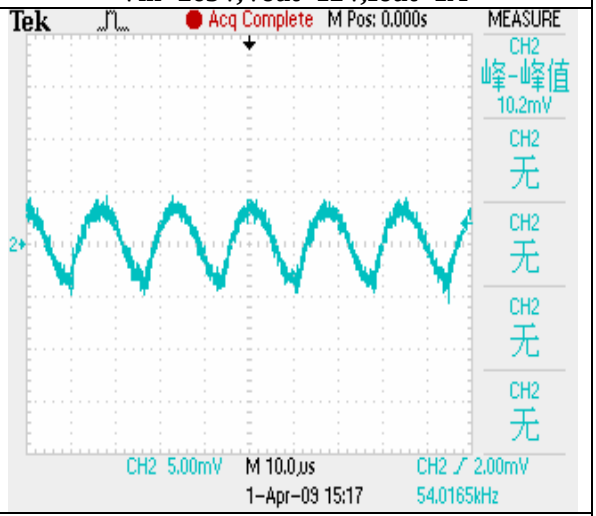
Test Waveform:

Vce waveform:

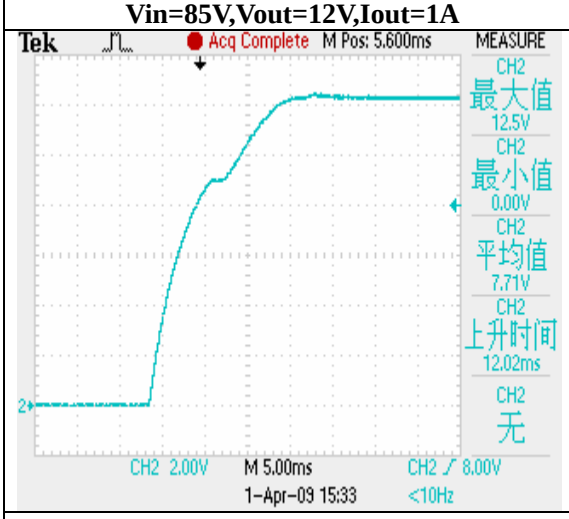
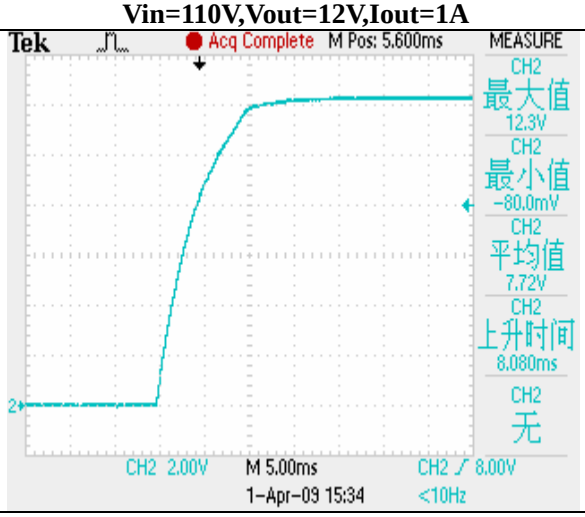
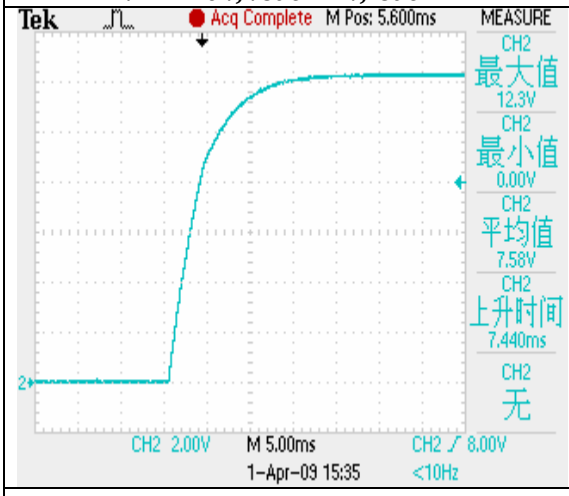
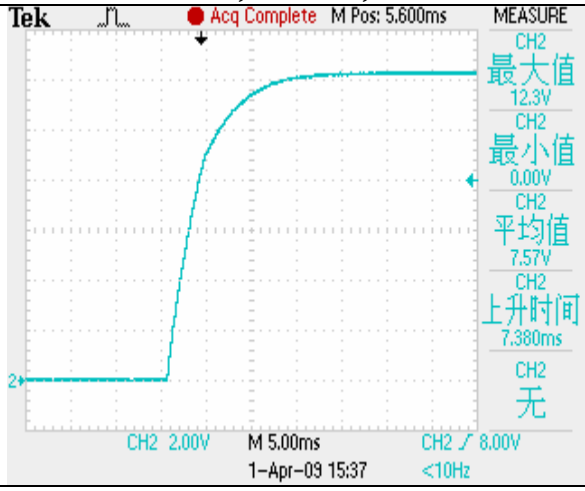
Vin=85V,Vout=12V,Iout=0.5A	Vin=85V,Vout=12V,Iout=1A
	
Vin=110V,Vout=12V,Iout=0.5A	**Vin=110V,Vout=12V,Iout=1A**
	
Vin=220V,Vout=12V,Iout=0.5A	**Vin=220V,Vout=12V,Iout=1A**
	

Vin=265V,Vout=12V,Iout=0.5A	Vin=265V,Vout=12V,Iout=1A
	

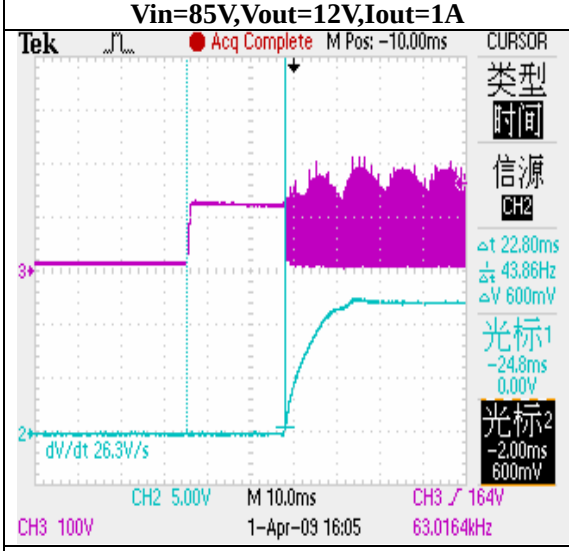
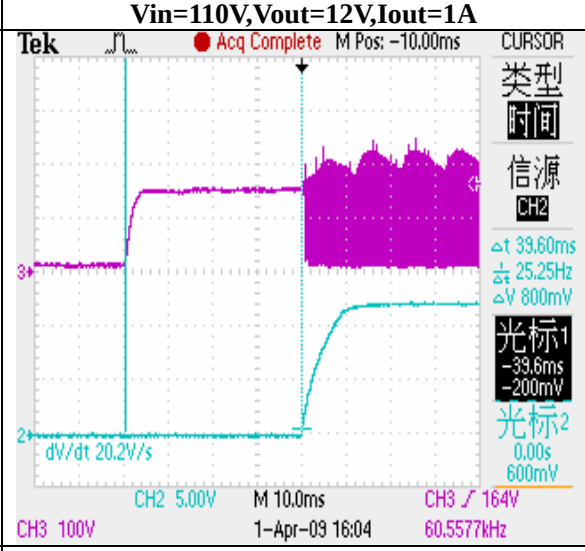
Output Ripple Voltage

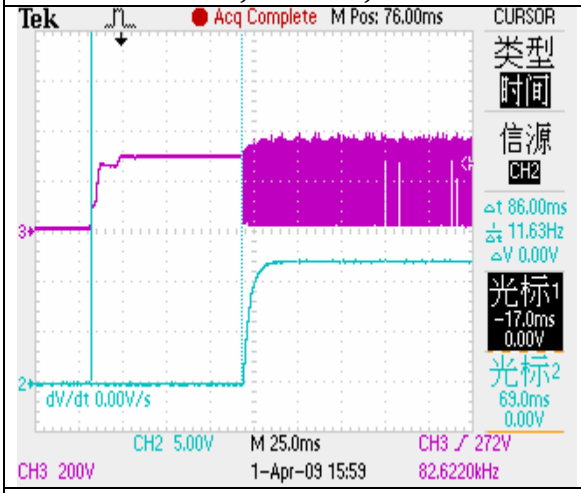
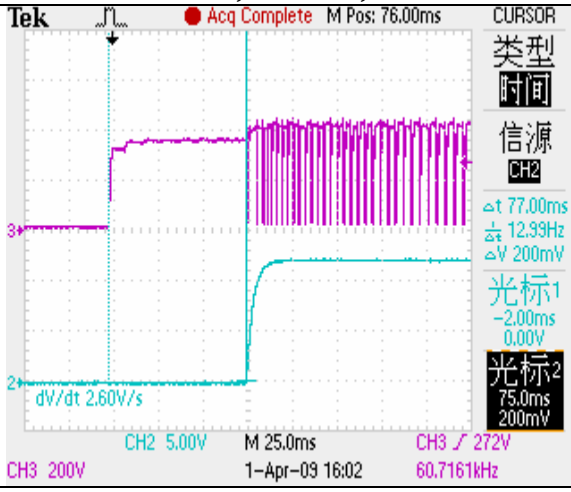
Vin=85V,Vout=12V,Iout=0.5A	Vin=85V,Vout=12V,Iout=1A
	
CH2:Vout	**CH2:Vout**
Vin=265V,Vout=12V,Iout=0.5A	**Vin=265V,Vout=12V,Iout=1A**
	
CH2:Vout	**CH2:Vout**

Turn On Waveform:

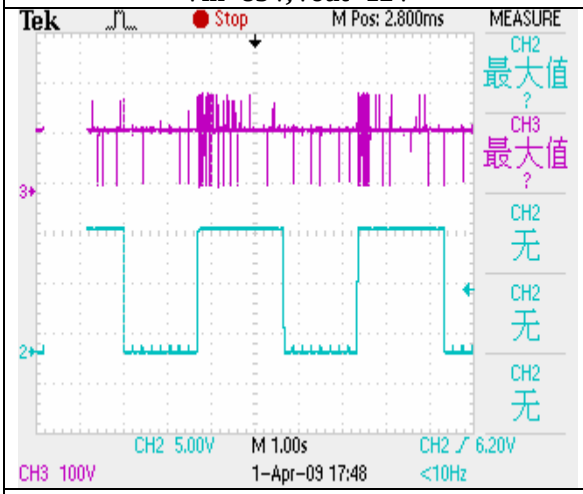
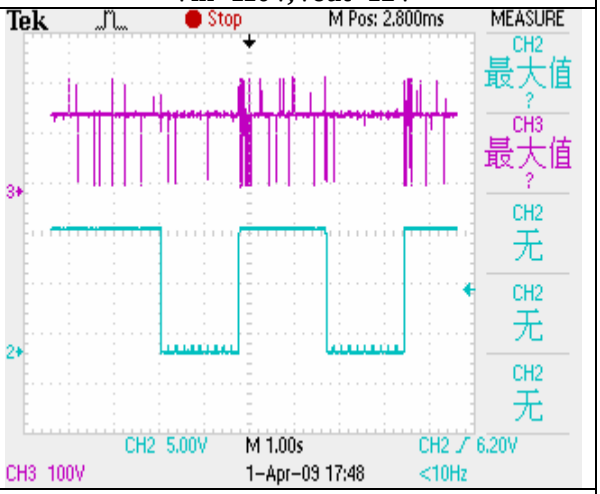
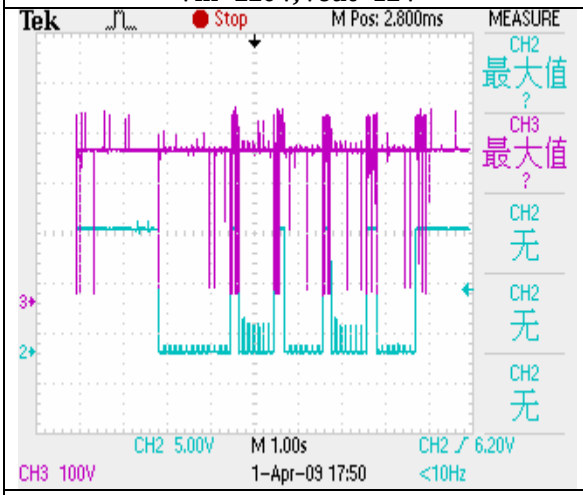
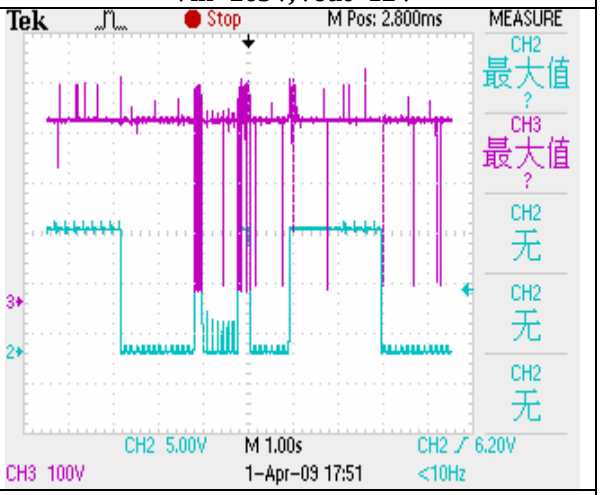
Vin=85V,Vout=12V,Iout=1A	Vin=110V,Vout=12V,Iout=1A
	
CH2:Vout	CH2:Vout
Vin=220V,Vout=12V,Iout=1A	Vin=265V,Vout=12V,Iout=1A
	
CH2:Vout	CH2:Vout

Vce and Vout

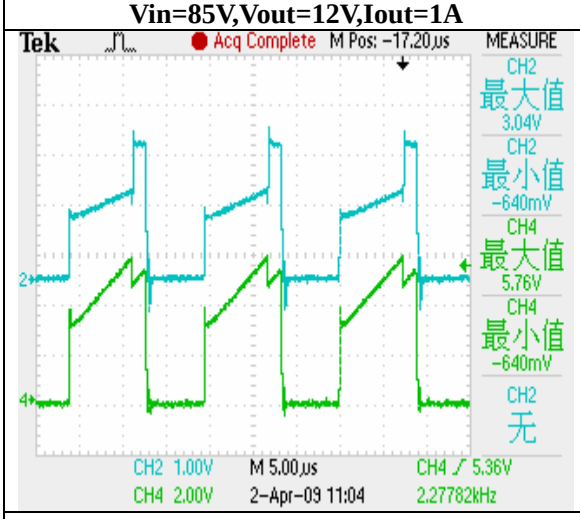
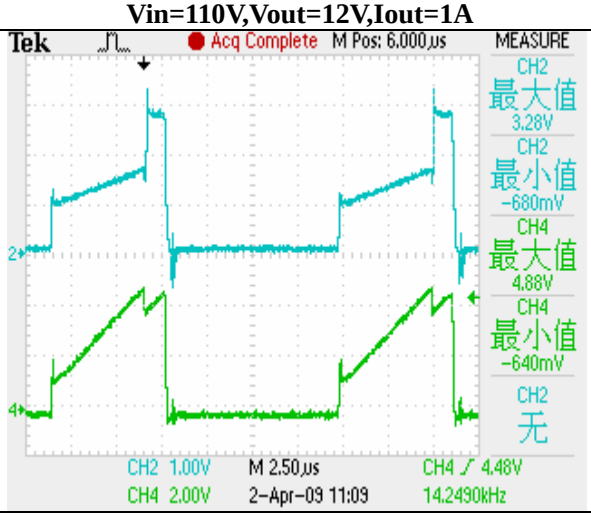
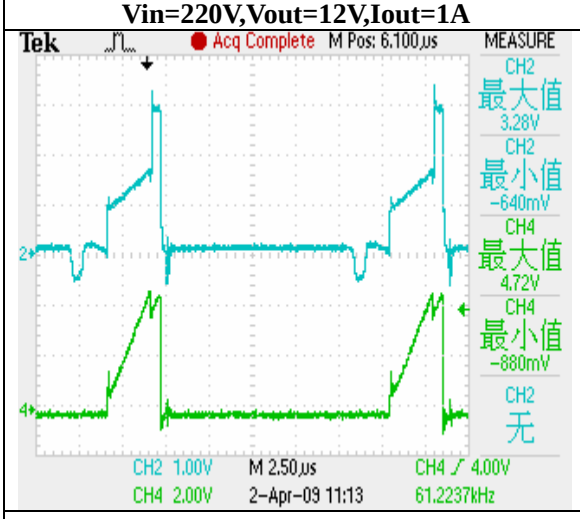
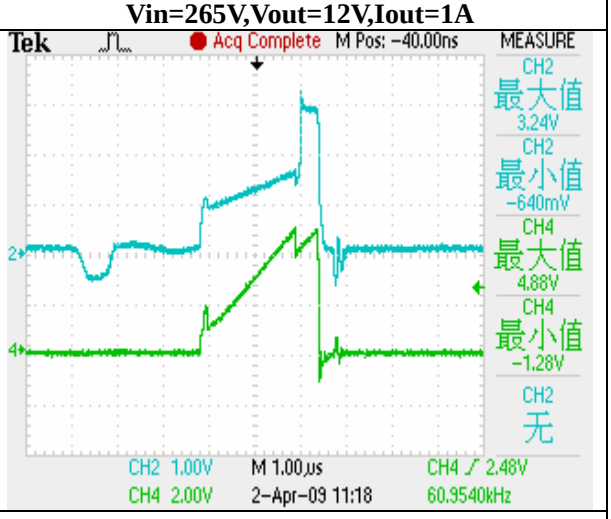
Vin=85V,Vout=12V,Iout=1A	Vin=110V,Vout=12V,Iout=1A
	
CH2:Vout;CH3:Vce	CH2:Vout;CH3:Vce

Vin=220V,Vout=12V,Iout=1A	Vin=265V,Vout=12V,Iout=1A
	
CH2:Vout;CH3:Vce	CH2:Vout;CH3:Vce

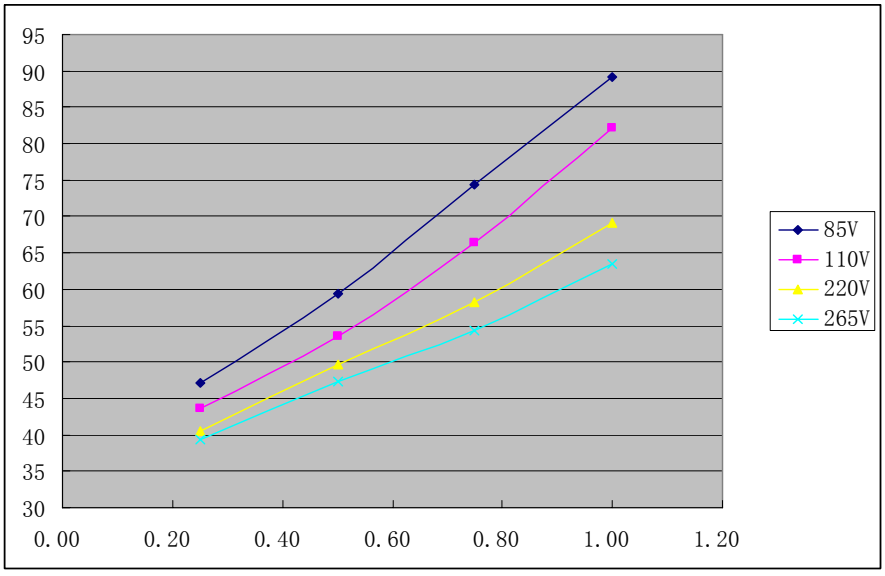
Short Output:

Vin=85V,Vout=12V	Vin=110V,Vout=12V
	
CH2:Output Voltage,CH3:Vce	CH2:Output Voltage,CH3:Vce
Vin=220V,Vout=12V	**Vin=265V,Vout=12V**
	
CH2:Output Voltage,CH3:Vce	CH2:Output Voltage,CH3:Vce

VOB and VIS

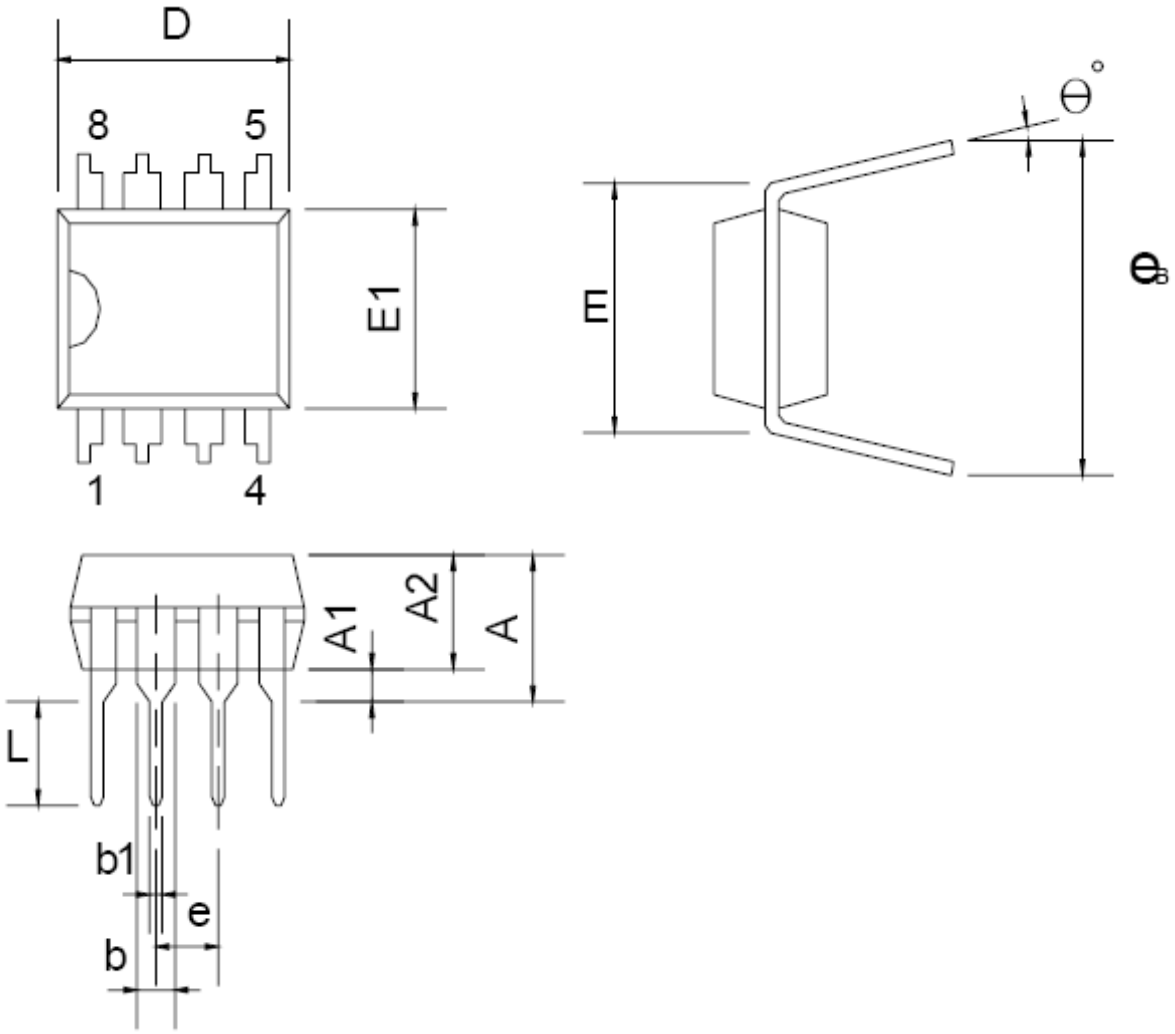
Vin=85V,Vout=12V,Iout=1A	Vin=110V,Vout=12V,Iout=1A
	
CH2:VOB; CH4:VIS	CH2:VOB; CH4:VIS
Vin=220V,Vout=12V,Iout=1A	**Vin=265V,Vout=12V,Iout=1A**
	
CH2:VOB; CH4:VIS	CH2:VOB; CH4:VIS

Temperature:



PACKAGE INFORMATION

DIP-8



Dimensions

Symbol	Millimeter			Inch		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			5.334			0.210
A1	0.381			0.015		
A2	3.175	3.302	3.429	0.125	0.130	0.135
b		1.524			0.060	
b1		0.457			0.018	
D	9.017	9.271	10.160	0.355	0.365	0.400
E		7.620			0.300	
E1	6.223	6.350	6.477	0.245	0.250	0.255
E		2.540			0.100	
L	2.921	3.302	3.810	0.115	0.130	0.150
e_B	8.509	9.017	9.525	0.335	0.355	0.375
θ°	0°	7°	15°	0°	7°	15°