AN-8025

Design Guideline of Single-Stage Flyback AC-DC Converter Using FAN7530 for LED Lighting

Summary

This application note describes the single-stage power factor correction (PFC) and presents the design guidelines of a 75W universal-input, single-stage PFC for LED lighting applications. Flyback converter topology controlled by the critical current mode control IC, FAN7530 is applied and several functions; such as CV/CC mode feedback circuits, cycle-by-cycle current limit, soft-starting function, and so on, are considered for LED lighting applications.

Introduction

Despite large output voltage ripple, single-stage AC-DC conversion is a more attractive solution than two-stage conversion from the standpoint of the cost and power density. Especially in applications like battery chargers, Plasma Display Panel (PDP)-sustaining power supplies, and LED lighting; low frequency, 100Hz or 120Hz, large output voltage ripple is inconsequential. Consequently, the single-stage AC-DC conversion is very advantageous.

Single-stage AC-DC converter directly converts AC input voltage to the DC output voltage without a pre-regulator, as shown in Figure 1.

This application note presents a 75W single-stage AC-DC converter for LED lighting. As a power-conversion topology, flyback converter is normally chosen because it doesn't need an inductive output filter; the main transformer works as an inductive filter itself.

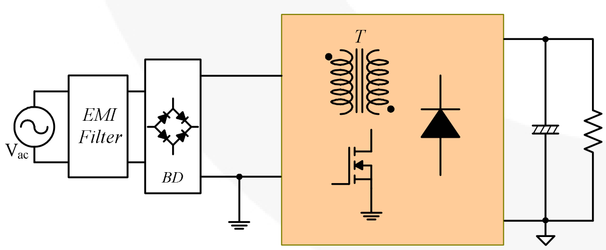


Figure 1. Single-Stage AC-DC Converter

Figure 2 shows the circuit diagram of a flyback AC-DC converter. FAN7530 is used as a controller and both CV (constant voltage) and CC (constant current) mode feedback circuits are applied to prevent overload and over-voltage conditions. In LED lighting, the output is always full-load condition and the forward voltage drop of LED decreases if the junction temperature of LED increases. Therefore the output should be controlled by CC mode in the normal state while CV mode only works as over voltage protection.

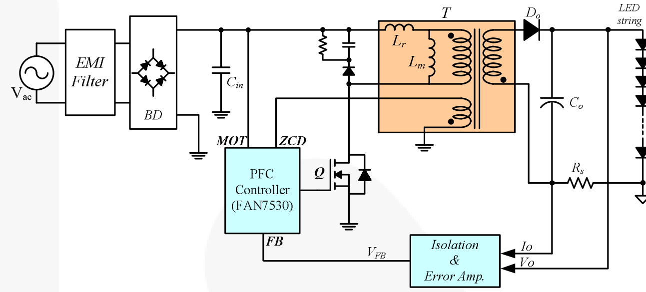


Figure 2. Circuit Diagram of a Flyback AC-DC Converter

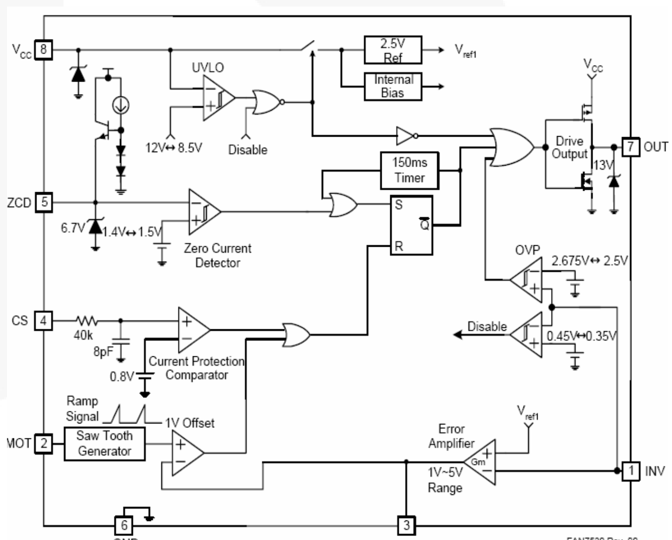


Figure 3. Block Diagram of FAN7530

Figure 3 shows the block diagram of FAN7530. Its major features are:

- Fixed On Time CRM PFC Controller
- Zero Current Detector (ZCS) & Valley Switching
- MOSFET Over-Current Protection
- Low Startup (40µ A) and Operating Current (1.5mA)
- Totem Pole Output with High State Clamp
- +500/-800mA Peak Gate Drive Current

FAN7530 is a voltage-mode CRM PFC controller; the turn-on time of switch is fixed while the turn-off time is varied during the steady state. Therefore, the switching frequency varies in accordance with the input voltage variation shown in Figure 4.

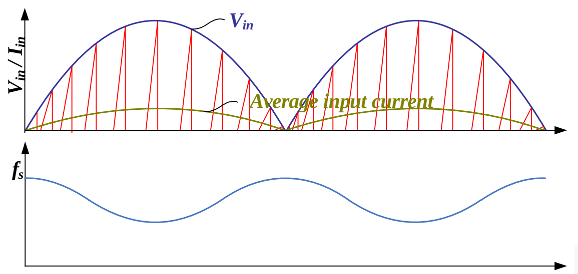


Figure 4. Switching Frequency Variation

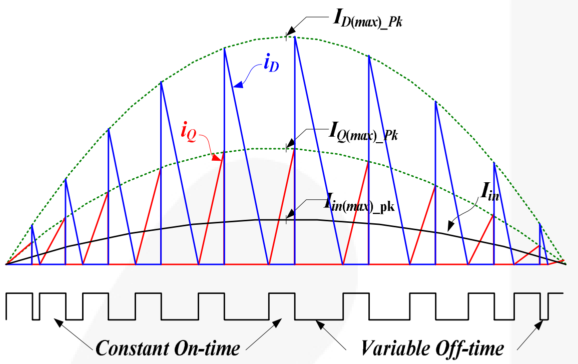


Figure 5. Theoretical Waveforms

Figure 5 illustrates the theoretical waveforms of the primary-side switch current, the secondary-side diode current, and gating signal. MOSFET Q turns on and Fast Recovery Diode (FRD) D_o turns off under zero-current condition, while Q turns off and D_o turns on under the hard-switching condition.

Design Example

A design guideline of 75W single-stage flyback AC-DC converter using FAN7530 is presented. The applied system parameters are shown in Table 1.

Table 1. System Parameters

Parameter	Value
Output Power	75W
Input Voltage Range	85~265V_{AC}
Output Voltage	45V
Output Limit Voltage	50V
Duty Ratio at $I_{in(max)\_pk}$, $D_{@\ Iin(max)\_pk}$	0.6
Minimum Switching Frequency, f_{s_min}@ V_{in_min}	50kHz
Efficiency, η	85%

1. Flyback Transformer Design

In flyback converter, the transformer is easily saturated because the transformer is only utilized in the first quadrant. Moreover, if it works under the critical conduction mode, the peak current is much higher than that of the continuous conduction mode. Therefore, air-gap should be inserted to prevent saturation of the transformer.

A proper turn ratio, N_1/N_2, should also be considered in a flyback single-stage AC-DC converter because the maximum voltage rating of the MOSFET and Fast Recover Diode (FRD) strongly relates to the turn ratio of transformer. There is a trade-off relationship between the drain-to-source voltage rating, V_{dss}, of MOSFET and the reverse voltage rating, V_R, of the FRD in accordance with the turn ratio of the transformer. A larger turn ratio (N_1/N_2) requires a higher V_R of FRD while V_{dss}, of MOSFET is decreased. In contrast, a lower turn ratio causes a higher voltage stress on the MOSFET, while V_R of the FRD is decreased. Figure 6 shows the trade-off relationship between V_{dss} of the MOSFET and V_R of the FRD.

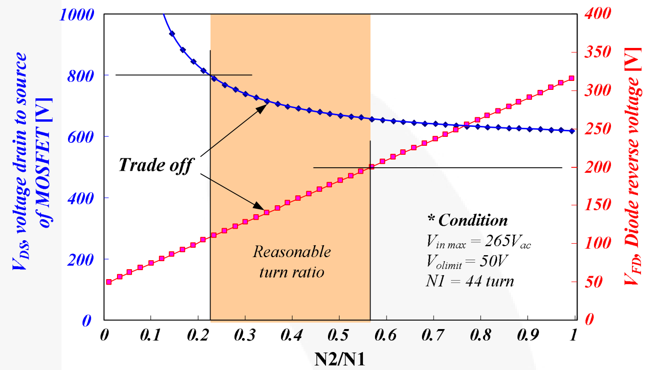


Figure 6. Trade-Off Between V_{DS} and V_R

From $P_o=\eta V_{in} I_{in}$, the maximum line current $I_{in(max)} = P_o/\eta V_{in(min)}$. If the switching frequency f_s is much higher than the AC line frequency, f_{ac}, the input current can be assumed to be constant during one switching period.

To define the magnetizing inductance of transformer, the largest period must be defined. The largest switching period occurs at the peak of input current, $I_{in(max)\_pk}$, when the minimum input voltage is applied. It can be defined as:

$$I_{in(\max)\_pk} = \frac{1}{T}\int_0^{DT} \frac{I_{Q(\max)\_pk}}{D_{\max}T} t\,dt = \frac{D_{\max} I_{Q(\max)\_pk}}{2} \tag{1}$$

$$I_{Q(\max)\_pk} = \frac{2}{D_{\max}} I_{in(\max)\_pk} \tag{2}$$

where $I_{in(\max)\_pk} = \sqrt{2} I_{in(\max)}$ and $V_{in(\min)\_pk} = \sqrt{2} V_{in(\min)}$, respectively.

The transformer primary-side voltage, V_T, is defined as:

$$V_T = L_m \frac{\Delta I}{\Delta T} = L_m \frac{I_{Q(\max)\_pk} f_{s(\min)}}{D_{@\ \mathrm{Iin(max)\_pk}}} \tag{3}$$

Therefore, the magnetizing inductance is calculated by:

$$L_m \geq \frac{D_{@\ \mathrm{Iin(max)\_pk}}{}^2 V_{in(\min)}}{2 I_{in(\max)\_pk} f_{s(\min)}} = \frac{0.6^2 \times 85}{2\times 1.04 \times 50 \times 10^3} \tag{4}$$
$$= 294 \times 10^{-6}$$

From Equation (4) and Table 1, the calculated magnetizing inductance is 294μH.

There are several methods defining the turn number for the desirable inductance, but using the AL-value is the most common and the easiest. The turn number can be obtained with AL-value as:

$$N = \sqrt{\frac{L}{AL - value}} \quad (4)$$

However, if air-gap is inserted into the magnetic core, a designer should find the AL-value. To obtain AL-value, wind several turns into a bobbin and measure the inductance, then calculate AL-value with the equation:

$$AL - value = \frac{L}{N^2} \quad (5)$$

Once the AL-value is obtained, calculate the turn number using Equation (5).

Applying coil dummy EER3435 with 0.33mm of air gap for the transformer and 14.9µH is measured when 10 turns are winded into the core and 0.149×10-6 of AL-value is obtained. Therefore, the calculated primary-side turn number is 44.4 from Equation (5) and determines 44 as the primary-side turn number. (The actual inductance is measured as 330µH).

The secondary-side turn number is obtained as 17 turns by following equation:

$$N_2 = \frac{\pi N_1 V_o (1 - D_{\max})}{2\sqrt{2} D_{\max} V_{in(\min)}} = \frac{\pi \times 44 \times 45 (1 - 0.6)}{2\sqrt{2} \times 0.6 \times 85} = 17 \quad (6)$$

2. MOSFET and FRD

The voltage stress of MOSFET is calculated as:

$$V_{ds(\max)} = V_{in(\max)\_pk} + \frac{N_1}{N_2} V_o + V_{sn} \quad (7)$$

where V_{sn} is the maximum ringing voltage of the snubber circuit and normally estimated as 1.5 times of the flyback voltage. The maximum voltage of MOSFET is obtained as:

$$V_{ds(\max)} = \sqrt{2} \times 265 + \frac{44}{17} \times 45 + 1.5\left(\frac{44}{17} \times 45\right) = 665.94V \quad (8)$$

The maximum rms current and the peak current are:

$$I_{in(\max)} = \frac{P_o}{\eta V_{in(\min)}} = \frac{75}{0.85 \times 85} = 1.04A \quad (9)$$

and

$$I_{Q(\max)\_pk} = \frac{2\sqrt{2} P_o}{\eta D_{\max} V_{in(\min)}} = \frac{2\sqrt{2} \times 75}{0.85 \times 0.6 \times 85} = 4.89A \quad (10)$$

respectively.

Therefore, an N-Channel enhancement-mode MOSFET, FQPF8N80C (800V, 8A, R_{DS_ON} = 1.55Ω), is chosen in consideration of the margins.

The maximum reverse voltage and the forward peak current of the FRD are:

$$V_{R(\max)} = V_{o\_Limit} + \frac{N_2}{N_1} V_{in(\max)\_pk} = 50 + \frac{17}{44} \times \sqrt{2} \times 265 = 195V \quad (11)$$

$$I_{R\_pk} = \frac{2}{(1 - D_{\min})} I_o = \frac{2}{(1 - 0.33)} \times \frac{75}{45} = 4.98A \quad (12)$$

respectively, where minimum duty ratio D_{min} is obtained as:

$$D_{\min} = \frac{V_o}{\frac{N_2}{N_1} V_{iavg(\max)} + V_o} = \frac{45}{\frac{17}{44} \times \left(\frac{2\sqrt{2}}{\pi} \times 265\right) + 45} = 0.33 \quad (13)$$

Therefore, the Ultra-Fast Rectifier Diode (UFRD), F06UP20S (200V, 6A, V_F=1.15V), is finally chosen in consideration of the margins.

3. Snubber Circuit Design

In flyback converter, the resonant between L_{leak} and C_{oss} causes an excessively high voltage surge that causes damage to the MOSFET during turn-off. This voltage surge must be suppressed and a snubber circuit is therefore necessary to prevent MOSFET failures.

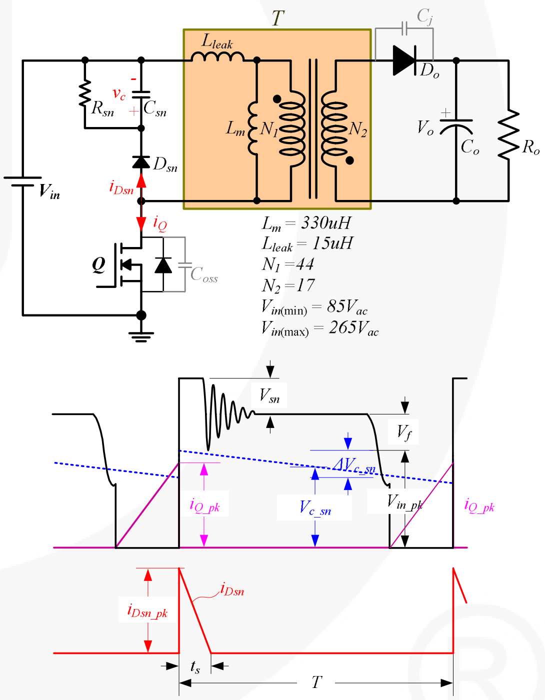


Figure 7. Snubber Circuit

The clamping voltage by snubber is:

$$V_{sn} = L_{leak} \frac{\Delta i}{\Delta t} = L_{leak} \frac{I_{Dsn\_pk}}{t_s} \quad (14)$$

Therefore:

$$t_s = \frac{L_{leak} \times I_{Dsn\_pk}}{V_{sn}} \quad (15)$$

The maximum power dissipation of the snubber circuit is determined by:

$$P_{sn} = \frac{1}{T}\int_0^{t_s} V_{sn} i_{Dsn}(t)dt = \frac{1}{2} L_{leak} I_{Dsn\_pk}{}^2 f_s \qquad (16)$$

The maximum power dissipation is:

$$P_{sn(\max)} = \frac{1}{2} L_{leak} I_{Dsn\_pk}{}^2 f_{s@vin\max} = \frac{v_c{}^2}{R_{sn}} \qquad (17)$$

where $v_c = V_f + V_{sn}$.

Therefore, the resistance, R_{sn}, is determined by:

$$R_{sn} = \frac{2 v_c{}^2}{L_{leak} I_{Dsn\_pk}{}^2 f_{s@vin\max}} \qquad (18)$$

The maximum ripple voltage of the snubber circuit is obtained by:

$$\Delta v_c = \frac{v_c}{C_{sn} R_{sn} f_{s@vin\max}} \qquad (19)$$

The larger snubber capacitor results, the lower voltage ripple, but the power dissipation increases. Consequently, selecting the proper value is important. In general, it is reasonable to determine that the snubber voltage is 1.5 times of the flyback voltage and the ripple voltage, Δv_c is 50V. Thus the snubber resistor and capacitor are determined by the following equations:

$$I_{Dsn\_pk@V_{in}=265V} = \frac{2\sqrt{2}P_o}{\eta D_{\min} V_{in}} = \frac{2\sqrt{2}\times 75}{0.85\times 0.33\times 265} = 2.85A \qquad (20)$$

$$V_{sn(\max)} = 1.5V_f = 1.5\times\frac{N_1}{N_2}\times V_{o\_Limit} = 1.5\times\frac{44}{17}\times 50 = 194.1V \qquad (21)$$

$$t_s = \frac{15\times 10^{-6}\times 2.85}{194.1} = 220.3ns \qquad (22)$$

$$f_{s@v_{in}(\max)} = \frac{D_{\min} V_{sn(\max)}}{L_m I_{Dsn\_pk@V_{in}=265V}} = \frac{0.33\times 194}{297\times 10^{-6}\times 2.85} = 75.63kHz \qquad (23)$$

$$R_{sn} = \frac{2\times 194^2}{15\times 10^{-6}\times 2.85\times 75.63kHz} = 23.3k\Omega \qquad (24)$$

$$C_{sn} = \frac{v_f + V_{sn}}{\Delta v_c \times R_{sn}\times f_{s@v_{in}(\max)}} = \frac{194+129}{50\times 23.3\times 10^3\times 75.63\times 10^3} = 3.67nF \qquad (25)$$

4. Sensing Resistor

The CS pin of FAN7530 limits the peak current and protects the MOSFET during transient state or over load condition. Normally, it is reasonable to limit to 1.5 times the switching peak current. The limiting level of switching peak current and the sensing resistor are obtained as:

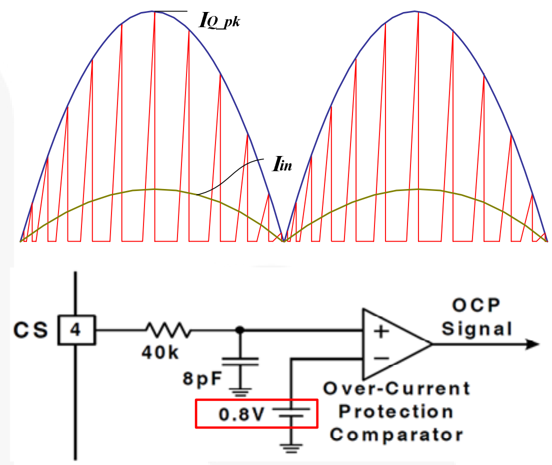


Figure 8. Switching Current Limit

$$I_{Q\_Limit} = 1.5 I_{Q(\max)\_pk} = 1.5\times\frac{2}{D_{\max}}\left(\sqrt{2}\frac{P_o}{\eta V_{in(\min)}}\right) = 1.5\times\frac{2}{0.6}\left(\sqrt{2}\frac{75}{0.85\times 85}\right) = 7.4A \qquad (26)$$

$$R_s \le \frac{0.8}{I_{Q\_Limit}} = \frac{0.8}{7.4} = 0.11\Omega \qquad (27)$$

5. Soft-starting Circuit

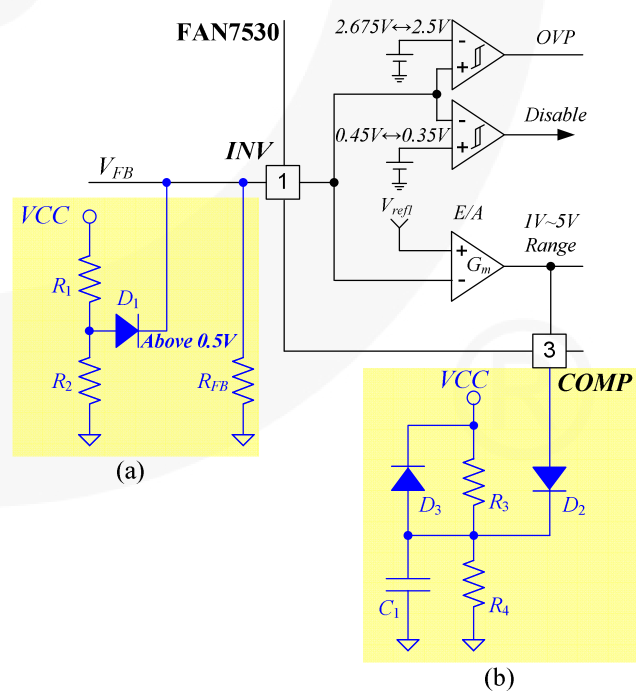


Figure 9. Soft-Starting Circuit

Since the FAN7530 is designed for a non-isolated boost PFC circuit, some circuits are added externally. The internal disable amplifier can be used as soft-start function when FAN7530 is applied to non-isolated PFC circuit. However, the disable amplifier can not participate in the operation if it is applied to isolated single stage PFC circuit because the initial voltage at Pin 1 is zero and FAN7530 can not start. To exclude the disable amplifier from operation, over 0.5V of voltage must be applied through a blocking diode, as shown in Figure 9(a).

The initial V_{FB} is approximately defined as:

$$V_{FB\_initial} = \frac{R_1 R_{FB}}{R_{FB}(R_1 + R_2) + R_1 R_2} \cdot VCC \qquad (28)$$

To prevent MOSFET failure due to the initial excessive switching current, an external soft-start function is necessary. The circuit shown in Figure 9(b) makes the output voltage of E/A increase slowly and, consequently, the converter can be smoothly started in accordance with the gradual increase of the on time.

6. Voltage and Current Feedback

Power supplies for LED lighting must be controlled by constant current (CC) mode as well as a constant voltage (CV) mode. Because the forward voltage drop of LED varies with the junction temperature and the current also increases greatly consequently, devices can be damaged.

Figure 10 shows an example of a CC and CV mode feedback circuit. During normal operation, CC mode is dominant and CV mode only acts as OVP for abnormal modes.

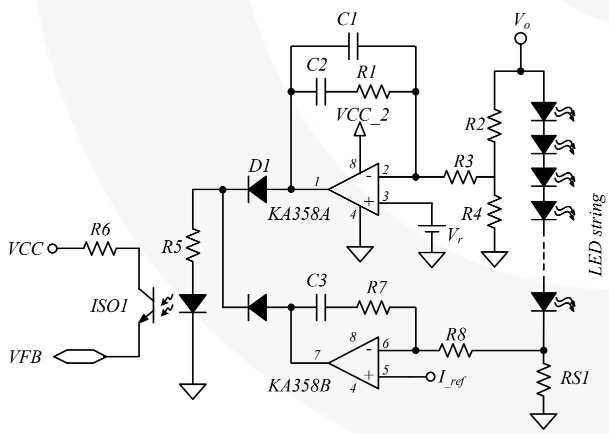


Figure 10. Example of CC & CV Feedback Circuit

Experimental Results

To verify the validity of the design guideline in this application note, a prototype test set-up was built and tested. The design parameter and component values are shown in the appendix.

Figure 11 shows the input voltage and current at $110V_{AC}$ input and $220V_{AC}$ input conditions. The power factors at $110V_{AC}$ and $220V_{AC}$ condition are measured as 0.997 and 0.955, respectively.

Figure 12 shows the waveforms of the switching voltage and current, which shows the switching current waveforms following the shape of the input voltage well. The switch is turned on at zero current condition.

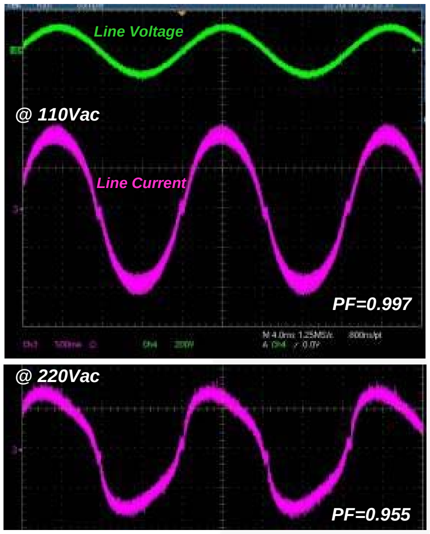
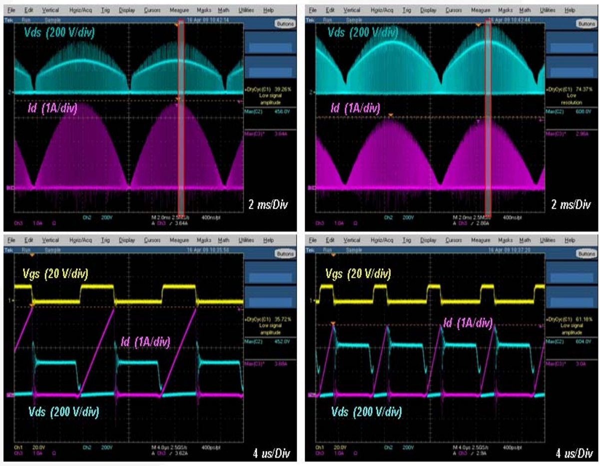


Figure 11. Input Voltage and Current



(a) at 110 V_{ac} Input (b) at 220 V_{ac} Input

Figure 12. Switching Voltage and Current

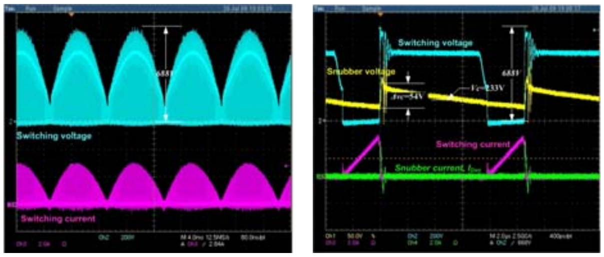


Figure 13. Drain-Source Voltage and Switching Current at 265V$_{AC}$ Input Condition

Figure 13 shows the waveforms of the drain-source voltage and current of 265V of input line voltage, the maximum input voltage, is applied. The voltage ripple is measured at 54V and the maximum voltage stress is 688V, which shows the actual results are approximately in accord with the calculation. Since the maximum voltage is 688V, 800V rating MOSFET is needed for wide input voltage range.

The efficiency characteristics according to the load variation for 110 V_{ac} and 220 V_{ac} of the input conditions are plotted in Figure 14. In the case of 110V_{ac} input, the maximum efficiency is measured as 85.17% at 45W load condition.

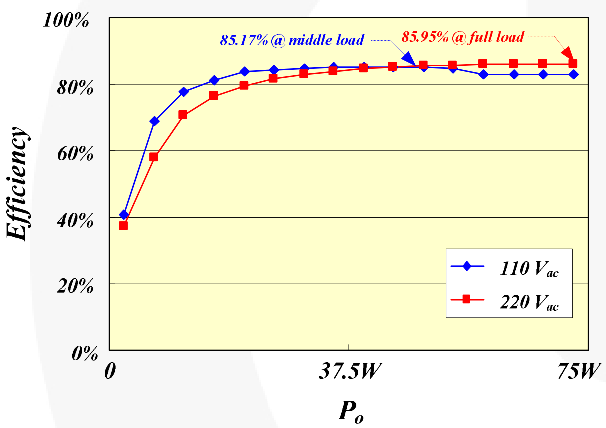


Figure 14. Efficiency Comparison

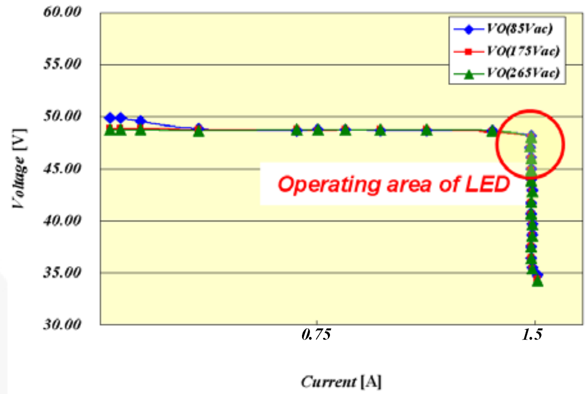


Figure 15. Output V-I Characteristic

In the case of 220V_{ac} input, the maximum efficiency is measured as 85.95% at full-load condition 75W.

In LED lighting, LED strings are driven by the rating current and the power supply should be operated under the full-load condition. Therefore, the power supply is controlled by constant current during normal condition. Figure 15 shows the *V-I* characteristics of the prototype experimental set-up. The result verifies that the output is driven well by the constant current control for whole input voltage condition.

Schematic

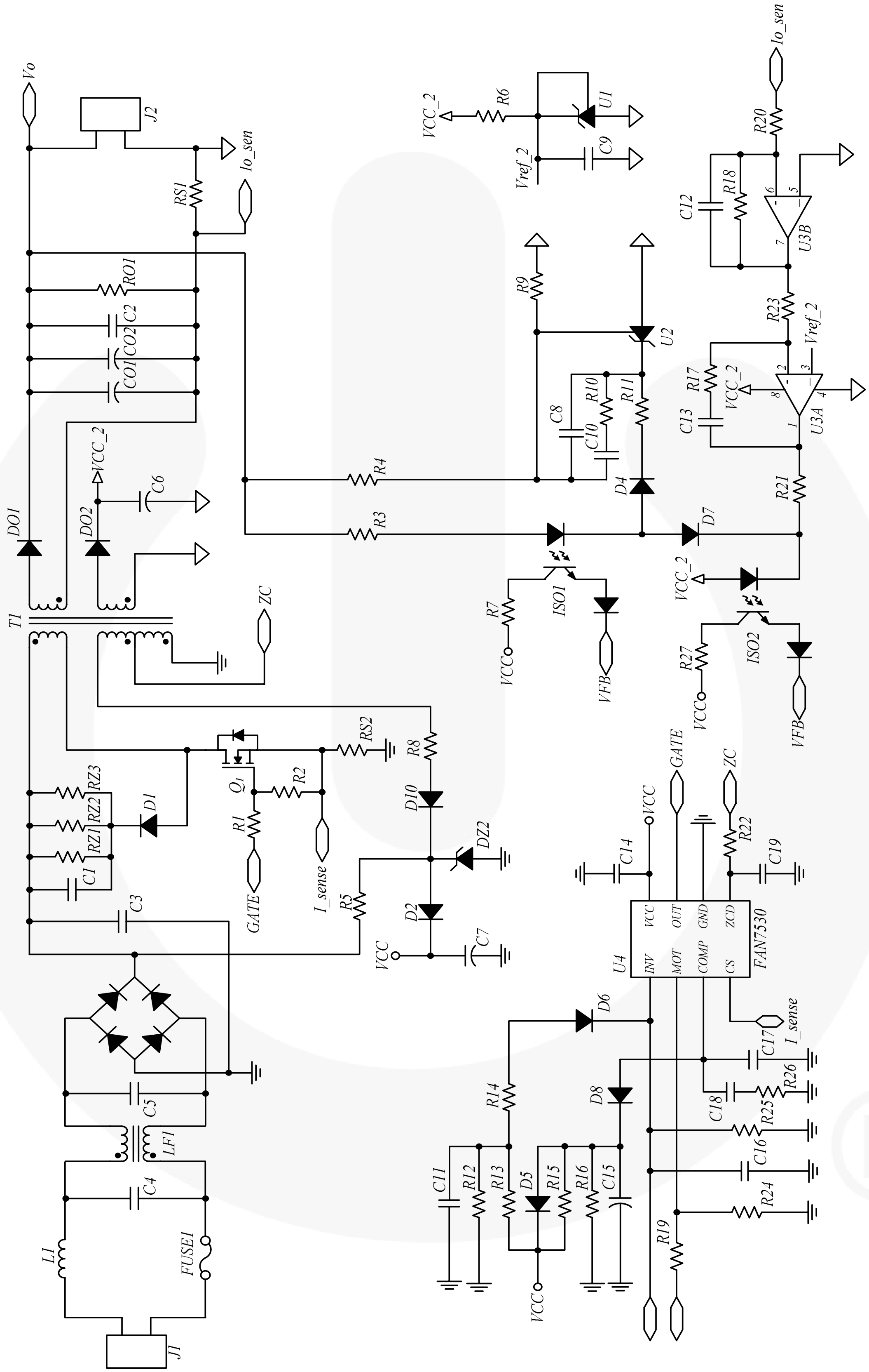


Figure 16.Schematic

Part List

Component	Symbol	Value/Part number	Component	Symbol	Value / Part Number
Rectifier	BD1	GBU8J	Resistor	RO1	56k/2W
Capacitor	CO1	1000µ/100V		RZ2	56k/2W
	CO2	1000µ/100V		RZ3	56k/2W
	C1	103/1kV		R5	56k/2W
	C2	104		RS1	0.05/5W
	C3	474/NP/630V		RS2	0.1/5W
	C4	220nF/1000V		R1	15
	C5	440nF/1000V		R2	1.5k
	C6	33µ/35V		R3	36k
	C7	33µ/35V		R4	180k
	C15	33µ/35V		R19	330k
	C8	473		R6	1.5k
	C17	473		R7	11k
	C9	105		R27	11k
	C14	105		R8	82/1W
	C10	224		R9	33k
	C11	224		R11	33k
	C18	224		R10	10k
	C12	475		R13	10k
	C13	475		R23	10k
	C16	683		R26	10k
	C19	56p		R12	1.2k
Diode	DO1	F06UP20S		R25	5.1k
	DO2	UF4005		R14	33
	D1	UF4005		R15	100k
	D10	UF4005		R16	100k
	D2	RGF1J		R17	50k
	D3	1N4148		R18	42K
	D4	1N4148		R20	1k
	D5	1N4148		R21	28k
	D6	1N4148		R22	28k
	D7	open		R24	24k
	D8	1N4148	Test point	TP1	Test point
	D9	1N4148		TP2	Test point
Zener diode	DZ2	1N4746(18V)		TP3	Test point
Fuse	FUSE1	FUSE		TP4	Test point
Opto-coupler	ISO1	817B		TP5	Test point
	ISO2	817B		TP6	Test point
Connector	J1	CONNECTOR	Transformer	T1	EER3435
	J2	CONNECTOR	Regulator	U1	KA431E
Chock-coil	LF1	EMI_CHOCK		U2	KA431E
Inductor	L1	10µH Toroidal	OP-Amp.	U3	KA358
MOSFET	Q1	FQPF8N80C	PFC IC	U4	FAN7530
Resistor	RZ1	56k/2W			

Related Datasheets

FAN7527 — Boundary Mode PFC Control IC

FAN7528 — Dual-Output Critical Conduction Mode PFC Controller

FAN7529 — Critical Conduction Mode PFC Controller

FAN7530 — Critical Conduction Mode PFC Controller