Reduction of Voltage Stresses in Buck-Boost-Type Power Factor Correctors Operating in Boundary Conduction Mode

Lars Petersen

Institute of Electric Power Engineering
Technical University of Denmark
Building 325, 2800 Lyngby, Denmark
lpe@eltek.dtu.dk

Robert W. Erickson

Colorado Power Electronics Center
Department of Electrical and Computer Engineering
University of Colorado at Boulder
Boulder, CO 80309-0425, USA

***Abstract*-In this paper a new converter is proposed for universal line PFC operated in Boundary Conduction Mode. The proposed Modified SEPIC enables the use of lower voltage rated semiconductors compared to other single-switch buck-boost derived topologies with a resulting performance comparable to the boost topology. The operation and the design procedure is described in detail and the proposed converter is experimental verified with a 210V, 100W prototype for the universal line input (90Vac-270Vac).**

I. INTRODUCTION

The Boost topology is often used for PFC applications because of its superior performance (efficiency, cost). In some cases the buck-boost topology is preferred because of the ability to generate output voltages less than the line peak voltage. This can be an advantage for the downstream converter since lower voltage rated devices and/or more cost-effective topologies can be used. The problem for the buck-boost family of converters (especially for the universal line range) is the high voltage and current stresses. Typically the voltage rating of the semiconductors are in the 800V range which impairs the performance dramatically compared to boost-type converters. [1-4]

A new converter is proposed that addresses all of the needs described above. The benefits of the proposed converter are:

- Low voltage stresses (500-600V devices)
- Single switch
- Small magnetics
- Simple control

The proposed converter is targeted for the low power range (50-200W) and operated in the Boundary Conduction Mode (BCM). The BCM operation is often preferred in the lower power range because it facilitates zero-current switch turn-on, minimizes the reverse recovery problem of the freewheeling diode and tends to reduce the overall magnetic size.

The paper will include: analysis, design guidelines, comparison with previous approaches, experimental data and a prototype schematic.

II. MODIFIED SEPIC

The standard PFC SEPIC for the univerasal line application requires high voltage (800V) semiconductors [2] which adds to the converter cost and impairs the efficiency compared to the Boost converter. The Modified SEPIC shown in Fig. 1a can be forced into operation modes where the voltage stress is reduced to a level compareable with that of the PFC Boost [5].

The major difference between the Modified SEPIC and the SEPIC is the diode D_2 added in series with L_2 in Fig. 1a. The diode effectively blocks the current path from the input through L_1, C_1, L_2 and D_2 that in normal SEPIC operation secures the volt-second balance of L_1 and L_2 by adjusting the voltage on C_1 to be equal to the input-voltage. With this diode in series with L_2, the voltage on C_1 is now govern by the power-equality ($P_{IN}=P_{OUT}$). If the inductor L_1 and L_2 is operated in DCM, the voltage on C_1 can be controlled by the inductance ratio L_1/L_2. Further more, the C1 voltage will go towards a DC-voltage if large bulk capacitors are used.

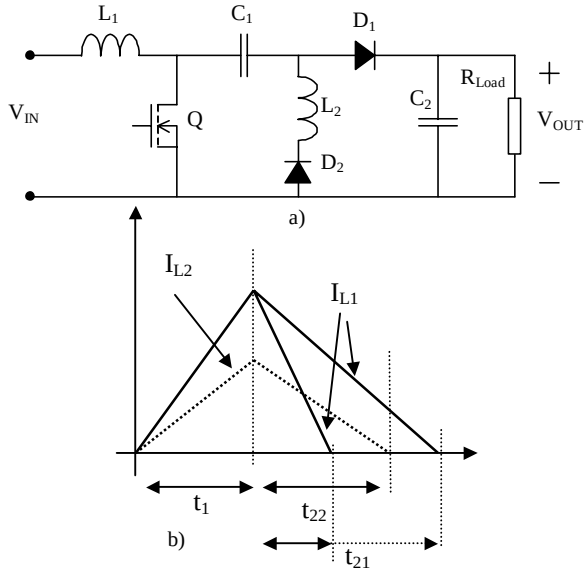


Figure 1. a) The proposed Modified SEPIC. b) Current waveforms of the inductors L_1 and L_2. Down-ramp time of the inductor L_1 is dependent on the instantaneous line voltage.

$$t_{21} = t_1 \cdot \frac{V_{IN}(t)}{V_{OUT} + V_{C1} - V_{IN}(t)} \quad (1)$$

$$t_{22} = t_1 \cdot \frac{V_{C1}}{V_{OUT}} \quad (2)$$

A. Operation modes

When operating the Boost PFC converter in BCM the following key points characterizes the operation:

- Variable frequency operation
- Small magnetic size
- Switch turned on under Zero-current condition
- Theoretical PF = 1

In case of the Modified SEPIC converter we will consider two different operation modes, both based on the BCM Boost PFC.

Mode #1:

The input section of the Modified SEPIC is similar to the boost converter so the control-method used in the BCM Boost PFC can be adopted directly. Since the PFC Boost BCM control detects zero-current in the input inductor (L_1), the zero-current condition is not always met for the current in Buck-Boost inductor (L_2). The down-ramp time of the input inductor L_1 (shown in Fig. 1b as t_{21}) determines the switch turn-on action. The zero-current switch turn-on condition is only met when t_{21} is larger than the down-ramp time of the inductor L_2, t_{22}. By manipulating (1) and (2) one can find that the zero-current switch turn-on condition is satisfied when:

$$V_{IN}(t) > V_{C1} \quad (3)$$

Mode #2:

One of the very nice features of the BCM operation mode is that the losses associated with the diode reverse recovery is greatly reduced. If this feature and the zero current turn-on of the switch is to be maintained during all operation of the Modified SEPIC-converter, current sensing in both inductors L_1 and L_2 has to be implemented. While maintaining the zero-current switch turn-on, the power factor can no longer reach the theoretical value of 1. The reason for this is that the L_1 inductor-current will no longer be in BCM when the L_2 inductor-current determines the switch turn-on. The following key points characterizes this operation mode:

- Variable frequency operation
- Small magnetic size
- Switch turned on under Zero-current condition
- Theoretical PF < 1

Since PF = 1 is not at all necessary to comply with EN61000-3-2 the operation mode #2 described above is the preferred operation, mainly because of the zero-current switch turn-on, but there are other advantages that will be explained later. The disadvantage is the implementation of the zero-current detection of L_2.

B. Steady-state analysis

In order to obtain the capacitor voltage V_{C1}, the power equality is used ($P_{IN}=P_{OUT}$):

$$P_{IN} = 2 \cdot f_{line} \cdot \sum \frac{\left(\hat{V}_{AC} \cdot \sin(\omega \cdot t)\right)^2 \cdot t_1}{2 \cdot L_1} \cdot \left(t_1 + t_{21}(t)\right) \quad (4)$$

$$P_{OUT} = 2 \cdot f_{line} \cdot \sum \left[\frac{\hat{V}_{AC} \cdot \sin(\omega \cdot t) \cdot t_1}{2 \cdot L_1} \cdot t_{21}(t) \cdot V_{OUT} + \frac{V_{C1} \cdot t_1}{2 \cdot L_2} \cdot t_{22} \cdot V_{OUT} \right] \quad (5)$$

,where t_{21} and t_{22} is defined as in (1) and (2), t_1 is the constant switch on-time.

Setting $P_{IN} = P_{OUT}$:

$$\frac{L_1}{L_2} = \frac{\sum \left(\hat{V}_{AC} \cdot \sin(\omega \cdot t)\right)^2 \cdot \left(t_1 + t_{21}(t)\right) - \sum \hat{V}_{AC} \cdot \sin(\omega \cdot t) \cdot t_{21}(t) \cdot V_{OUT}}{V_{C1} \cdot V_{OUT} \cdot t_{22}} \quad (6)$$

Using (1), (2) and (6):

$$\frac{L_1}{L_2} = \frac{\sum \left(\hat{V}_{AC} \cdot \sin(\omega \cdot t)\right)^2 \cdot \left(\frac{V_{OUT} + V_{C1}}{V_{OUT} + V_{C1} - \hat{V}_{AC} \cdot \sin(\omega \cdot t)} \right)}{V_{C1}^2} - \frac{\sum \hat{V}_{AC} \cdot \sin(\omega \cdot t) \cdot V_{OUT} \cdot \left(\frac{V_{OUT} + V_{C1}}{V_{OUT} + V_{C1} - \hat{V}_{AC} \cdot \sin(\omega \cdot t)} \right)}{V_{C1}^2} \quad (7)$$

There is no closed form solution to (7) when solving for V_{C1}, but (7) can very easily be solved numerically. For a given output voltage and line voltage, the capacitor voltage V_{C1} only depends on the inductance-ratio, L_1/L_2. This is only true because both inductors L_1 and L_2 are operated in BCM/DCM. Going into CCM operation the load will also influence the V_{C1} voltage.

III. Performance Of The Proposed Converter

For the universal line application ($90V_{AC}$-$270V_{AC}$), the maximum semiconductor stress occurs at high line ($270V_{AC}$). Fig. 2a displays the inductance-ratio as a function of the maximum voltage stress for 180V, 210V and a 240V output-voltage.

The reason for using a Buck-Boost type converter is in most cases a necessity of generating an output voltage less than the line peak voltage, typically in the area of 200V. If the semiconductor voltage stress of the Modified SEPIC

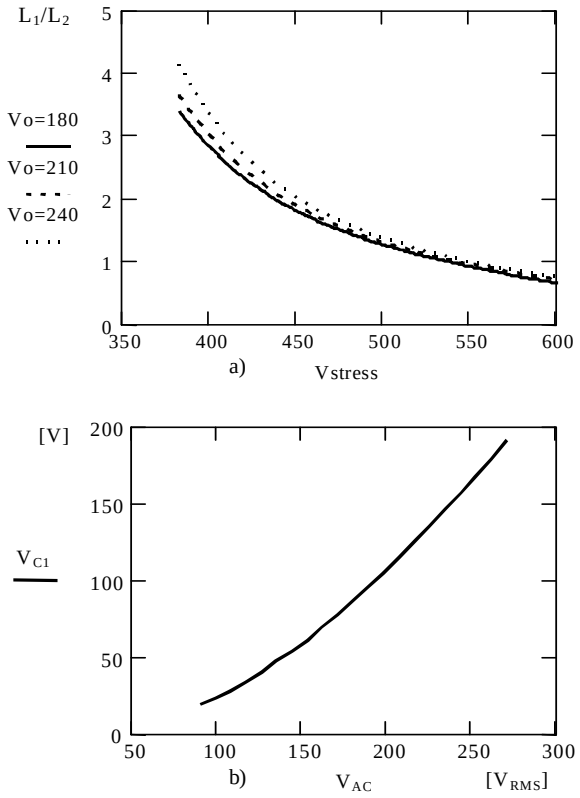


Figure 2. a) The inductance ratio as a function of the maximum semiconductor stress. b) VC1-voltage as a function of AC-line voltage, L_1/L_2=3, V_{OUT}=210V.

converter should be comparable with a boost converter (~400V) the inductance ratio value should be chosen to be in the area of 3 (Fig. 2a). This would facility the use of 500V rated semiconductors with a margin of 100V for the 100/120 Hz capacitor voltage ripple and overshoots.

Fig. 2b shows the capacitor voltage, V_{C1}, as a function of the line voltage. At low-line the V_{C1} is about 20V and increases with the line voltage to 190V at high-line.

The BCM control is a variable switching frequency control method but for the Modified SEPIC using the operation mode #2 described in section II, the frequency operation can be divided into parts:

- $V_{C1} < V_{IN}(t)$ => Variable switching frequency
- $V_{C1} > V_{IN}(t)$ => Constant switching frequency

When V_{C1} is below the instantaneous line voltage the L_1 inductor current down-ramp time determines the switch-on action, which varies with the line voltage supporting the variable frequency. When V_{C1} is above the instantaneous line voltage the L_2 inductor current down-ramp time determines the switch-on action. Since V_{C1} is considered constant the down-ramp of the L_2 inductor current will also be constant supporting constant frequency operation.

The greatest impact of the operation mode #2 is found at high line. Fig. 3a shows how the variable frequency range is

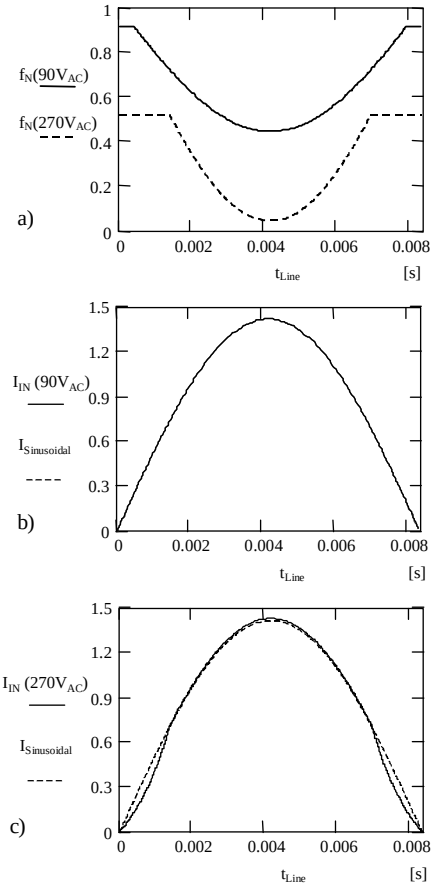


Figure 3. a) Normalized frequency with respect to the (constant) switch on-time. b) Normalized line current at V_{AC}=90V. c) Normalized line current at V_{AC}=270V.

greatly reduced compared to the operation mode #1 where the normalized frequency would go all the way up to 1. The impact of the constant frequency operation on the line current is depicted in Fig. 3c. The dashed line is the normalized ideal sinusoidal line current and one can see that the actual line current is somewhat distorted in the region of the constant frequency operation. The power obtained from the line in the area of the line voltage zero-crossing is small which only give rise to a slight increase of peak-current in the actual line current.

At low line the difference between the ideal and the actual line current is insignificant (no visual difference in Fig. 3b).

IV. Comparison

Besides the reduced voltage stress, the Modified SEPIC converter also reduces the stress on the magnetic components leading to smaller magnetic size compared to the classical SEPIC. Because of the reduced component stress the performance of the Modified SEPIC is even comparable with the BCM Boost PFC. When comparing the Modified SEPIC with the boost converter one should keep in mind the

difference in output voltage. The comparison can never be ideal because of this difference. Nevertheless the comparison is carried out to demonstrate that the increase in component stress is not that significant when choosing a medium output voltage (using the proposed topology) instead of a high output voltage (boost topology).

The comparison will include the following converters:

- BCM SEPIC [1]
- The proposed BCM Modified SEPIC
- BCM Boost [4]

The comparison is carried out assuming that the converters are satisfying a minimum switching frequency of 20 kHz and an input power of 110W. For the SEPIC and the Modified SEPIC, the output voltage is 210V, and for the Boost converter, 400V. The Modified SEPIC uses an inductance ratio of 3, so that the maximum voltage stress is 400V.

A. Inductor stress

The minimum switching frequency (20 kHz) and the Power level determines the inductor sizes for the BCM operated converters. Table 1 sums up the results for the three converters in this comparison.

	L_1	L_2	Energy storage
SEPIC	1.5mH	1.5mH	9.1 mJ
Proposed M. SEPIC	750uH	250uH	4.8 mJ
Boost	1.25mH	-	7.5 mJ

Table 1. Inductor-size comparison.

For the same minimum frequency the energy storage needed in the BCM Boost PFC converter is about 50 % larger than for the BCM Modified SEPIC PFC. Since the boost topology only uses one magnetic component compared to two in the Modified SEPIC it is not entirely fair only to use the energy storage as a measure of magnetic size - practical implementations should also be taken into account.

B. Switch stress

At high line the performance of the Boost converter is superior. However, the boost converter is incapable of producing the required 210Vdc output. At low-line the Boost converter also exhibits the lowest stress in terms of rms current-stress, but the voltage that the Boost converter is switching is still the output voltage whereas for the Modified SEPIC this voltage is almost reduced with a factor of 2. Table 2 summarizes the results.

	V_{AC} = 90V			V_{AC} = 270V		
	SEPIC	Proposed M. SEPIC	Boost	SEPIC	Proposed M. SEPIC	Boost
I_{RMS} [A]	1.74	1.61	1.21	0.74	0.75	0.2
Voltage[V]	337	229	400	592	400	400

Table 2. RMS-current- and voltage-stress.

Note that the SEPIC converter would require semiconductor devices rated at least 700V. The proposed approach can produce a 210Vdc output using semiconductor devices having same voltage rating as in a conventional boost converter.

V. PRACTICAL DESIGN CONSIDERATIONS

One of the nice features of the SEPIC converter is the inherent capability of limiting the inrush-current. The series capacitor is a relatively low value capacitor, which means that under start up conditions the capacitor will charge very fast to the line peak voltage and thereby reducing the inrush-current. Since a large capacitor is used in the Modified SEPIC converter, the issue of inrush-current has to be addressed. The following key-points have been considered during the circuit design:

- Inrush current
- Current limiting
- Zero-current detection (both L_1 and L_2)
- Output voltage measurement

A. Inrush current

In low-power boost PFC converters the inrush current during start-up is usually bypassed by a heavy-duty diode that circumvents the branch with the inductor and the fast output diode, charging the output capacitor to the line peak voltage.

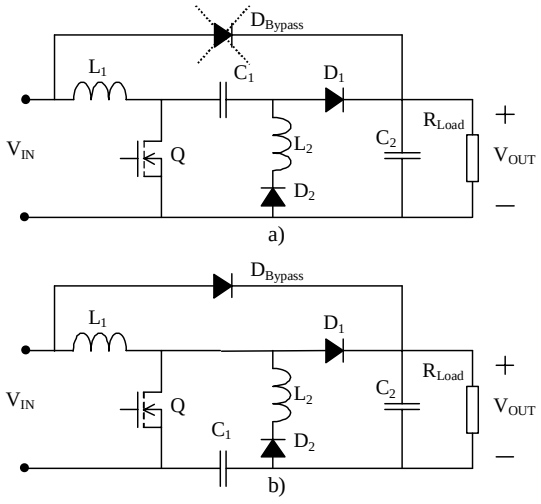


Figure 4. a) Standard inrush scheme for boost converters. b) adopted scheme for the Modified SEPIC.

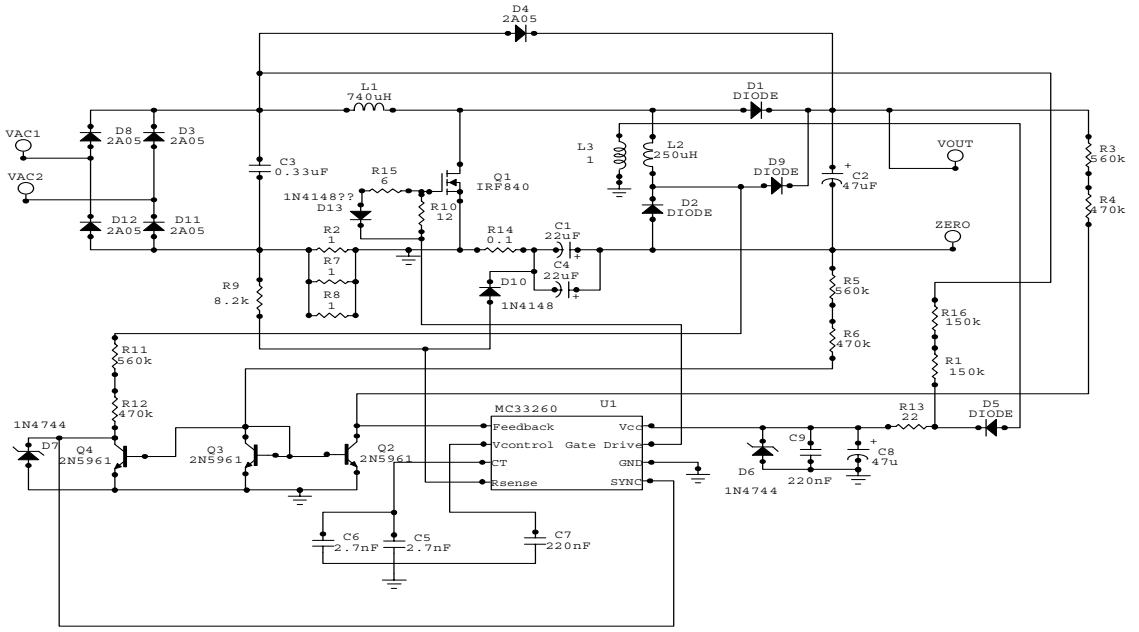


Figure 5. Circuit diagram of the proposed converter prototype.

This is done to protect the fast output diode. Since the proposed converter operates with and output voltage that can be lower than the line voltage this scheme cannot be adopted directly (Fig. 4a). To solve this problem, the capacitor C_1 is placed in the return path instead. Now it is no longer the output capacitor C_2 that is charged to the line peak voltage but both C_1+C_2 (Fig. 4b).

Using this scheme shown in Fig. 4b, give rise to another problem – measuring the output voltage.

B. Output voltage measurements

The output voltage is no longer referenced to the ground potential but biased by the C_1 capacitor voltage. In order to measure the correct output voltage a differential measurement has to be implemented.

The complete schematic of a prototype of the proposed converter is shown in Fig. 5. The control chip (MC33260) used for this prototype has an internal reference current-source that is used to control the output voltage. The output voltage is converted in to a current by the resistors R3 and R4 and compared internally with the reference current. Because of the biased output voltage a contribution from the V_{C1} voltage is added to the current through R3 and R4. This current is effectively subtracted by the current-mirror at the feedback pin (pin 1) implemented by Q2 and Q3 where the resistors R5 and R6 convert the V_{C1} voltage to the mirror current.

C. Current limiting

When the Rsense pin on the control chip (pin 4) is pulled below the ground potential (pin 6), an over current condition has occurred. This is a standard method for most BCM control ICs. For the Modified SEPIC converter an over current condition can also occur in the loop consisting of C1, D2, L2 and Q1. In order to solve this problem, a resistor, R14, is added in this loop. An over current condition can then be detected at the junction of R14 and C1 through the diode D10 connected to the Rsense pin. The control IC will react when the voltage drop over R14 becomes greater than the threshold voltage of D10.

D. Zero current detection (both L_1 and L_2)

The control IC has an extra feature intended for synchronizing the PFC converter with the down-stream dc/dc converter. When the synchronize function is enabled the gate drive is disabled until both the zero-current condition has occurred and a synchronizing signal has been detected (pin 5). For the proposed converter, the synchronizing signal is generated when the zero-current condition of L_2 occurs.

When current is flowing through L2, the potential at the junction between D2 and D9 is clamped to the V_{C1} voltage through D2. When the zero-current condition for L2 occurs, a step in this potential follows (clamped through D9 to the output voltage). An extra branch in the current-mirror consisting of R11, R12 and Q4 detects this step. Zero current detection for L1 is achieved using the standard method for BCM boost PFC (sense resistor in the return path).

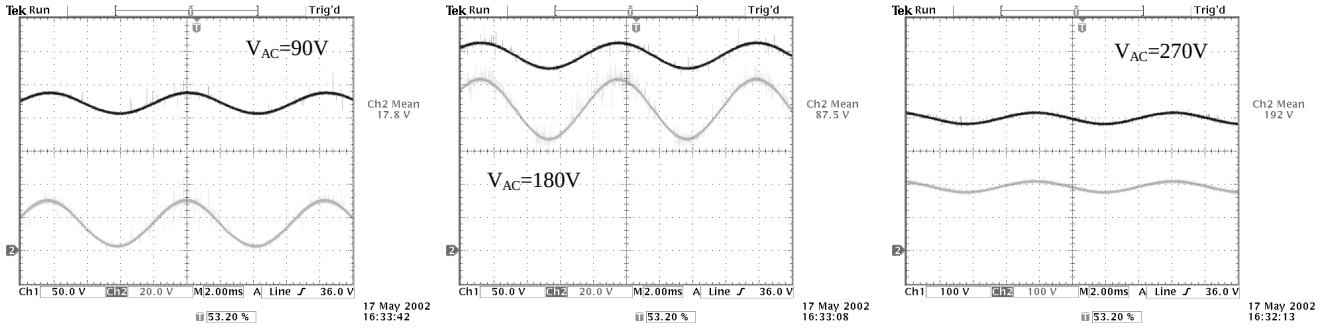


Figure. 5. V_{C1} voltage and $V_{OUT}+V_{C1}$ Voltage at V_{AC}=90V, 180V and 270V

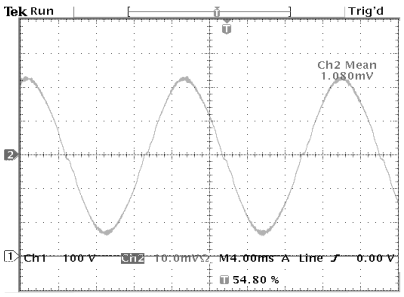
	Measured data		Theoretical data	
V_{AC}	V_{C1} (Mean)	Max. Voltage stress	V_{C1} (Mean)	Max. Voltage stress
90V	18V	240V	19V	229V
180V	88V	315V	86V	296V
270V	192V	420V	190V	400V

Table 3. V_{C1} capacitor voltages and Maximum semiconductor voltages. Measured and theoretical data.

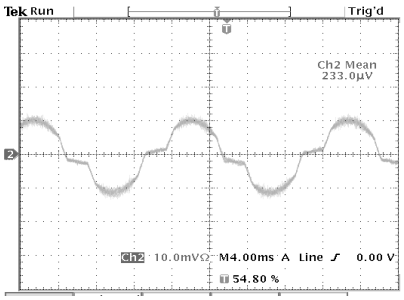
VI. Experimental Results

A 210V, 100W prototype for the universal line input (90Vac-270Vac) has been tested to verify the performance of the Modified SEPIC. The full circuit schematic is shown in Fig. 5.

In the steady-state analysis it is assumed that the capacitor voltage V_{C1} is constant during the line period. This is not through at low line voltage where the V_{C1} voltage has a very large ripple (±16V!) compared to the DC value (18V) (Fig. 5).



a)



b)

Figure 6. Experimental line currents. P_{OUT}=100W. a) V_{AC}=120V, PF=0.998, THD=5.8%. b) V_{AC}=270V, PF=0.968, THD=22.5%.

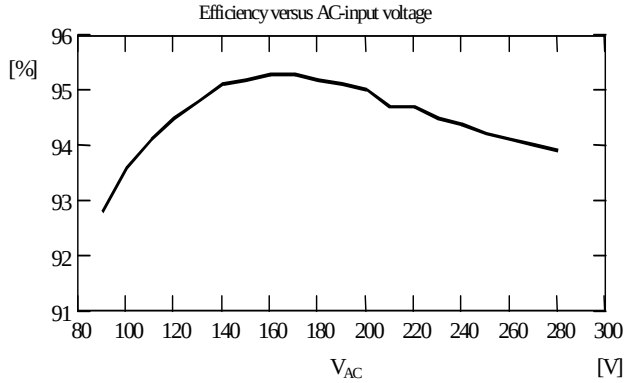


Figure 7. Efficiency of the experimental converter as a function of the AC-line voltage.

This ripple will cause a slight decrease in PF and an increase in the switch rms-current but the large ripple voltage has little effect on the overall converter performance.

The line current distortion at high line is larger than expected by theoretical predictions. This is due to the fact the energy is transferred back to the input when the L_2 inductor current down-ramp time is larger than the L_1 inductor current down-ramp time. The energy is stored in the capacitance present at the rectifier-bridge at a voltage equal to the $V_{OUT}+V_{C1}$ voltage.

The efficiency of the prototype for the full line range is shown in Fig. 7. Compared to other single-switch buck-boost type PFC converters reported in the literature, the efficiency achieved with the proposed converter is significantly higher (e.g. [1]). Normally the buck-boost type converters achieve efficiencies in the range of 80-90%.

The worst-case efficiency of 92.8% is achieved at low line ($90V_{AC}$). In the area where the peak line voltage is close to the output voltage the performance is very good achieving efficiencies of over 95%. At high line the efficiency drops again, mainly because of the higher switching losses.

CONCLUSION

The BCM Modified SEPIC PFC converter is analyzed and experimental verified. The voltage stress can be reduced to a level comparable with the Boost PFC converter facilitating the use of low voltage rated semiconductors compared to other single-switch Buck-Boost derived converters. While the rms-current stress is still higher in the Modified SEPIC converter compared to the Boost converter, the switching stress is comparable. Comparing the magnetics of the above converters shows that the Boost converter needs more magnetic storage capability than the Modified SEPIC.

The efficiency achieved with the experimental converter is comparable with the performance of the Boost converter but superior to other single-switch Buck-Boost derived converters.

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