Introduction

The ZVS (Zero Volt Switching) full-bridge topology has been around for many years and has become the industry's workhorse. Despite its many advantages, the topology does present the designer with some interesting challenges. One of the drawbacks to this topology is the complex gate drive required to produce the correct switching waveforms. This has been resolved with Intersil products such as the ISL6752 and ISL6753.

Another challenge is the limited load range over which zero voltage switching can be achieved. An ambitious design can achieve ZVS down to 50% of maximum load. However, there are techniques that will help improve the ZVS operating range down to as low as 10% of maximum load current. These techniques will be discussed here.

Scope

This design guide provides techniques for improving the zero voltage range on the ZVS full-bridge converter. These methods require minimal hardware modification and provide significant circuit improvements not just in zero voltage switching but in other areas, such as reducing common mode currents and limiting the voltage stress of the output diodes. Also this design guide provides some helpful circuit applications.

Energy and Resonance

The key to zero voltage switching is the amount of energy stored in the transformer inductance versus the energy required to charge and discharge the circuit capacitances. Increasing the stored energy in the inductance or reducing the capacitance, will allow the design to ZVS at lower output currents.

The amount of energy stored, E, is:

$$E = \frac{1}{2}L_{RES}I^2 \tag{EQ. 1}$$

where L_{RES} is the effective resonant inductance of the transformer and I is the current through the effective resonant inductance. This inductance can be as low as the leakage inductance or as high as the reflected output inductance, depending on the technique employed. Details will be discussed in a later section.

The energy needed for ZVS is required at the end of the free-wheeling cycle or just prior to the start of the power transfer cycle. The transformer primary voltage and current is shown in Figure 1. The free-wheeling current occurs between time T0 and T1. It is at time T1 when the energy for ZVS is required. In a normal full-bridge, this current is zero because all the switching devices are off during the free-

wheeling time. However, in a clamped primary topology such as the ZVS full-bridge, current can continue to flow during the free-wheeling mode. At time T1, when the primary clamp is released, the circulating current will continue to flow and charge/discharge the MOSFET capacitances and other parasitic capacitances.
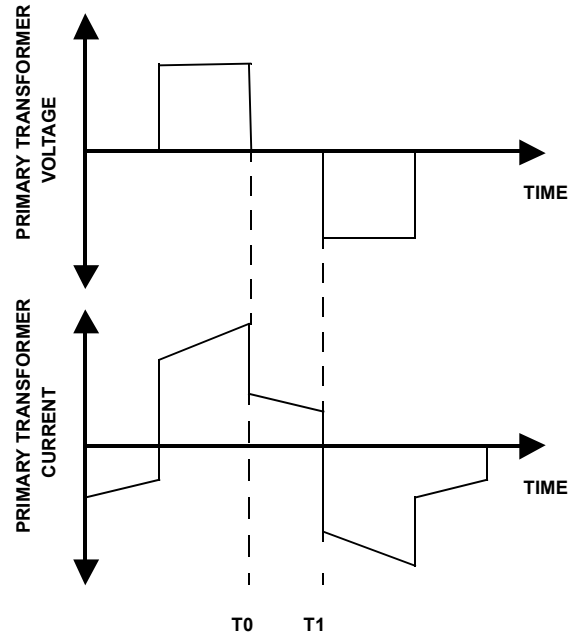

FIGURE 1. TRANSFORMER VOLTAGE AND CURRENT

There are three key techniques that can be used to improve ZVS performance:

- Reduce the capacitance

- Increase effective transformer resonant inductance

- Increase the free-wheeling current at time T1

Since the capacitance and transformer resonant inductance will be modified when using these methods, the resonant transition duration that occurs at time T1 will change.

The time duration of the resonance is determined by the charging and discharging of the upper and lower MOSFET parasitic capacitors. This capacitance is a function of the drain to source voltage and is known as C_{OSS} (the gate-drain plus the drain-source capacitance). Information about C_{OSS} can be found in the device manufacturer's data books. Since the capacitance is a function of voltage, an average capacitance, C_{AVG}, will be used and is defined as:

$$C_{AVG} = \frac{1}{V_B} \int_0^{V_B} C_{OSS}(v)dv \tag{EQ. 2}$$

where V_B is defined as the supply voltage to the ZVS full-bridge converter. Since the upper and lower MOSFETs must charge and discharge, the total capacitance is twice C_{AVG}. Therefore, the resonant frequency may be estimated by:

$$F_{RES} = \frac{1}{2\pi\sqrt{2L_{RES}C_{AVG}}}$$ (EQ. 3)

Because the MOSFET turns on after 1/4 of the cycle (π/4 radians), the turn-on delay time is:

$$T_{DELAY} = \frac{1}{4F_{RES}} = \frac{\pi\sqrt{2L_{RES}C_{AVG}}}{2}$$ (EQ. 4)

Equation 4 shows that if either the resonant inductance or capacitance of the MOSFETs increases, the resonant time will also increase. This delay reduces the range of usable duty cycle and must be taken into account in maximum duty cycle calculations. It is preferable to have a small resonant time.

In 400V designs, the resonant time is typically 300ns and in 48V units the time is 100ns. It is advisable to increase the inductance for energy storage and reduce the capacitance for resonant time and energy requirements.

Another reason for increasing the L_{RES}/C_{AVG} ratio is to improve the minimum load current to achieve ZVS operation. The amplitude of the resonant voltage on the transformer depends on the current in the inductance and the LC network's characteristic impedance, which is the ratio of the inductance over MOSFET capacitance. This equates to:

$$V_{RES} = I_{PRI}\sqrt{\frac{L_{RES}}{2C_{AVG}}}$$ (EQ. 5)

where I_{PRI} is the current through the transformer primary and V_{RES} is the voltage across the transformer during the resonant time. As the primary current, I_{PRI}, increases due to an increase in the load, the resonant voltage amplitude increases until it is clamped by the bulk voltage, V_B. I_{PRI} will then flow through the MOSFET's channel or body diode. Note that it is desirable to have the characteristic impedance value as large as possible so that low values of primary current will produce $V_{RES} > V_B$ to achieve ZVS. For design purposes, the effective resonant inductance of the transformer should be high as possible, but not so high as to be detrimental to the resonant time, and the MOSFET capacitance should be kept to a minimum.

Note that by setting V_{RES} equal to V_B and solving for I_{PRI}, the minimum reflected load current at which the converter will ZVS can be estimated.

Now that a basic understanding of the ZVS topology has been established, techniques for improving the performance can be discussed.

Transformer

Every time the voltage across the primary winding of the transformer changes, the transformer winding capacitance must be charged or discharged. Not only does this decrease the available energy for ZVS but it is also a source of common mode currents which contribute to EMI emissions.

What can be done is to add more insulation tape between the primary and secondary windings. Doubling or tripling the insulation thickness will not increase the overall transformer size by much. By doing this, the leakage inductance is increased and the load current to maintain ZVS is lowered. The common mode currents may be decreased by 1/2 to 1/3, depending on the tape thickness.

Unlike other topologies, leakage inductance is beneficial in the ZVS full-bridge. Higher leakage energy results in more losses in the primary side snubbers in a standard full-bridge. The higher energy is desired in the ZVS full-bridge.

Arbitrarily increasing the leakage inductance may have detrimental effects as well. One concern is eddy currents in the transformer windings due to high H fields [1]. If the H fields get too high, the primary and secondary windings should to be interleaved to reduce AC winding losses.

Another transformer modification that can be done is to gap the transformer core. This decreases the magnetizing inductance and increases the magnetizing current, thereby increasing the energy stored. Even a small gap will improve the ZVS performance since the energy stored is proportional to I^2. Gapping the core will help to improve ZVS slightly, and yield other benefits as well

- By gapping the core more than 2mils, the variation in magnetizing inductance from unit to unit can be significantly reduced. When putting 2 core halves together, a gap of anywhere from 0 to 2mils may be formed due to uneven mating surfaces.

- If the supply voltage to the converter is regulated, such as the output of a PFC, the core may be gapped to the obtain the correct magnetizing current for the desired slope compensation.

The draw back with gapping the core is the slight increase in primary current and conduction losses of the MOSFETs.

MOSFETs

Another opportunity to reduce capacitance is to use lower capacitance MOSFETs. It is often tempting to use low R_{DSON} MOSFETs to minimize conduction losses. However, a low R_{DSON} MOSFET will have high capacitances that will hurt the minimum load at which the converter will ZVS. Because of the high capacitance, switching loss can become an issue at light loads where ZVS does not occur.

Figure 2 shows such an example. MOSFET #1 is a low R_{DSON}, high capacitance MOSFET. MOSFET #2 has twice the R_{DSON} and half the capacitance, or ½ the die size. In

this example, MOSFET #1 design will no longer ZVS below 5A. You will note that at 0A load, the MOSFET power loss is higher than the power loss at full load. This happens because the switching loss can be higher than the conduction loss. In conventional full-bridge converters, the power loss curve is monotonic and higher in value because the power loss is always the sum of conduction + switching loss. This is not the case in ZVS full-bridges. In this example, a design with MOSFET #1 will dissipate 15W more than at no load than at full load.
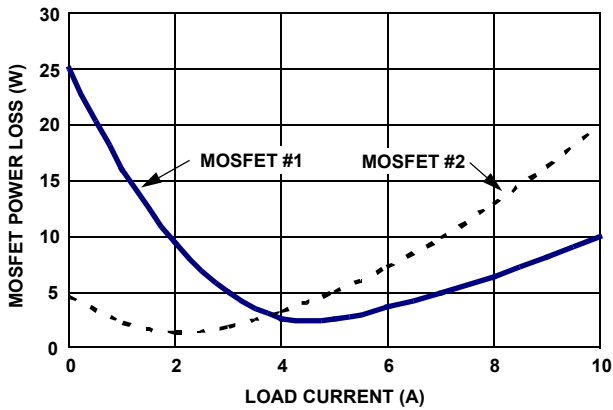
FIGURE 2. MOSFET POWER LOSS

MOSFET #2 has higher conduction losses at full load but lower switching loss at light loads. Also note that switching loss does not become an issue until the load current drops below 3A. The lower capacitance requires less energy to achieve ZVS. Even though the conduction loss is higher at 20W, it is less than the 25W maximum loss using MOSFET #1. When one considers maximum losses, it is apparent that a design using MOSFET #2 would yield superior thermal performance.

Saturable Cores

One of the key ZVS full-bridge innovations is the use of saturable cores to improve the ZVS operating range, and to dampen ringing on the output diodes. The following circuit shows the placement of the saturable cores on the output.
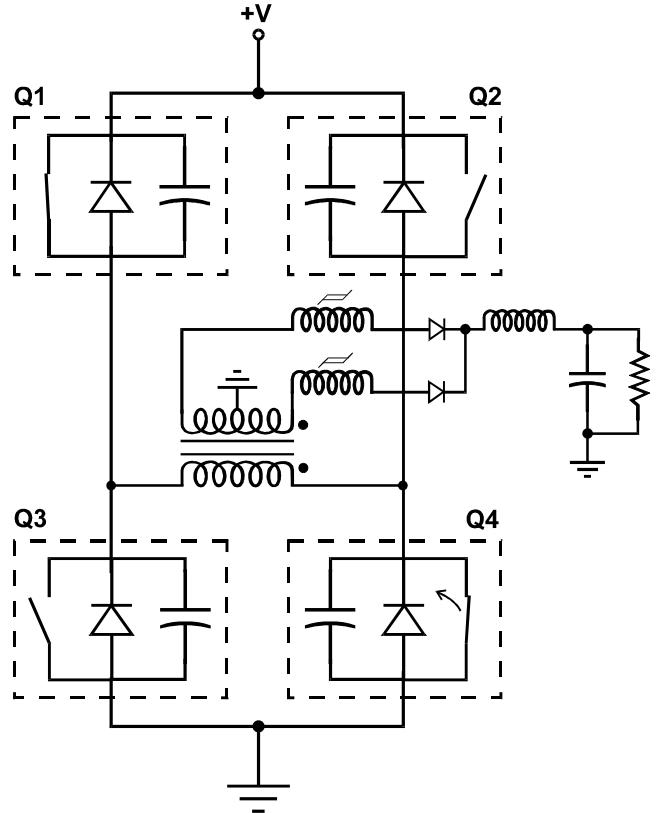

FIGURE 3. CIRCUIT WITH SATURABLE CORES

To understand how saturable cores work and their effect in improving ZVS operation, a background in the behavior of magnetic material will be discussed first.

Theory

All magnetic material exhibits a characteristic B-H loop which illustrates the relationship between the magnetic field strength, H, and the flux density, B. The slope of the B-H loop is the permeability.

When used in this application, the saturable core's B-H loop is typically operated in one quadrant, as shown below.
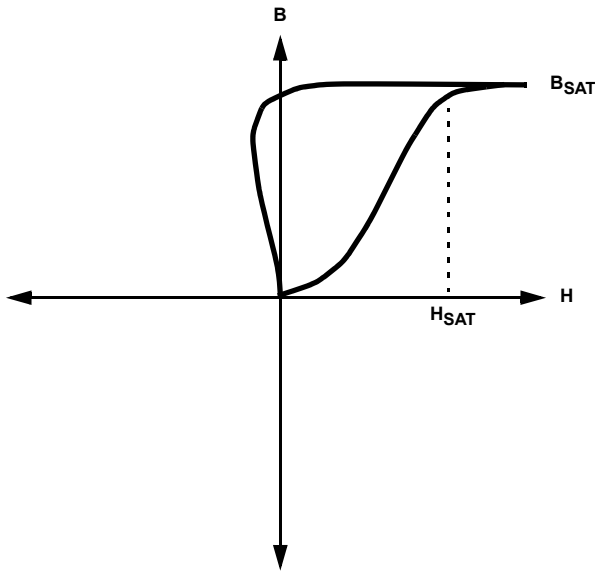

FIGURE 4. B-H LOOP

As the magnetic field strength, H, increases from zero, the flux density, B, increases until a saturation point occurs known as B_{SAT}. When B_{SAT} is reached the permeability of the material reduces to μ_0, the permeability of free space. B_{SAT} occurs at H_{SAT}. As H continues to increase, B increases at a much reduced rate, determined by μ_0. In this state the material is saturated.

Now, if H drops, B does not decrease significantly until H becomes slightly negative and then the core starts to reset. The value of H required to reset (demagnetize) the core is known as the coercivity or H_C.

Based on this information, a simplification can be made. If H < H_{SAT}, the permeability (μ = B/H) is high and if H > H_{SAT}, the permeability is low, as shown below:
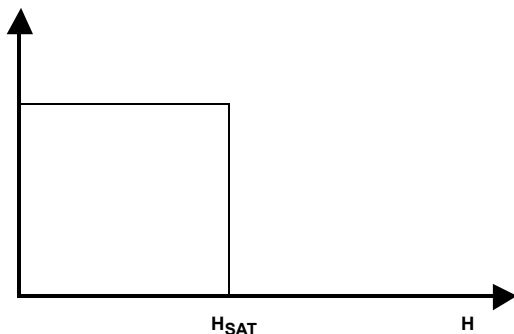

FIGURE 5. PERMAEBILITY vs H

Since inductance is directly related to permeability, the inductance also varies with H. However, the inductance also depends on the physical shape of the core and its magnetic

properties. Currently only toroidal shaped cores are used because of their ease in winding and lower cost. A drawing of a saturable core is shown in Figure 6.
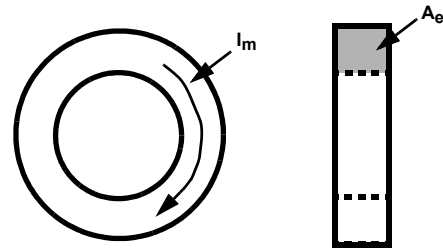

FIGURE 6. SATURABLE CORE GEOMETRY

There are a couple important core parameters to consider. One is l_m, the mean magnetic path length of the core, and the other is the effective cross sectional area, A_e. The inductance for a toroidal shaped core is:

$$L = \frac{\mu(I) N^2 A_e}{l_m} \qquad \text{(EQ. 6)}$$

where $\mu(I)$ indicates that μ is a function of I. The core permeability has 2 states and because of this, the inductance has two states. The relationship between H and I is:

$$H = \frac{I \times N}{l_m} \qquad \text{(EQ. 7)}$$

where I is the current and N is the number of turns. The current magnitude that saturates the core is then:

$$I_{SAT} = \frac{H_{SAT} \times l_m}{N} \qquad \text{(EQ. 8)}$$

The permeability of the core with zero or low bias will have a high μ while at currents above I_{SAT}, μ drops to μ_o. The inductance as a function of current is illustrated in the figure below:
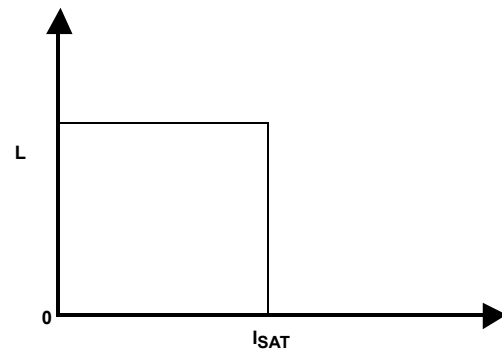

FIGURE 7. INDUCTANCE vs I_{SAT}

Figure 7 shows that when I < I_{SAT}, the inductance is high and when I > I_{SAT}, the inductance is near 0.

The core characteristics can now be used to understand core operation in a circuit. When a voltage is first applied to the core, the current ramps up. During this time the core is in

a blocking state. It behaves as a high impedance or a very large inductor. When the current reaches I_{SAT}, the inductance drops to approximately zero henries and the impedance becomes very low. If there are any other impedances in the circuit, the applied voltage will drop across these components and the voltage across the core drops to nearly zero volts. The following figure graphically shows this effect.
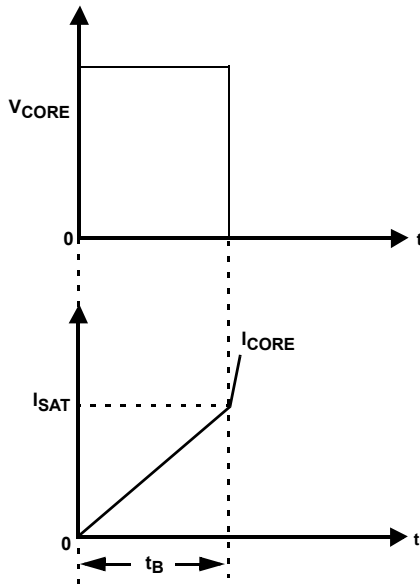

FIGURE 8. BLOCKING CHARACTERISTICS

The saturable core acts as a high impedance (switch open) until the current has ramped up to I_{SAT}. The period of time that the core remains in a high impedance state is known as the blocking time, t_B. Also note, from Faraday's Law, that magnetic cores have a constant volt-time characteristic. If the voltage applied to the core (V_{CORE}) is increased, the blocking time decreases proportionally such that the volt-time product is always constant. The reason for this is that if V_{CORE} increases, so does the rate of current rise so that less time is needed to reach I_{SAT}.

The relationship between voltage, current and time is quite simple. For $I < I_{SAT}$, the saturable core behaves like an inductor:

$$V = L\frac{dI}{dt} \qquad (EQ.\ 9)$$

The applied voltage is known, dI is simply I_{SAT} and dt is the blocking time, t_B. Solving for t_B results in:

$$t_B = \frac{L \times I_{SAT}}{V_{CORE}} \qquad (EQ.\ 10)$$

Substituting L and I_{SAT}:

$$t_B = \frac{1}{V_{CORE}} \times \left[\frac{\mu N^2 A_e}{l_m}\right] \times \left[\frac{H_{SAT}\ l_m}{N}\right] \qquad (EQ.\ 11)$$

Simplifying the equation:

$$t_B = \frac{1}{V_{CORE}} \times [A_e N] \times [H_{SAT}\mu] \qquad (EQ.\ 12)$$

This equation describes the blocking time as a function of the applied voltage (V_{CORE}), the core geometry and turns ($A_e N$), and the magnetic material property ($H_{SAT}\mu$). There are some interesting relationships revealed by Equation 12. First, the blocking time has nothing to do with the mean magnetic length, l_m. For a given material, varying the number of turns or the area of the core affects the blocking capability. Different materials have different $H_{SAT}\mu$ values. For example, J and W material from Magnetics Inc.[2] have the same $H_{SAT}\mu$ value, yet R material is quite different. Equation 12 is an approximation, and as such, is more useful for exploring relative relationships. It was derived assuming a constant applied voltage when in fact the voltage waveform is more complex. Even though Equation 12 may not predict the exact blocking time, it will show what parameters to vary to change the blocking time.

The next issue requiring discussion is how the core gets reset. From the B-H loop for the materials being discussed, if H does not go negative to reset the core, the core will always be in a saturated state. The core reset is directly related to the reverse recovery characteristics of the rectifier used.

In the circuit, there is a small amount of reverse charge (or current) to reset the core when it's placed in series with the diode. This reverse current results from discharging the diode capacitance (Schottky) or junction charge during turn-off. This current resets the core to some point so that a minor loop can be formed. Assuming there is sufficient reverse current to equal $-H_C$, the degree of reset depends on the voltage applied to the core winding and the duration for which it is applied. While the core is being reset, the reverse current must equal the value of current corresponding to $-H_C$. This behavior softens the reverse recovery characteristics. It should be noted that H_C is not a fixed value, but is dependent on the core permeability and the rate of change of the flux. The degree of core reset, therefore, depends on the stored charge in the diode junction.

It has been found that Magnetics Inc. W and J material offer excellent blocking characteristics. However, materials such as R or Metglas® FT-3 and 2714A materials (Metglas, Inc./Hitachi) do not reset with typical Schottky diodes and thus stay in a saturated state. The reason for this is that the reverse current is not high enough or on long enough to fully reset the core because these cores have a higher H_C than either W or J material. Therefore, the core does not form a minor loop. This effect has been seen when using Schottky, GaAs or SiC diodes. For PN diodes, the effect is quite different. These diodes have a high reverse recovery charge. This reverse recovery charge is directly proportional to the forward current at which the diode operates. As the forward current increases through the diode, the saturable

core resets deeper and the B-H loop increases. Of course, an increase in B-H loop area means increase in power dissipation. It also means that the blocking time increases with the forward current. Neither of these effects are desirable. It's not recommended that PN diodes be used with saturable cores unless they have very good reverse recovery characteristics.

For low voltage designs both t_B and P_{CORE} are proportional to the number of turns. However, at higher voltages an interesting phenomenon occurs. Core loss is also dependent on the diode used. Core loss is defined as:

$$P_{core} = f \int_0^\tau B \times H \, dt = f \times \frac{1}{\mu} \int_0^\tau (\Delta B)^2 \, dt \qquad \text{(EQ. 13)}$$

where f is the switching frequency, ΔB is defined as the change in flux density of the minor loop. The reset current determines how far the core resets. As reset current goes up, ΔB increases. This has an effect on blocking, such as:

$$V_{CORE} \times t_B = NA_e \Delta B \qquad \text{(EQ. 14)}$$

The reset current changes because the dv/dt applied to the diode changes due to the inductance of the core. So, as N increases, the inductance increases, the reset current decreases and so does ΔB. Thus, with N going up and ΔB going down, V_{CORE} x t_B (volt-time) is not easily predicted.

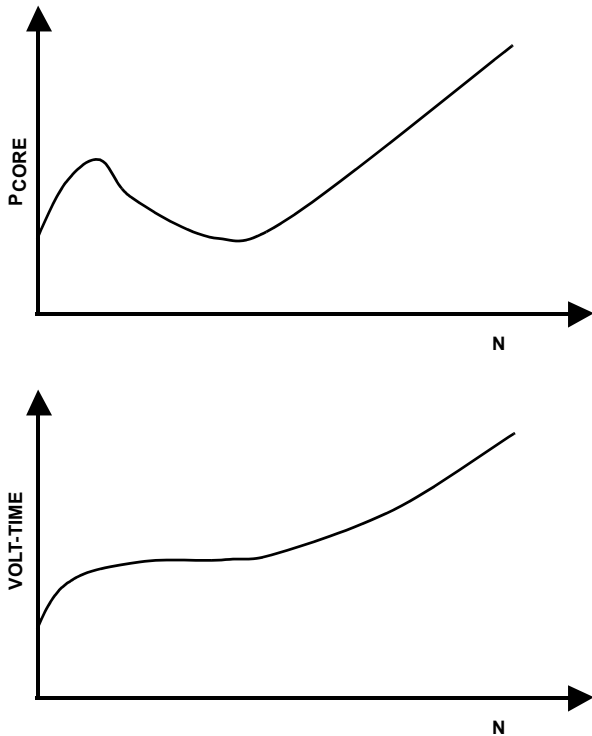The following figure shows the results of experimentation with 48V output units.

FIGURE 9. CORE LOSS, BLOCKING TIME EFFECTS WITH NUMBER OF TURNS

It shows that changing turns in a certain region of operation will have little effect on blocking time but a major effect on core loss. This is something to consider for higher output voltage designs.

Behavior of Saturable Cores in Circuit

The saturable cores behave as switches in the ZVS full-bridge topology steering the secondary current to maximize the primary current during free-wheeling. In a standard full-bridge the output inductor current is split into each secondary winding during the free-wheeling time and there is no primary current. In the ZVS full-bridge the secondary will be directed to one side only. The following figures will step through each mode of operation to show how the saturable core behaves.

On Mode 1

For On Mode 1, known as the power transfer cycle

- Q1, Q4 is on
- Q2, Q3 is off
- L1 is reset (high impedance)
- L2 is saturated (short)

The current is flowing through the channels of Q1 and Q4. The transformer has the full supply voltage across it. Due to the secondary voltages, all the secondary current will flow through L2 and current is blocked by the series diode for L1.
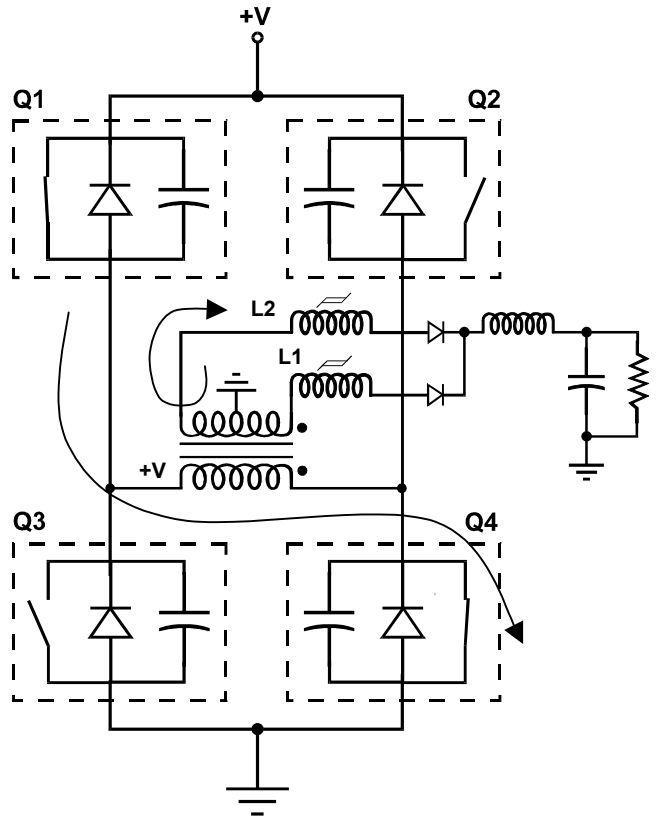
FIGURE 10. ON MODE 1

Free-wheeling Mode

For the Free-wheeling Mode

• Q1 is on

• Q2, Q3, Q4 is off

• L1 is reset (high impedance)

• L2 is saturated (short)

The current is flowing through the channel of Q1 and the body diode of Q2. The transformer has approximately 0V across the primary winding. The secondary winding voltage is also at 0V, and the secondary side free-wheeling current continues to flow through L2. L2 is in a saturated state while L1 still remains in a reset state (high impedance). There is not enough voltage across L1 to ramp the current up and saturate the core. During this time, the primary side free-wheeling current will be the reflected output inductor current plus magnetizing current.

Resonant Mode

For the Resonant Mode

• Q2 is on

• Q1, Q3, Q4 is off

• L1 is blocking (high impedance)

• L2 is saturated (short)

The current continues to flow in the primary and secondary windings. The primary current charges the capacitance of Q1 and discharges the capacitance of Q3. At the node of Q1 and Q3, the voltage is decreasing and the voltage across the transformer is reversing polarity. The voltage is also reversing polarity on the secondary. As the voltage reverses, the voltage across L1 will increase and remain in a blocking state until saturated. During this time the output inductor current continues to flow through L2 and assists the ZVS transition.

As L1 saturates, the voltage across L1 decreases, a reverse voltage across the diode in series with L2 develops and the output inductor current transfers from L2 to L1. Just as the voltage across the diode in series with L2 reverses, the reverse recovery current from the diode resets L2. After which L2 is fully reset and L1 is saturated.

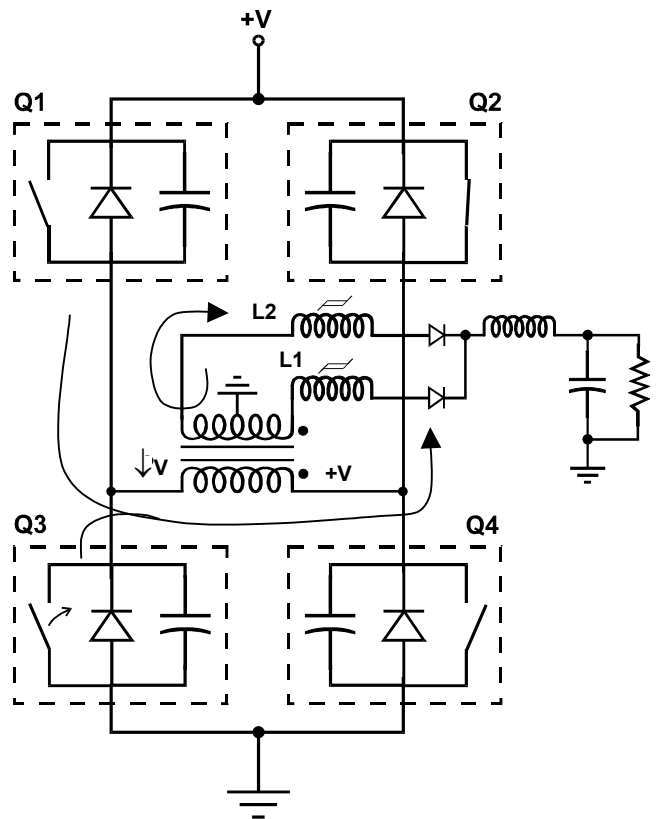FIGURE 11. FREE-WHEELING MODE

FIGURE 12. RESONANT MODE

This is the key mode where the highest current in the primary is required to charge and discharge the capacitance for ZVS operation. The saturable cores help steer the current to achieve this by keeping the primary current as high as possible.

On Mode 2

For On Mode 2, the other power transfer cycle

- Q2, Q3 is on

- Q1, Q4 is off

- L1 is saturated (short)

- L2 is reset (high impedance)

The current is flowing through the channel of Q2 and Q3. If there is excess ZVS energy, as there will be for all loads that exceed the minimum load for which ZVS occurs, the primary current direction must be reversed before power transfer to the secondary can occur. The delay this introduces causes the reduction of effective duty cycle mentioned earlier. L1 has gone past its blocking state and is now saturated. L2 has now completely reset and is in a high impedance state.
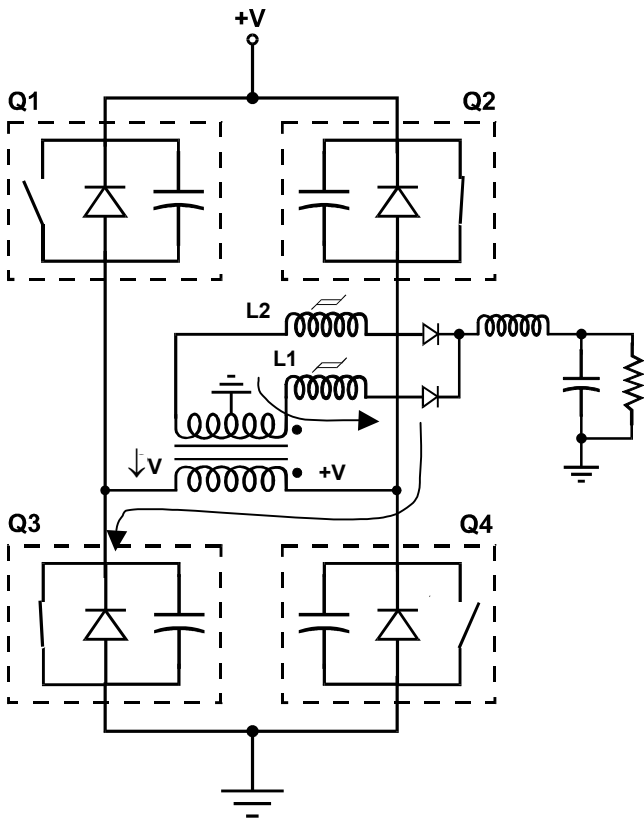

FIGURE 13. ON MODE 2

Once the saturable cores are added and they have the correct blocking time, there will be a noticeable change in the primary waveforms as shown in the following figure.
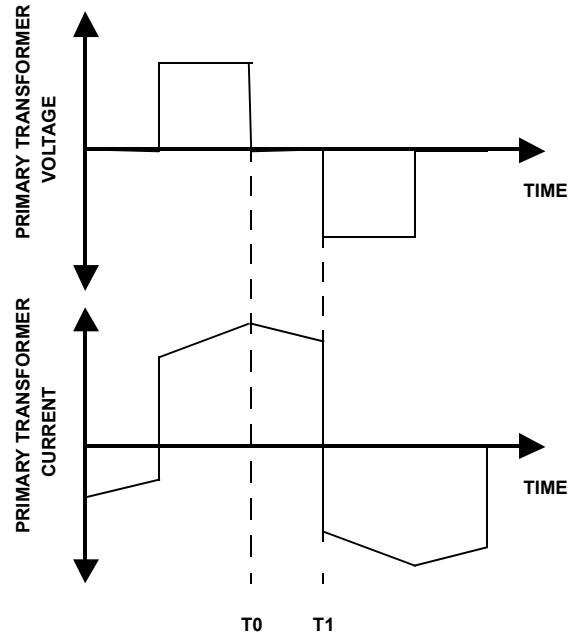

FIGURE 14. PRIMARY WAVEFORMS WITH CORES

Since all the secondary current is flowing through one side of the secondary winding, the primary free-wheeling current is just the output inductor reflected to the primary plus magnetizing current. There's a significant increase in energy at time T1 for ZVS. Also note that the output inductor size has an effect on the primary side free-wheeling current. A higher inductance will help ZVS.

Resonant Inductance

Adding the saturable cores also effect the resonant inductance. The resonant transition time is normally based on the leakage inductance of the transformer, but adding the saturable cores changes that. The following figure shows the equivalent circuit during the resonant mode.
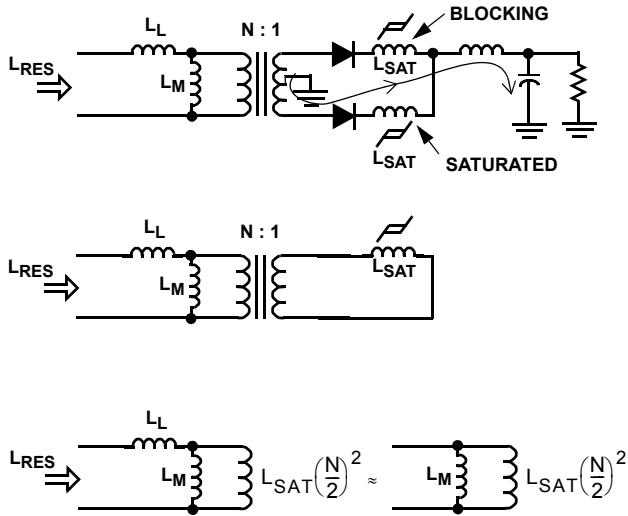
FIGURE 15. RESONANT MODE EQUIVALENT CIRCUIT

The circuit shows an ideal transformer with N:1 ratio. The leakage and magnetizing inductance are represented as discrete components on the primary side. The output section is a center tap with diodes, saturable cores and an output filter. During the resonant mode, one core is blocking and the other is in a saturated state. Most of the secondary transformer voltage will be across the saturable core in the blocking state. Both diodes are on except one will be conducting most of the current. With that in mind, both diodes and the saturated core can be redrawn as short circuits. This then simplifies to the circuit as indicated in the middle circuit of Figure 15. Further simplification can be made by reflecting all the circuit elements to the primary. Since the magnetizing inductance, L_M is much greater than the leakage inductance L_L ($L_M \gg L_L$), the circuit can further simplify down to magnetizing inductance in parallel with the inductance of the saturable core in a blocking state reflected to the primary. Even further simplification can further be made if the reflected saturable core inductance is much greater than the magnetizing inductance. Now the magnetizing inductance L_M, becomes the resonant inductance, L_{RES}. This significantly increases the stored energy. It is not uncommon to achieve ZVS at 10% of maximum load using this technique with saturable cores.

The following equation describes the resonant inductance.

$$L_{RES} = \cfrac{1}{\cfrac{1}{L_M} + \cfrac{1}{L_{SAT}\left[\frac{N}{2}\right]^2}} + L_L \qquad \text{(EQ. 15)}$$

This shows that depending on the saturable core's inductance, the resonant inductances can vary from the leakage inductance to the magnetizing inductance of the transformer. Since the resonant inductance increased, there will be an effect on the resonant delay (increasing it), and the

MOSFET timing must be adjusted accordingly. The increased delay will also reduce the effective maximum duty cycle, but the added performance is well worth the trade off.

Output Diode Snubbers

If the proper saturable cores are chosen, RC snubbers are not required. The energy required to dampen the secondary can be found by taking advantage of the core loss of the saturable cores. Also, using the saturable cores as snubbers will produce a much cleaner reverse voltage waveform.

The saturable core model looks like an inductor in parallel with a resistor. This resistor emulates the core loss which helps to dampen the ringing from the output diode. The following figure shows an equivalent circuit.
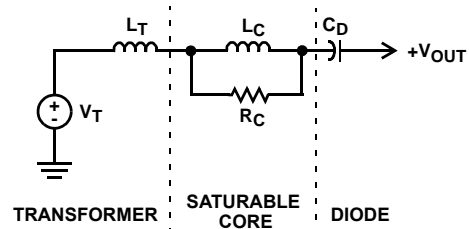

FIGURE 16. SNUBBER EQUIVALENT CIRCUIT

V_T represents the transformer secondary winding. L_T is the secondary side leakage inductance. L_C and R_C represent the saturable core inductance, L_C, and core loss, R_C. C_D is the output diode capacitance during reveres recovery. During reverse recovery the saturable core is coming out of saturation and the inductance is increasing. During that time, V_T will be across the parallel network formed by L_C and R_C. The inductive impedance will be higher than R_C so therefore R_C will dominate and form an L-R-C circuit with L_T and C_T. This is much more effective as a snubber than placing an R-C network across the output diode.

The equivalent core loss resistance is a function of the core geometry, applied waveform, and core material. Core loss resistance is inversely proportional to core loss. Higher core loss results in a lower R_C which also results in more dampening. The following equation shows an approximation to core loss.

$$P_C \propto f \times (V_C)^2 \times \left[\frac{I_m}{N}\right] \times \left[\frac{\mu H_{SAT}}{R_K}\right] \qquad \text{(EQ. 16)}$$

where f is the switching frequency, V_C is the voltage across the core and R_K is a core loss resistance constant based on the material. If there is sufficient blocking capability, then V_C and V_T are approximately equal. Increasing either the switching frequency or the voltage across the core will increase the core loss, but modifying the core geometry will also have an effect. This equation is useful for solving problems with saturable cores that are running too hot. Note that while I_m has no effect on the blocking time, it does affect the core loss.

Choosing the Right Core

Now that the theory has been discussed, choosing the correct saturable core is next. This is only a guide in directing the user in the right direction in selecting saturable cores.

For output designs of 5V or less, start with a single turn W-material core, such as 40705 from Magnetics Inc. For higher output voltages, V_{CORE} will be higher and requires more turns on the saturable core. For example, 48V output designs will need about 4 turns to maintain the same blocking performance. Also, core loss becomes an issue and F material is suggested as a starting point.

The blocking volt-time waveforms applied to the saturable cores are not simple. The voltage across the core is illustrated in Figure 17.
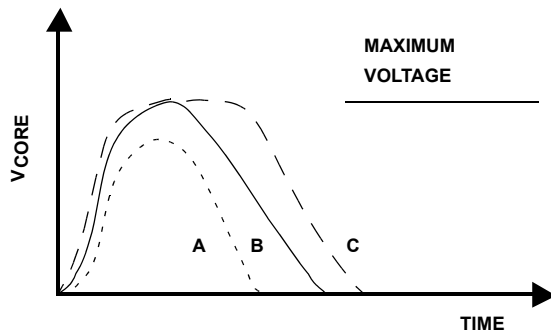

FIGURE 17. VARIOUS CORE BLOCKING TIMES

Figure 17 shows the blocking voltage of three different cores, each with a different blocking time. The shape of the blocking voltage waveform results from resonant ringing. Each of these traces shows different core blocking times.

- **Curve A** shows a core with not enough blocking. The peak voltage does not reach the same voltage as the reverse voltage on the output diode. To fix this problem either increase the core area or the number of turns. The affect on the primary is that the resonant time will be short and it will take a higher load current to ZVS.

- **Curve B** represents a core where the peak voltage is just about equal to the output diode reverse voltage. This is the optimal design. There is just enough blocking for the resonant period and not too much to affect the maximum duty cycle. When the primary D-S voltage on the MOSFET rings to 0 V, it has reached the point at which the blocking time is no longer needed.

- **Curve C** shows too much blocking. This is shown by the *clipped* voltage resulting from not enough transformer secondary voltage. This also drastically affects the maximum duty cycle of the output inductor and increases the core loss. For this situation, reduce the core area or the number of turns.

The "rule of thumb" when choosing a core is to set the blocking so that clipping just starts to occur. If there is insufficient blocking capability it will be more difficult to ZVS.

If there is too much blocking, too much time will be taken to saturate the core, and the effective duty cycle will be lowered. Additionally, there will be excessive core loss in the saturable cores.

Different materials will have different affects on blocking. W and J material from Magnetics Inc. have the exact same blocking characteristics. F, R and Metglas® materials have a higher H_C which requires higher reverse current to reset the core. They require an extra winding which carries current to offset the B-H loop for 5V output designs. See Figure 21. For 48V output designs, these materials do not require an extra winding but will require more turns than W material because the μH_{SAT} product is less.

The amount of damping required is dependent upon the user. A well damped design will require the saturable core to dissipate more energy than an under damped design. W and J material have the same blocking characteristics, but the core loss resistance is higher in J material. It does not dampen as well as the W material. F, R and Metglas® materials usually do not dampen enough unless an extra winding for current is used as in Figure 21, or an extra resistor is used in parallel with the core. The parallel resistor decreases the overall core loss resistance and dissipates the power in another element.

Another effect to consider is the frequency of operation. Core loss is directly proportional to the frequency. The frequency limitation is around 150kHz for the ferrite materials (like W, J and R) and up to 200kHz for Metglas®.

Thermal

One of the big issues with saturable cores is self-heating due to core loss. Depending on the material this could become a major issue.

All magnetic materials have what is known as the Curie temperature. If this temperature point is exceeded, the relative permeability, μ_r, of the material reduces to 1, the same as free space. In actual designs this temperature should never be approached in a core. The Curie temperature varies significantly from one material to the next. For example, Magnetic Inc.'s F material has a Curie temperature of 250°C while W material is only 125°C.

There are varies ways to minimize the self heating of the saturable core. Keeping the blocking time as low as possible or keeping the switching frequency to the minimum. Another is to use materials that have low damping to the diode voltage ringing and use a parallel resistor. Increasing I_m and keeping A_e constant will increase core loss and dampening on the diode. However, the improvement in cooling due to the increase in surface area to volume ratio outweighs the increase in core loss. These methods were discussed earlier. However, if these techniques are not practical and core temperature is still a problem, the following techniques can be applied to the core.

Reducing the heating from the wire can help reduce the overall temperature. Instead of one large wire, use multiple insulated wires in parallel where the radius of the wire is less than the skin depth at the operating frequency. Avoid bunching up the wire so that heating due to the wires do not generate a local hotspot. Having a short lead distance between the core winding and a large copper area on the PWB will help conduct the heat out of the core.

Placing the saturable core in high airflow also helps. However, careful core temperature measurements must be made to detect "dead spots" in the airflow. That part of the core can have high temperatures because of minimal airflow.

It is also possible to heatsink a saturable core. The following figure shows such a design.
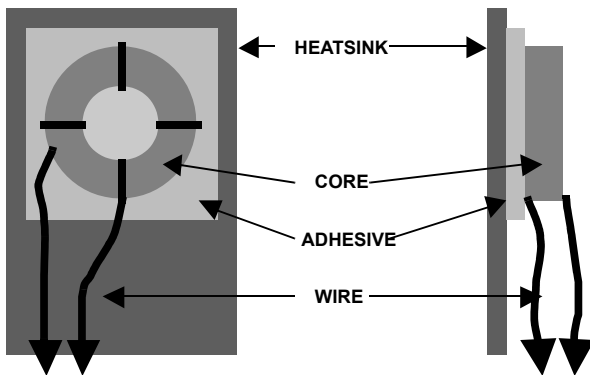
FIGURE 18. SATURABLE CORE HEATSINK

Figure 18 shows a saturable core with 4 turns mounted on a metal plate acting as a heatsink. Between the core and heatsink is a thermally conductive adhesive or epoxy to make better thermal contact between the core, windings and metal plate. This method has been shown to be very effective in cooling saturable cores.

Some core materials can be allowed to run hot because of their high curie temperature. However, if the temperature exceeds 130°C, it may be necessary to redesign the assembly for a higher rated insulation class per the relevant safety agencies.

Conclusion

This design guide shows several techniques to improve the ZVS range of the ZVS full-bridge converter. Some like the transformer are easy to implement while the saturable cores offers other significant advantages. Also what is provided is some practical design considerations and guidelines with these techniques.

References

[1] Lloyd H Dixon Jr., "Eddy Current Losses in Transformer Windings and Circuit Wiring", SEM600 Unitrode Seminar

[2] Magnetics Inc. Ferrite Cores catalog, 1999

Appendix

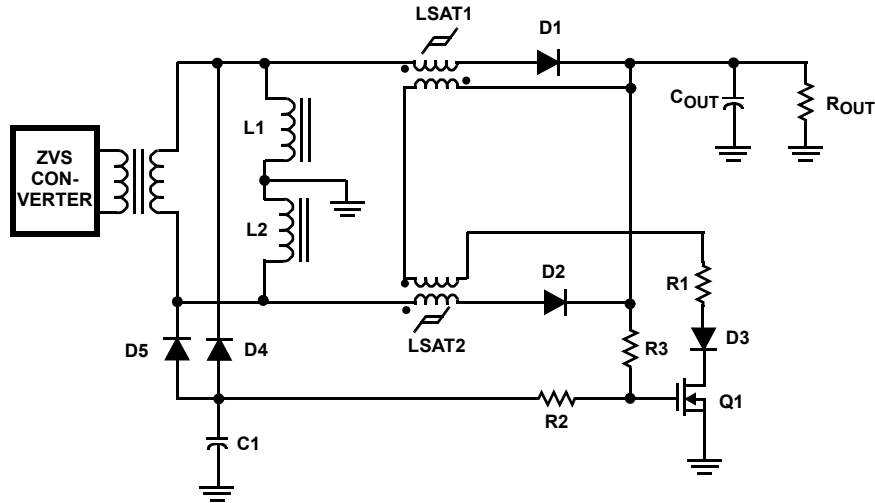The following section shows some useful circuit configurations involving saturable cores.

FIGURE 19. CONSTANT BLOCKING TIME CIRCUIT

Constant Blocking Time

The problem with wide range input converters is that the blocking time increases as the input voltage decreases. This is solved with the following circuit. This circuit behaves similar to magnetic amplifiers, but instead of regulating the output voltage, the blocking time will be held nearly constant as the secondary transformer voltage decreases. The circuit functions by using D5, D4 and C1 as a peak detect circuit. R2 and R3 form a voltage divider between the output voltage and voltage at C1. As the transformer secondary voltage decreases, the gate-source voltage increases and Q1 draws more current. As more current is drawn, the saturable cores will block less. R1 is a current limit resistor and D3 limits current flow to one direction. (Note: This configuration will work with a center-tapped output.)

Be careful of reverse voltage stress on the output diodes. When the saturable cores are disabled, there is no damping and reverse voltage ringing on the output diodes may be significant.

Magnetic Amplifier Post Regulator

Below is a magnetic amplifier circuit that can be used with the ZVS full-bridge topology. Not only does this facilitate post regulation on an output winding, but helps to ZVS the converter at the same time. For this application, the best saturable core material to use is either Permalloy 80 (Magnetics Inc.) or Metglas® 2714A alloy or equivalent. In order to control the output voltage with this material, blocking must occur over a wider range resulting in higher volt-times and increased core loss.
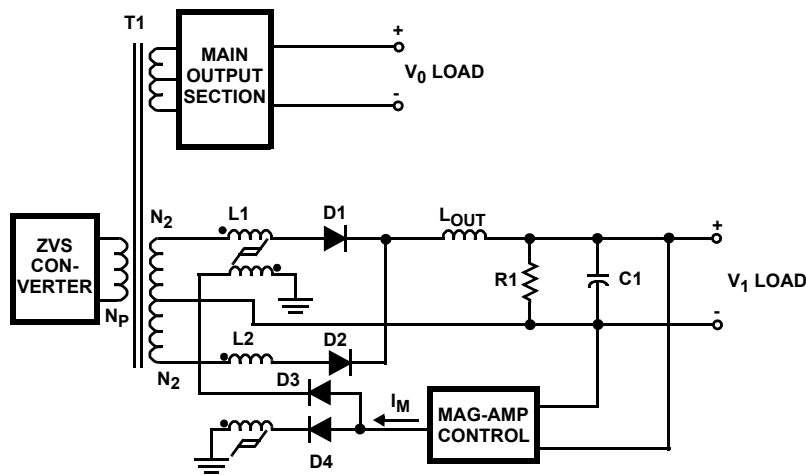

FIGURE 20. MAG-AMP CIRCUIT

B-H Loop Modifier

It was mentioned earlier that some magnetic materials which have high H_C, such as Metglas®, do not work properly as saturable cores for ZVS converters. The problem with these materials is that there is not enough reset current to reset the core. To fix this problem, a small amount of I_M is added to the core thus shifting the B-H loop.
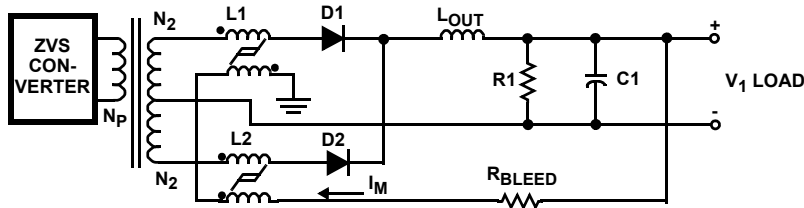
FIGURE 21. B-H LOOP MODIFIER CIRCUIT

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