STMicroelectronics
L6717A AM3 Solution for Desktop Power

AMD CPU Advanced & Green Power Management

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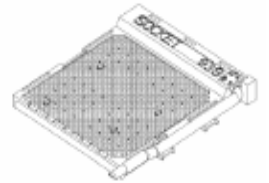
Agenda

- STMicroelectronics vs. AMD Alignment
- ST L6717 Power Solution
  - Pin Assignment & Reference Schematic
  - IC Operation & Configuration
  - LTB Snapshot
  - I2C Interface for Power Management
- Demo Board Overview
- Controller Details: LTB Technology ®
- XLS Design Tools & SVI-I2C Interface SW

ST Alignment with AMD Platforms

AMD Smarter Choice

	Revision E	Revision F/ G	GH[1]	H / >H
Socket	 Socket 939	 Socket M2	 Socket M2 and M3	 Socket M3
TDP	DC = 110W / 80A FX = 104W / 80A SC = 89W / 60A	FX = 125W / 95A DC = 104W / 80A SC = 72W / 60A	QC = 140W / 110A QC = 125W / 95A DC = 89W / 80A SC = 45W / 45A	QC = 140W / 110A QC = 125W / 95A DC = 89W / 80A SC = 45W / 45A
PVI / SVI	5bit PVI 1Rail	6bit PVI 1Rail	SVI 2Rails	
	L6713A, L6714 – 3 / 4 Phase Controllers - PVI			
	L6717, L6740L (*1st Hybrid Regulator*) – (4+1) Phase Controller			

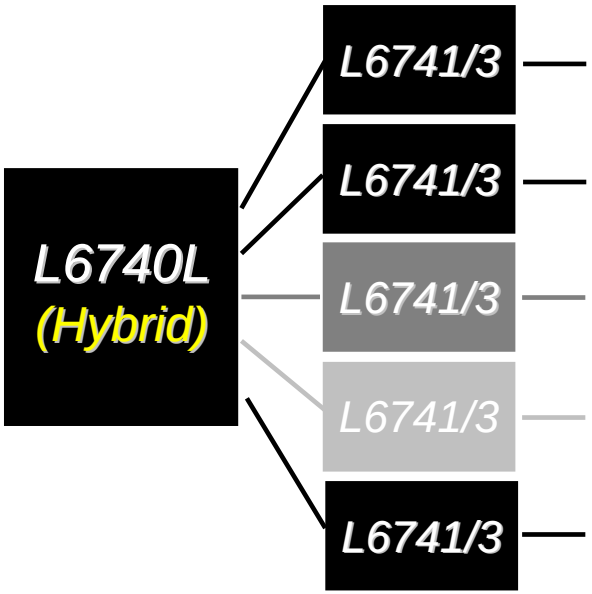
ST DT/Server AM2r2/Fr2 Solutions

ST L6713A, L6714

PVI Architecture

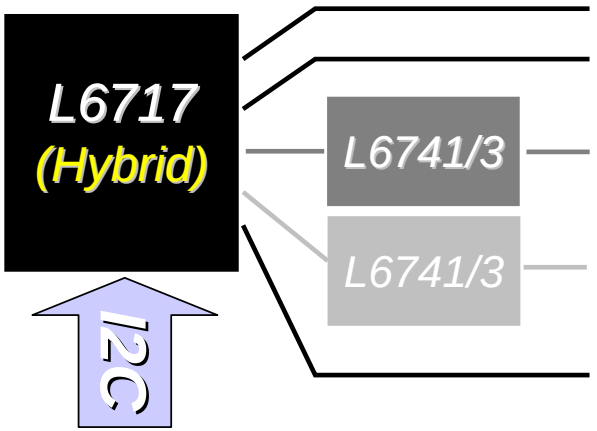
- 2 to 3/4 Phase Controller
- Embedded Drivers Arch.
- LTB Technology®
- OVP, OCP, FB_DISC
- 10x10 HTQFP64

ST L6740L



- **Hybrid Controller**
- 2 to 4Ph CORE + 1Ph NB
- PVI / SVI Compatibility
- PSI_L Management
- LTB Technology®
- OVP, OCP, FB_DISC
- 7x7 HTQFP48

ST L6717



Hybrid Controller + I2CPM

- 2 - 4Ph CORE (2Emb + 2PWM)
- 1Ph NB (Emb)
- PVI / SVI Compatibility
- *I2C Power Manager*
- LTB Technology®
- 7x7 VFQFPN48

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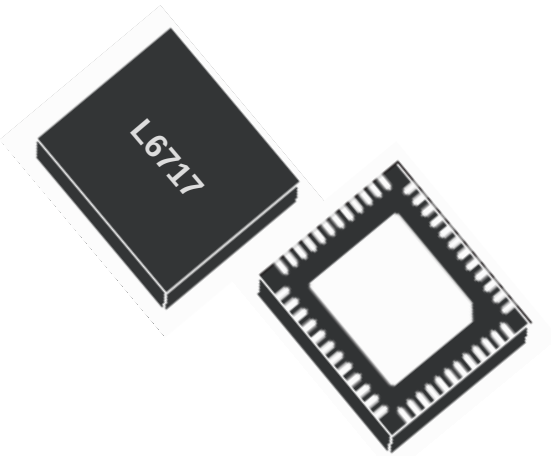
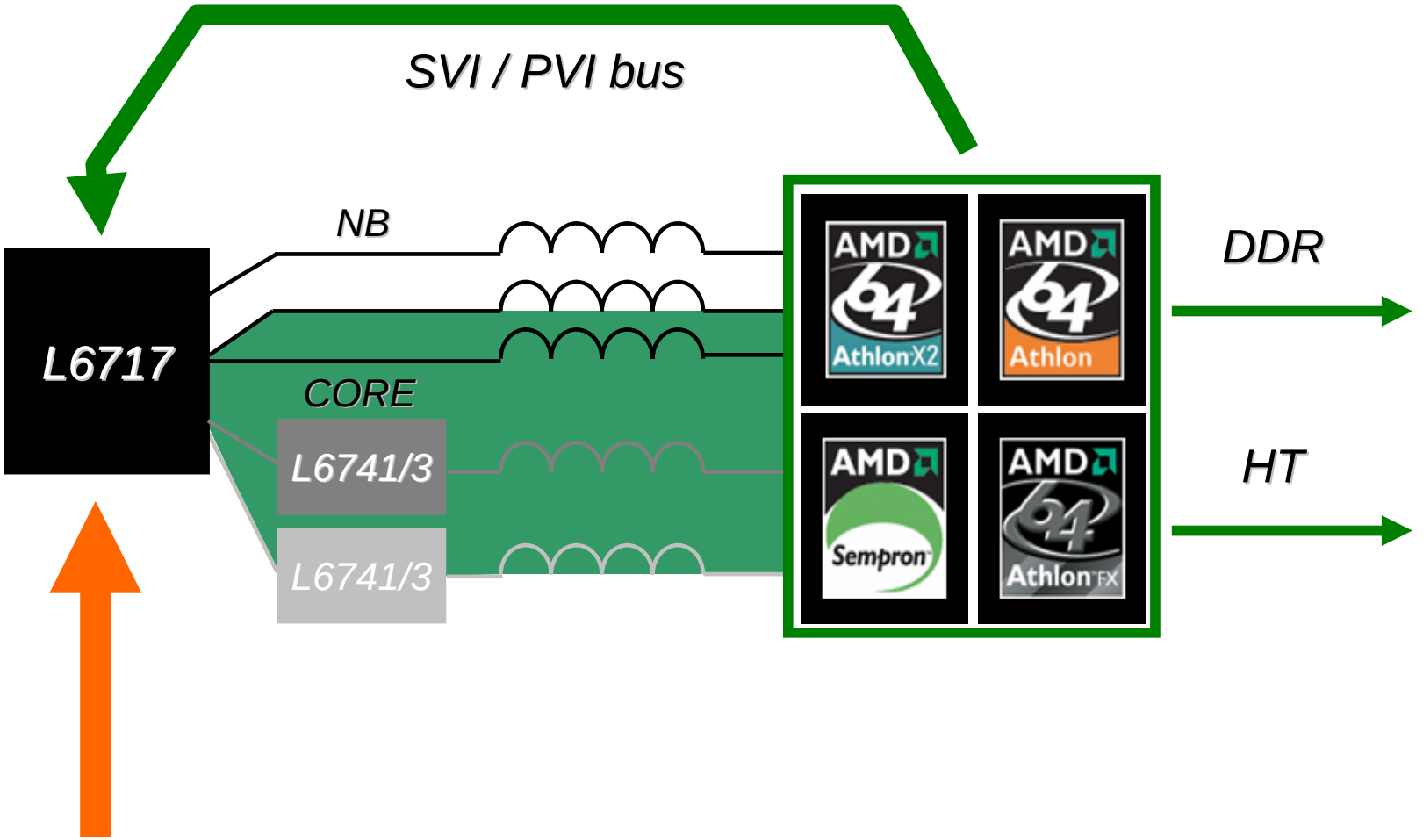
L6717 – Hybrid Controller with Power Manager I2C

- **HIGH CURRENT EMBEDDED DRIVERS (2+1) + 2 ADDITIONAL PWMs**
- ***Power Manager I2C Bus***
  - OVP SETUP
  - FSW MARGINING
  - POWER MANAGEMENT SETUP
  - LL ADJUSTEMENT
  - OVERSPEEDING
- **AUTOMATIC PVI/SVI CPU DETECTION**
- **EFFICIENCY OPTIMIZATION**
  - DYNAMIC PHASE MANAGEMENT (DPM)
- **LTB Technology®**
- DUAL DIFFERENTIAL REMOTE SENSE
- DIFFERENTIAL CURRENT SENSE for both CORE & NB
- CORE DUAL OCP THRESHOLD: PER-PHASE AND TOTAL CURRENT
- **PRE-BIAS STATUP MANAGEMENT**
- FEEDBACK DISCONNECTION PROTECTION
- VFQFPN48 (7x7mm) PACKAGE



L6717 – Application Block Diagram



Secondary I2C bus for ST Power Manager;
Allows Real-Time Over-speed, Fsw Modification, Phase Shedding…

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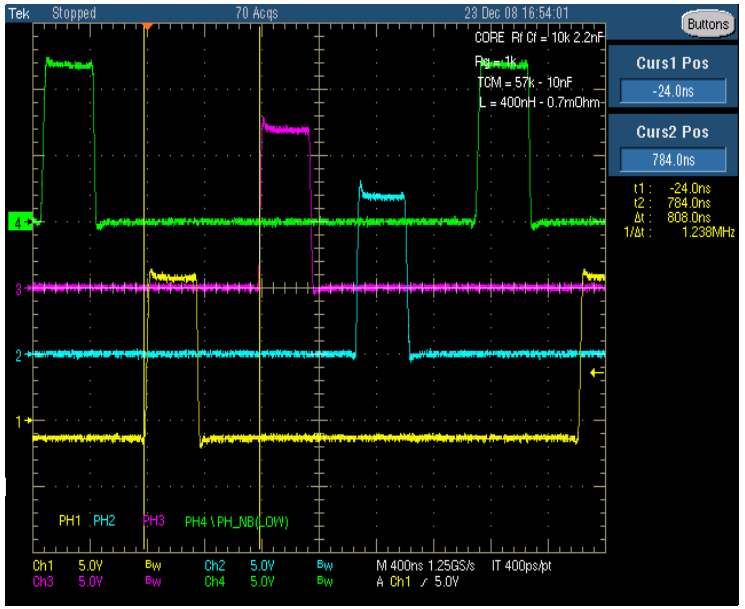
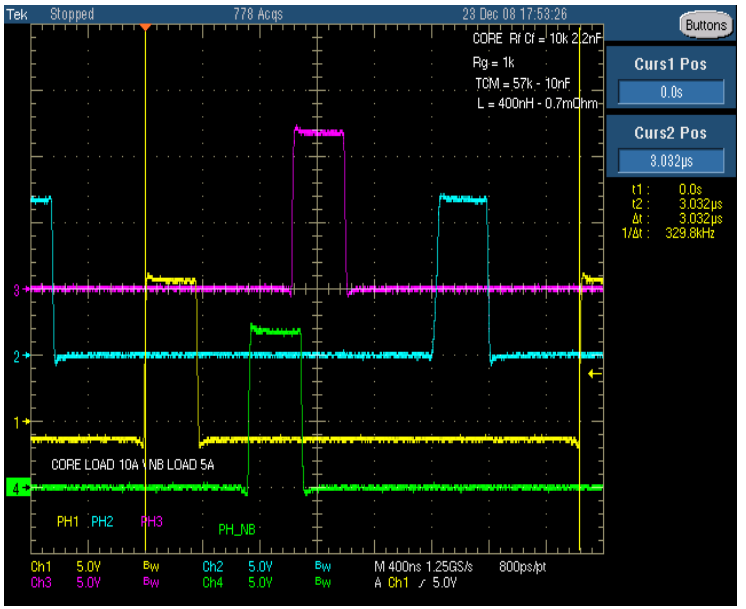
PHASE NUMBER Selection & Interleaving (1)

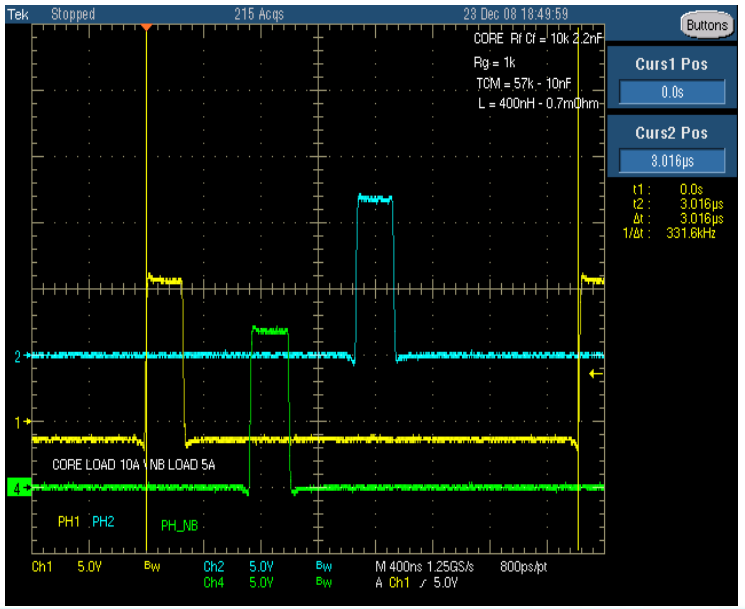
4 PHASE



3 PHASE



2 PHASE



3 Phase Operation

PWM4 = SGND

CS4+ connected to $V_{COR}E$

CS4- → V_{CORE} by same R_G of other channels

2 Phase Operation (see next slide)

PWM3 & PWM4 = SGND

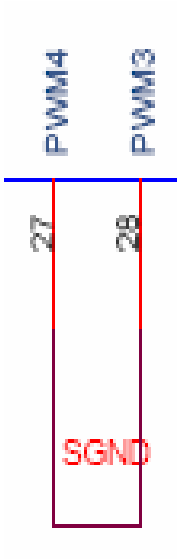
CS3+ & CS4+ connected to V_{CORE}

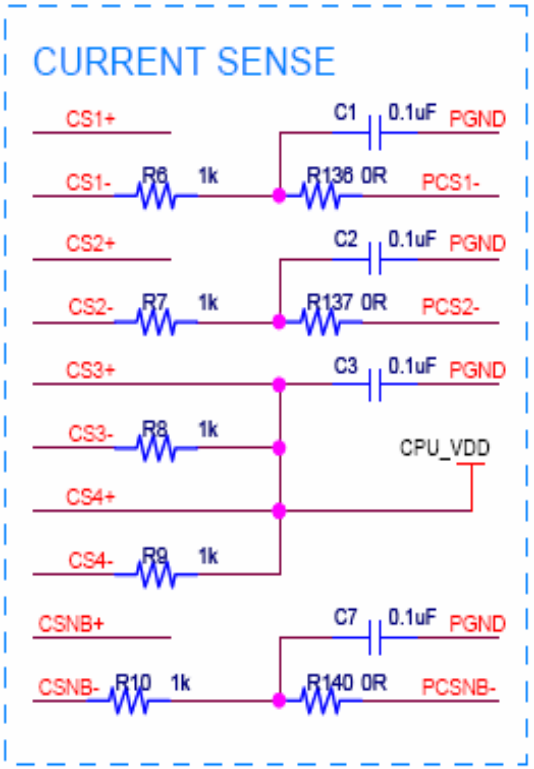
CS3- & CS4- → V_{CORE} by same R_G of other channels

PHASE NUMBER Selection & Interleaving (2)

2 PHASE Operation Case

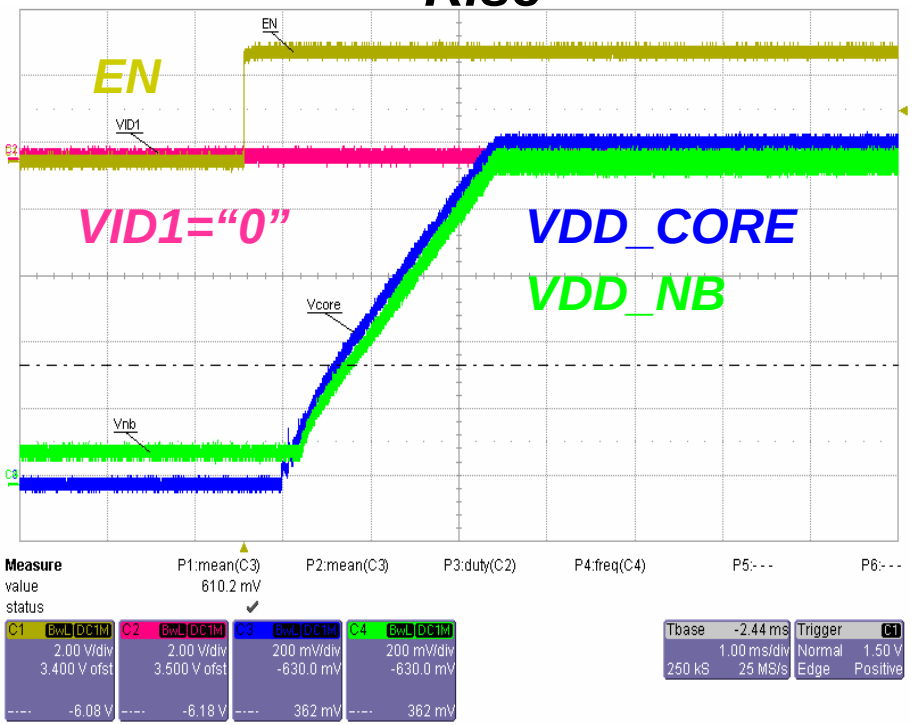
The information on the number of active phases is latched @ EN rise.





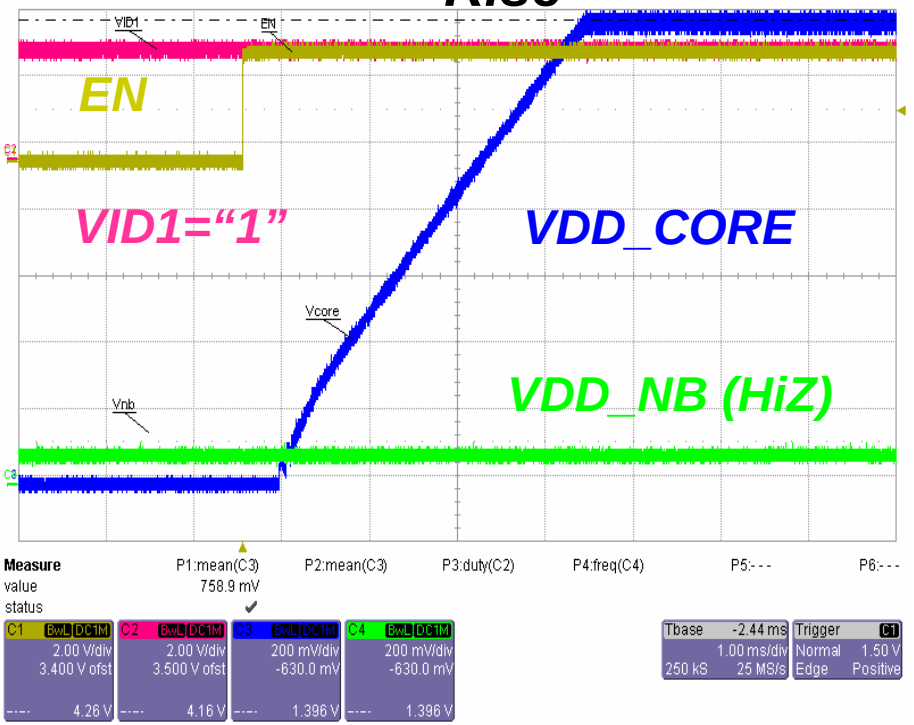
SVI/PVI Mode Detection

SVI Mode → VID1="0" @ EN Rise



VID[2:3]=[xy] are decoded
to define the bootstrap voltage

PVI Mode → VID1="1" @ EN Rise

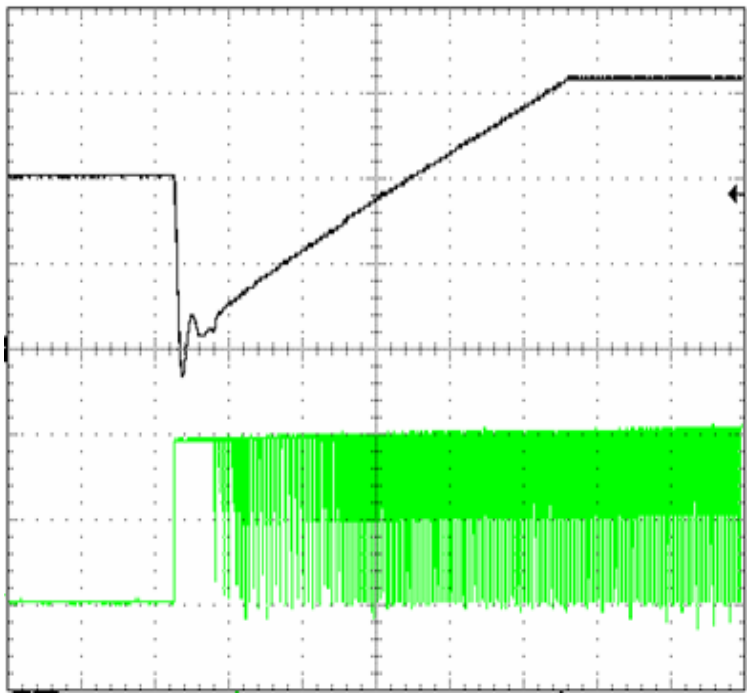


VID[5:0]=[xxxx1x] are decoded
to define the bootstrap voltage

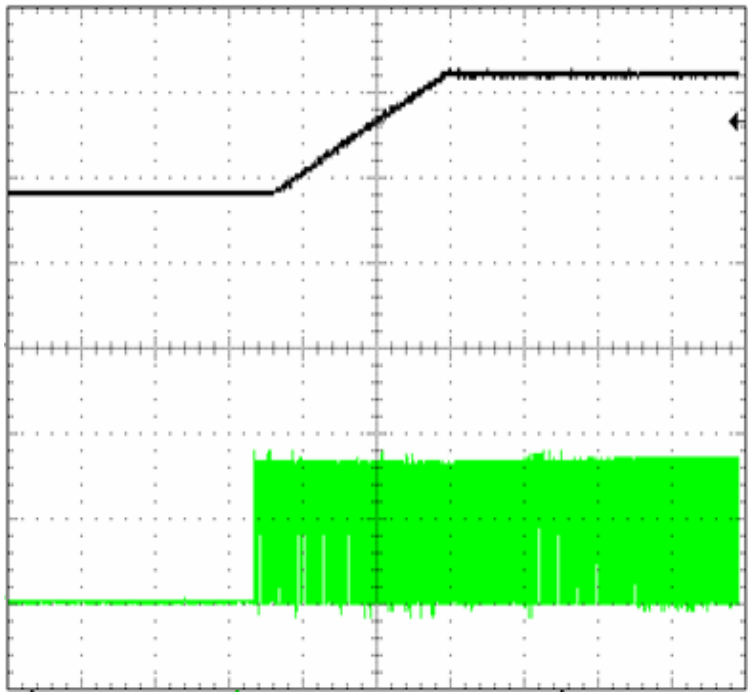
LS-Less Start-Up

- Allows managing pre-biased output start-up
  - Low-Side MOSFETs are kept OFF until reference = V_{OUT} (depends on ext driver compatibility, need to manage HiZ)
  - No Output Voltage undershoot observable (negative spike)!!

NO-LS-Less Startup



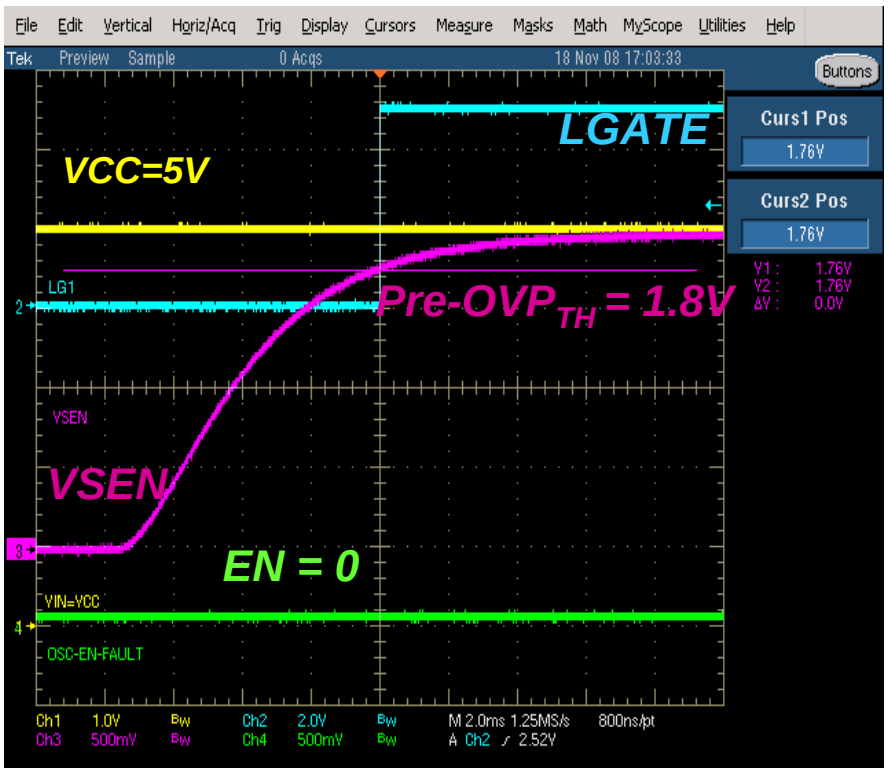
LS-Less Startup



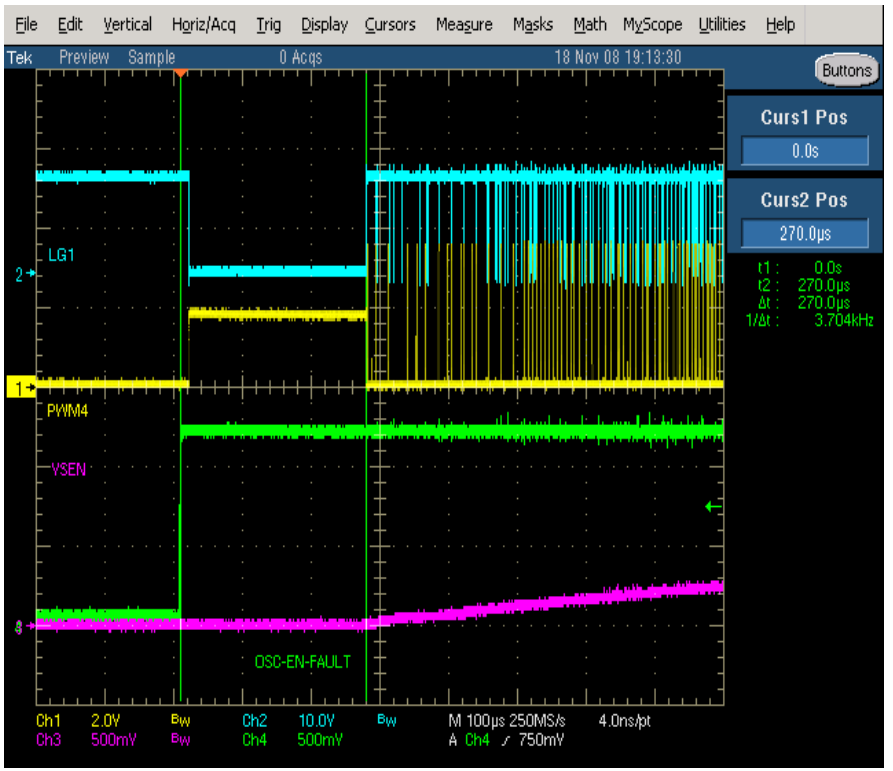
Pre OVP Protection

Pre-OVP Protection allow to protect the Load against OVP event also when L6717 is disabled.

- VCC and VCCDRV need to be connected to 5V_SBY
- VSEN is monitored for both CORE & NB section when EN="0"
- If VSEN/VSEN_NB rises over 1.8V threshold, corresponding LS Gate will be turned on
- EN rising edge will reset Pre-OVP and L6717 performs the SS
- If OVP condition still present after Pre-OVP and EN rising → OVP protection will trigger



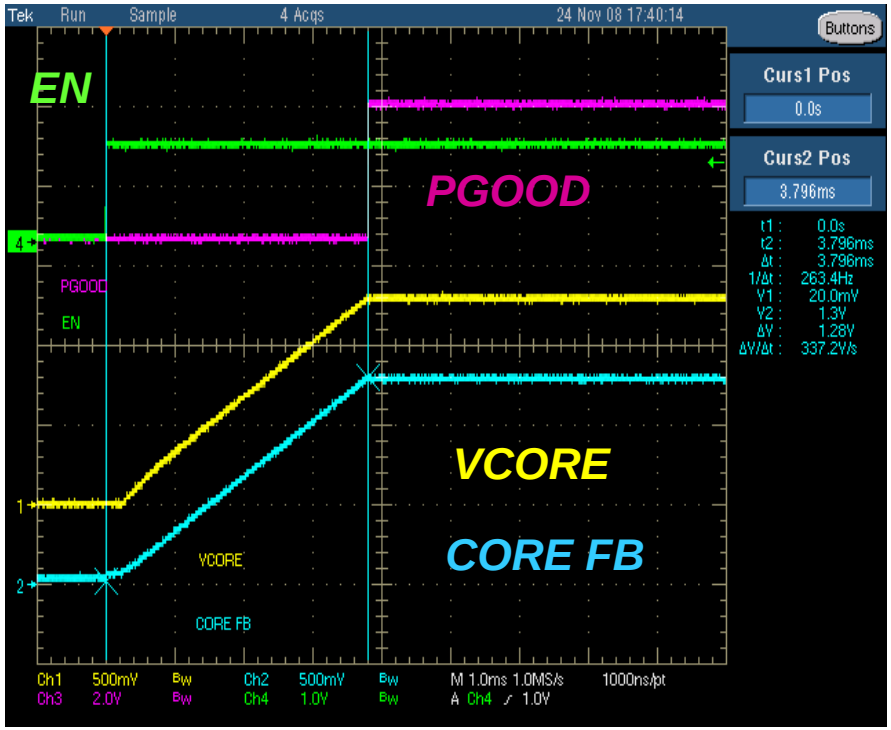
EN = "0" → PreOVP



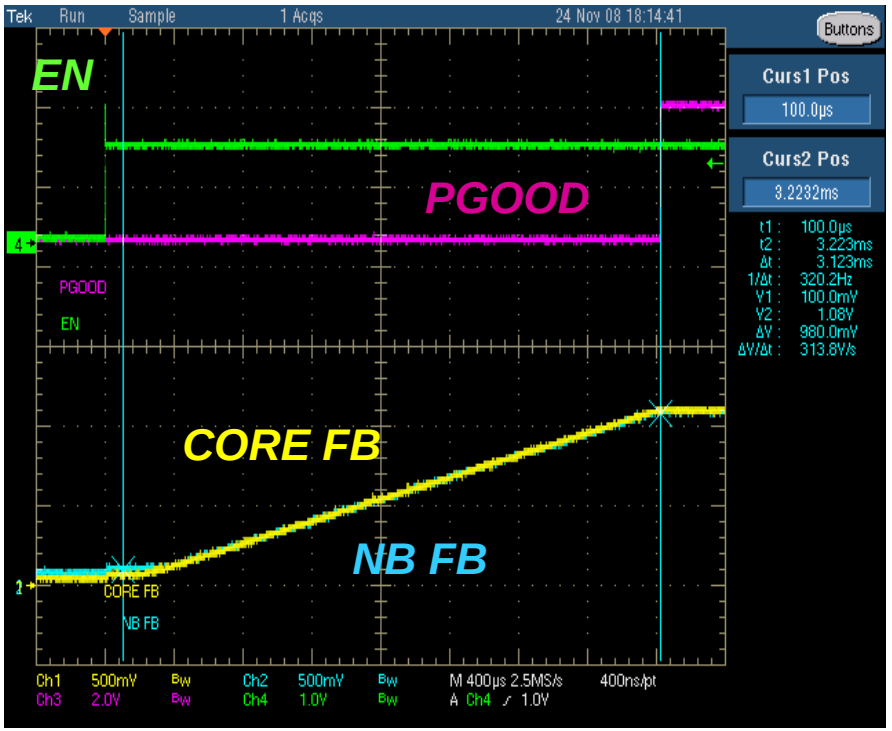
EN = "0"→"1"

PVI/SVI Soft Start & PGOOD

PVI Mode



SVI Mode



PVI Mode

- NB is kept in HiZ State;
- CORE rise its reference to the final voltage according with decoded VID;
- PGOOD is “CORE PGOOD”

SVI Mode

- Both CORE and NB perform simultaneous SS;
- CORE & NB boot to Pre-POWEROK Metal VID
- PGOOD is logic AND of “CORE & NB PGOODs”

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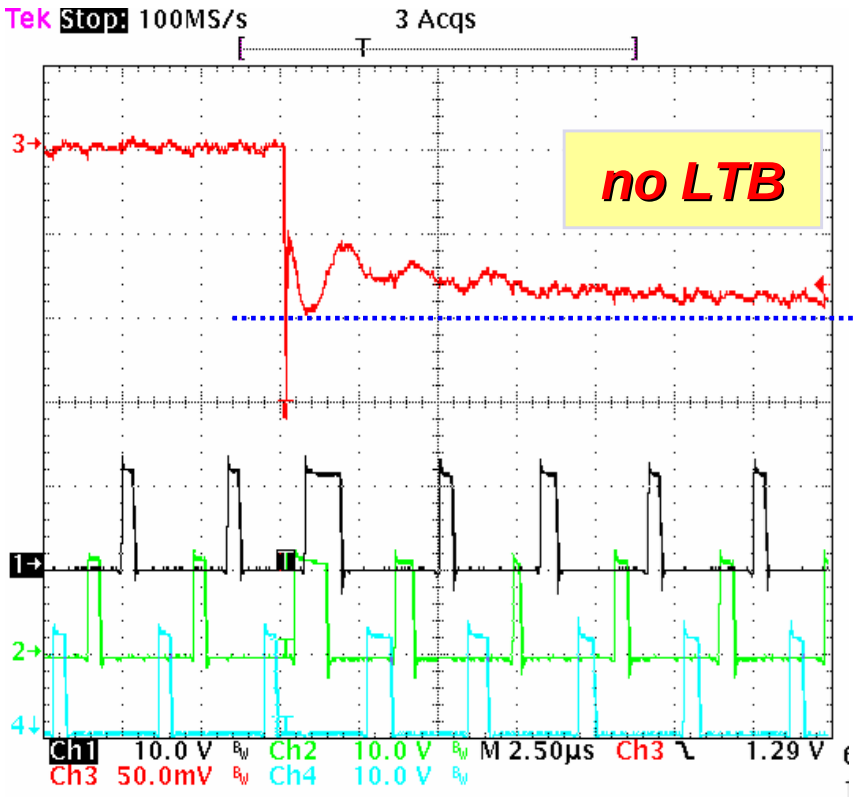
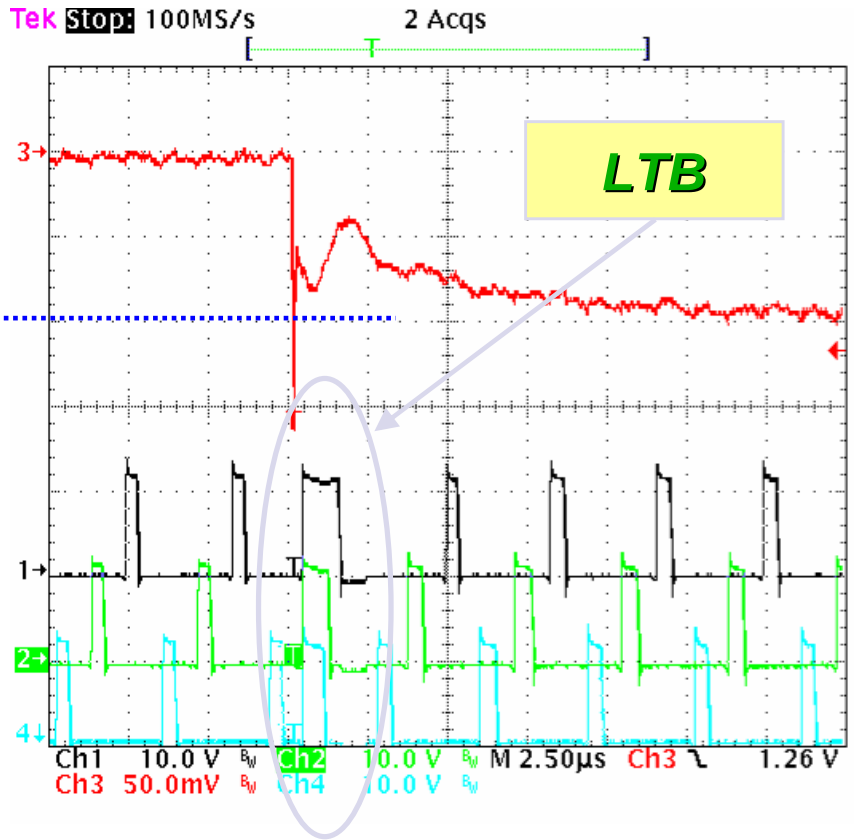
Technical Snapshot: LTB Technology®

- ***LTB Technology®*** **further enhances the performances of Dual-Edge Asynchronous Systems**
- ***LTB Technology®*** **cancels the interleaved phase-shift, turning-on simultaneously all phases. Asynchronous mode only when necessary, preserving noise immunity**
- ***LTB Technology®*** **implements a parallel, independent loop that reacts to Load-Transients bypassing E/A latencies. The LTB Comparator sets the correct amount of transferred energy**
- **With *LTB Technology®* each Phase is boosted with the correct amount of energy to recover from phase-to-phase asymmetries keeping the phase currents balanced.**

Fastest response through direct detection of high load transients,
for cost effective application design

Technical Snapshot: LTB Technology®





The device turns on simultaneously all the phases as soon as a load transient is detected (trough the dedicated LTB pin)

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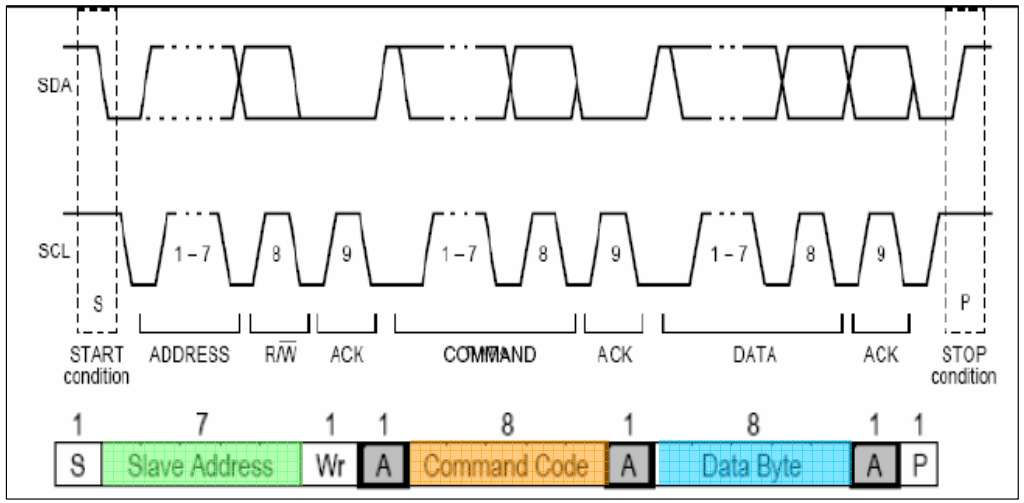
- I2C Interface for Power Management
  - I2C Protocol Overview
  - I2C Command Description
  - OS Setting
  - OVP Setting
  - FSW Adjust
  - Droop Adjust
  - DPM (Dynamic Phase Management)
- I2C Bus Special Features
  - I2C_ ADDRESS Change (SVI Mode Only)
  - I2C_DISABLE → Analog OVP & OS (SVI Mode Only)

I2C Bus: Protocol Overview

- I2C Interface is **Active** by default in both **SVI** and **PVI** Mode.
- **I2C Bus** & **SVI Bus** are two Parallel and Independent Interfaces.
- I2C Commands may be issued by I2C Master once **PGOOD** is High.



ADDRESS PHASE	
1:6	Always 110011b.
7	Slave Address. According to ADDR connection, the device will act if addressed by '0' or '1'.
8	WRITE bit.
COMMAND PHASE	
1:3	Not Applicable, ignored.
4:6	Command Code
7, 8	Not Applicable, ignored.

	Command Code [4:6]	Data Stream [1:8]
OFFSET CORE and/or NB	1CN	[1:2] xx [3] SIGN [4:8] OVRSPD
OVP SETTING	000	[1:4] xxxx [5:6] OV_NB [7:8] OV_CORE
FSW ADJUST	001	[1:5] xxxxx [6:8] FSW
DROOP ADJUST	010	[1:4] xxxx [5:6] k_{DRP} [7:8] k_{DRPNB}
POWER MANAGEMENT	011	[1:3] xxx [4:5] DPMTH [6] PSI_A [7] PSI_EN [8] DPM_ON

I2C Bus: Command Description

Command	Description
OVRSPD ***1 sign +5 data bit***	***OFFSET for Over-Speeding*** Sets offset above regulation reference up to 2.8V, 1bit sign+5bit data Applies to CORE and NB Section (NB only positive and clamped at +600mV)
OVP_SET ***2 +2 data bit***	***OVP Setup*** Sets OV threshold above the regulation reference of +250mV (default) with 4x 200mV steps. Section bit defines which section (CORE, NB) the data applies to.
FSW_ADJ ***+3 data bit***	***Fsw Adjustment*** Modifies the Fsw set by OSC pin by +20%, +10%, 0% (default), -10%, -20%.
DRP_ADJ ***2+2 data bit***	***Droop Adjustment*** Modifies the k_{DRP} and k_{DRPNB} to modify the LL without changing external components. Applies to CORE and NB Section.
PWRMNG ***2 + 1 data bit*** ***+ 1 +1 en bit***	***DPMTH → DPM Thresholds*** Allow to define different threshold for DPM transitions.. ***PSI_A → PSI Action*** Defines the action to take when PSI_L is asserted. #=1 (default) or #=2. ***PSI_EN → PSI ENable*** Enables (default) or Disables PSI_L (When 0, ignores PSI_L flag from CPU) ***DPM_EN → Dynamic Phase Management Enable*** Enables or Disables (default) DPM mode. (PSI_L flag overrides DPM when asserted.)

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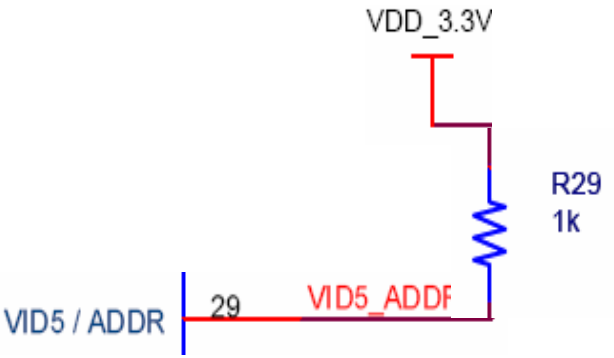
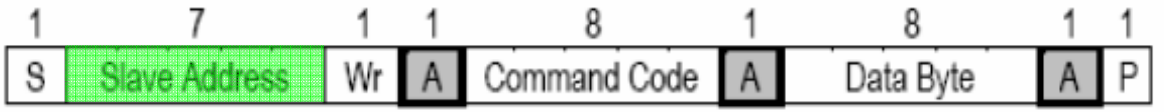
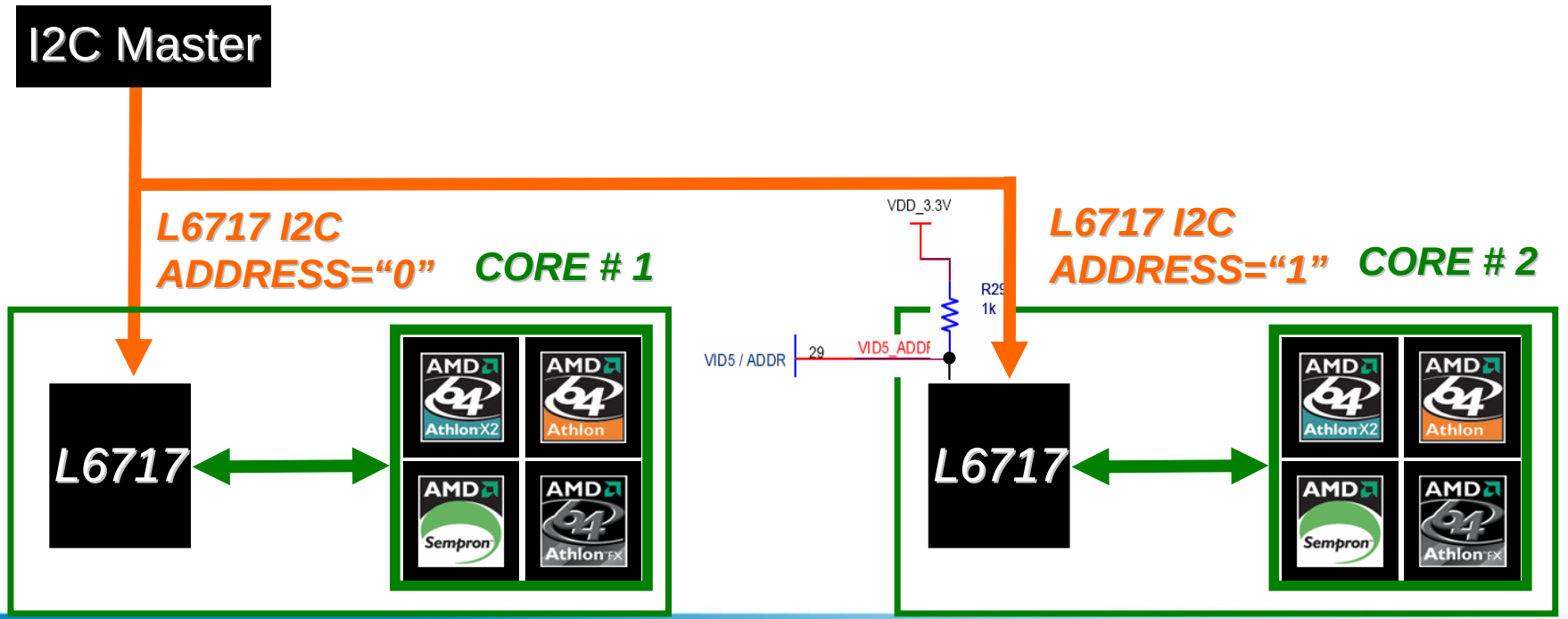
- I2C Bus Special Features
  - I2C_ ADDRESS Change (SVI Mode Only)
  - I2C_DISABLE → Analog OVP & OS (SVI Mode Only)

I2C Bus Special Features: I2C_ADDRESS *(SVI Only)*

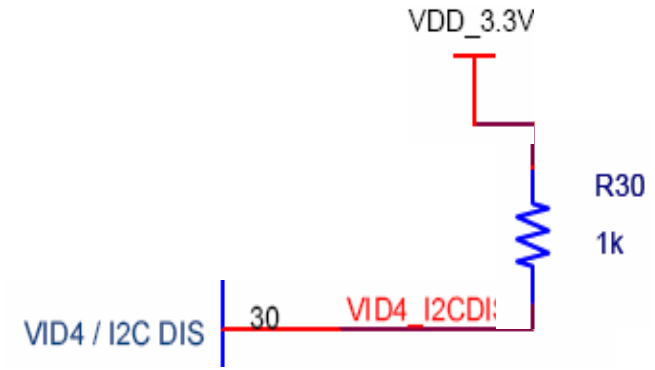


bits	Description
ADDRESS PHASE	
1:6	Always 110011b.
7	Slave Address. According to ADDR connection, the device will act if addressed by '0' or '1'.
8	WRITE bit.

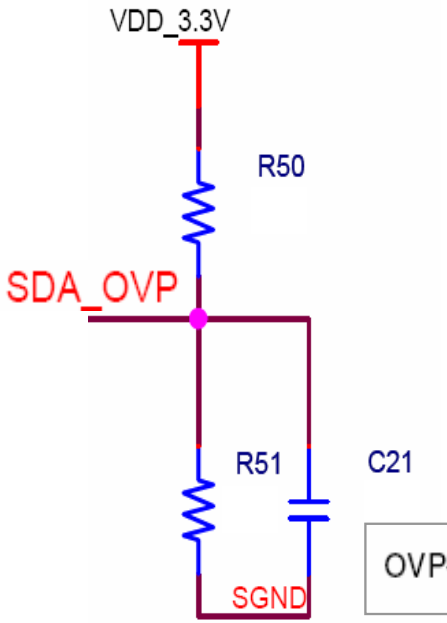




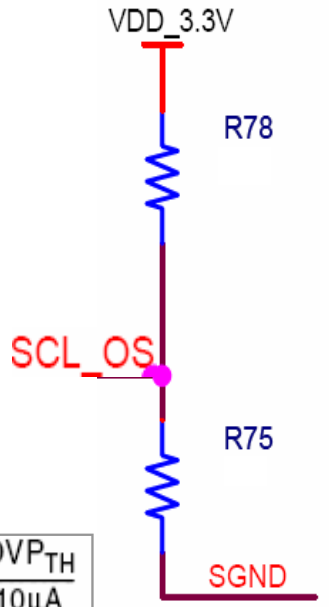
I2C Bus Special Features: I2C_DISABLE *(SVI Only)*



- **I2C_DISABLE**
  - **ANALOG CORE & NB OVP by SDA pin**
  - **ANALOG CORE Bidirectional OS by SCL pin**



$$OVP_{TH} = R_{OVP} \cdot 10\mu A \Rightarrow R_{OVP} = \frac{OVP_{TH}}{10\mu A}$$



$$V_{CORE} = VID - R_{FB} \cdot (k_{DRP} \cdot I_{DROOP} - I_{OS})$$

$$R_{OS} = \frac{1.240V}{V_{OS}} \cdot R_{FB} \text{ (positive offset)}$$

$$R_{OS} = \frac{VCC - 2.0V}{V_{OS}} \cdot R_{FB} \text{ (negative offset)}$$

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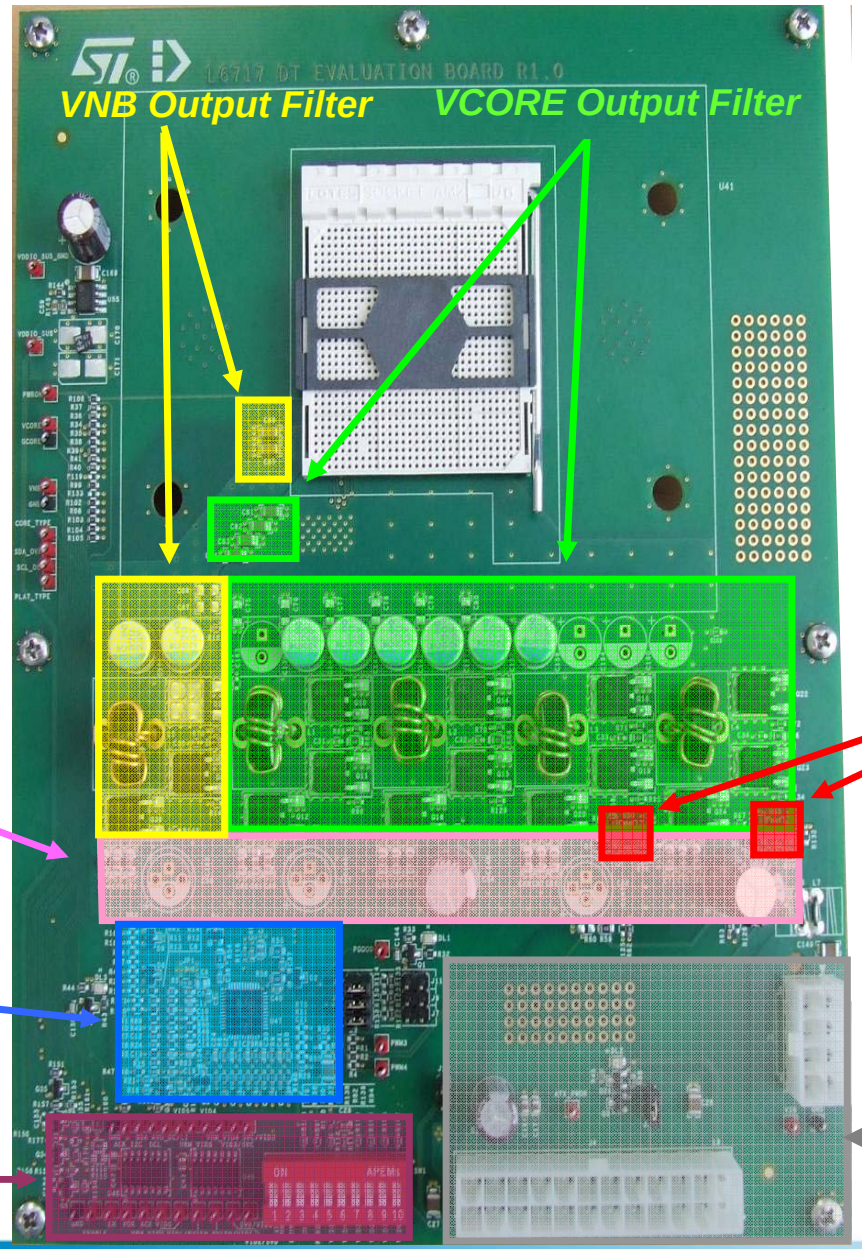
Demo-board Overview: All Board



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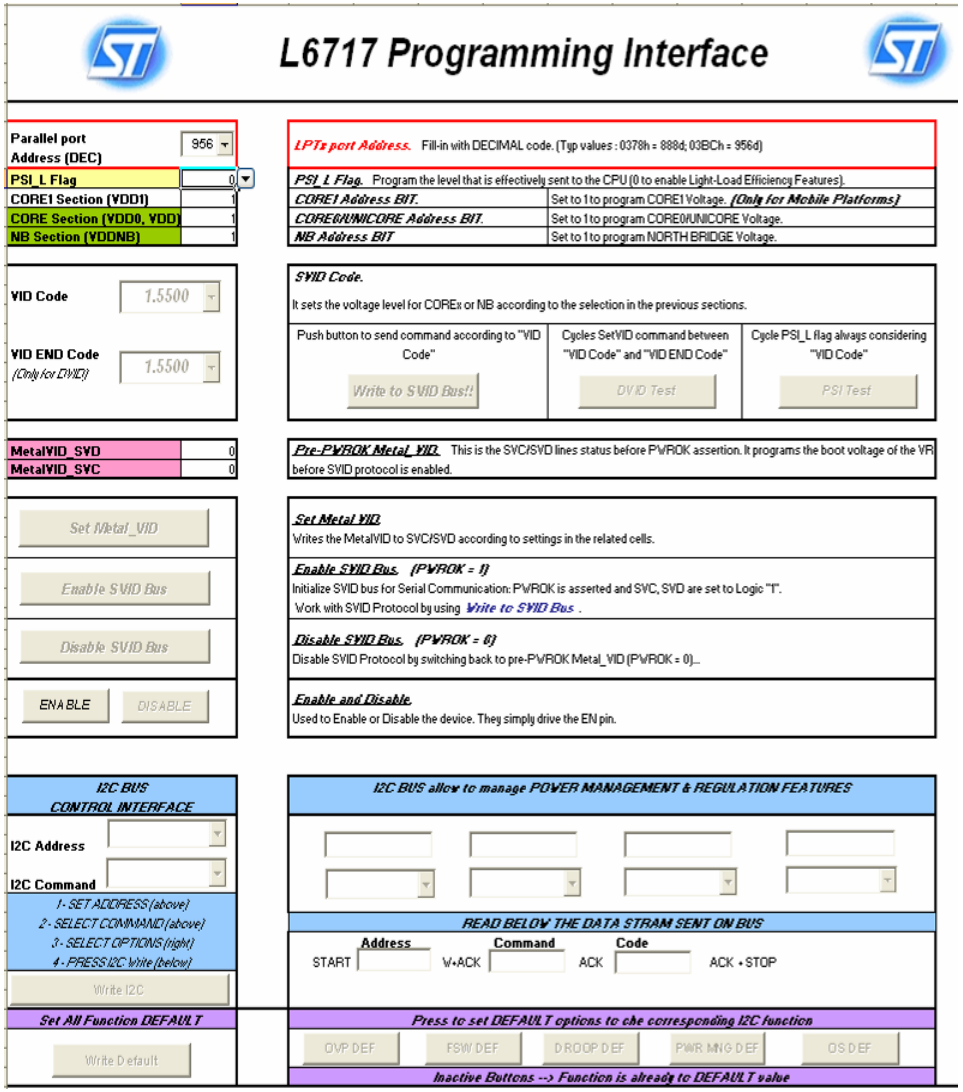


L6717 Programming Interface

Parallel port Address (DEC)	956
PSI_L Flag	0
CORE1 Section (VDD1)	1
CORE Section (VDD0, VDD)	1
NB Section (VDDNB)	1

LPTx port Address. Fill-in with DECIMAL code. (Typ values : 0378h = 888d; 03BCh = 956d)

PSI_L Flag. Program the level that is effectively sent to the CPU (0 to enable Light-Load Efficiency Features).

CORE1 Address BIT.	Set to 1 to program CORE1 Voltage. *(Only for Mobile Platforms)*
CORE0/UNICORE Address BIT.	Set to 1 to program CORE0/UNICORE Voltage.
NB Address BIT	Set to 1 to program NORTH BRIDGE Voltage.

VID Code: 1.5500

VID END Code (Only for DVID): 1.5500

SVID Code.

It sets the voltage level for COREx or NB according to the selection in the previous sections.

Push button to send command according to "VID Code"	Cycles SetVID command between "VID Code" and "VID END Code"	Cycle PSI_L flag always considering "VID Code"
Write to SVID Bus!!	DVID Test	PSI Test

MetalVID_SVD	0
MetalVID_SVC	0

Pre-PWROK Metal_VID. This is the SVC/SVD lines status before PWROK assertion. It programs the boot voltage of the VR before SVID protocol is enabled.

Set Metal_VID

Set Metal VID.
Writes the MetalVID to SVC/SVD according to settings in the related cells.

Enable SVID Bus

Enable SVID Bus. (PWROK = 1)
Initialize SVID bus for Serial Communication: PWROK is asserted and SVC, SVD are set to Logic "1".
Work with SVID Protocol by using *Write to SVID Bus*.

Disable SVID Bus

Disable SVID Bus. (PWROK = 0)
Disable SVID Protocol by switching back to pre-PWROK Metal_VID (PWROK = 0)..

ENABLE DISABLE

Enable and Disable.
Used to Enable or Disable the device. They simply drive the EN pin.

I2C BUS CONTROL INTERFACE

I2C Address

I2C Command

1- SET ADDRESS (above)
2- SELECT COMMAND (above)
3- SELECT OPTIONS (right)
4- PRESS I2C Write (below)

Write I2C

I2C BUS allow to manage POWER MANAGEMENT & REGULATION FEATURES

READ BELOW THE DATA STRAM SENT ON BUS

START | Address | W+ACK | Command | ACK | Code | ACK + STOP

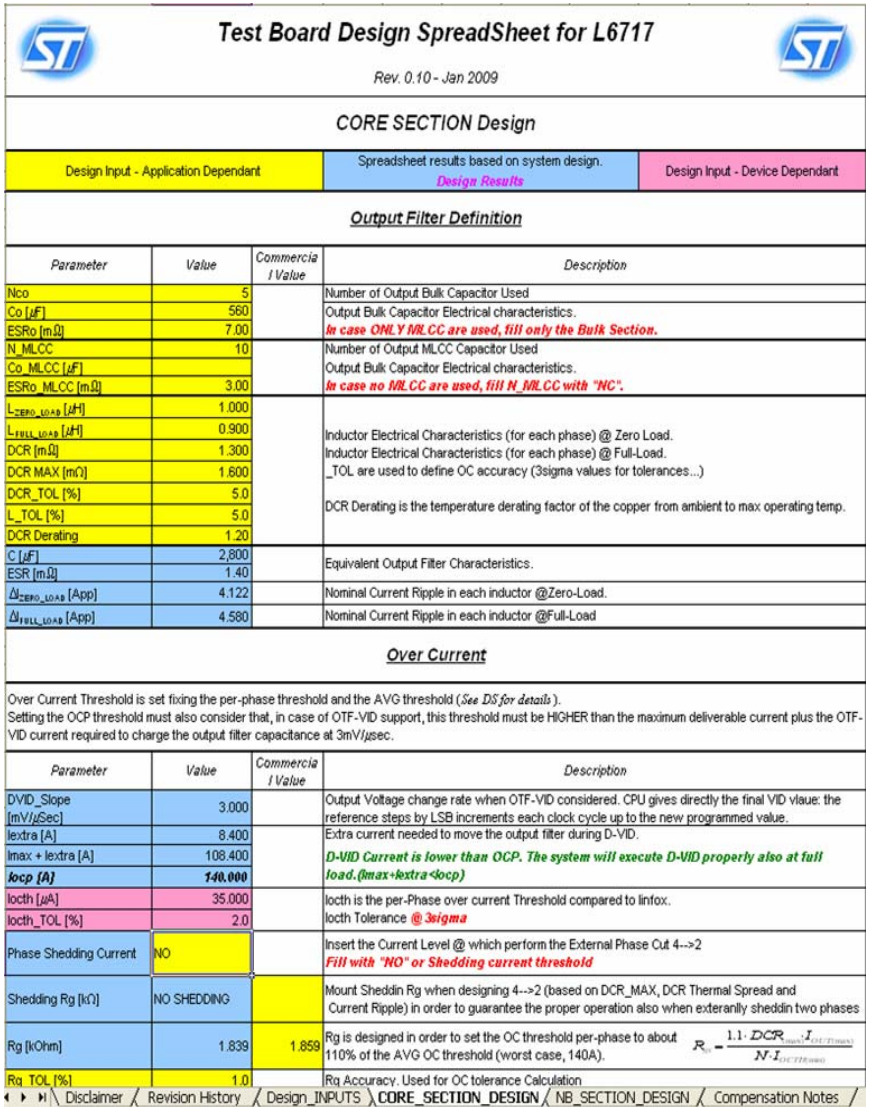
Set All Function DEFAULT

Write Default

Press to set DEFAULT options to the corresponding I2C function

OVP DEF | FSW DEF | DROOP DEF | PWR MNG DEF | OS DEF

Inactive Buttons --> Function is already to DEFAULT value



Test Board Design SpreadSheet for L6717

Rev. 0.10 - Jan 2009

CORE SECTION Design

Design Input - Application Dependant | Spreadsheet results based on system design. *Design Results* | Design Input - Device Dependant

Output Filter Definition

Parameter	Value	Commercial Value	Description
Nco	5		Number of Output Bulk Capacitor Used
Co [µF]	560		Output Bulk Capacitor Electrical characteristics.
ESRo [mΩ]	7.00		*In case ONLY MLCC are used, fill only the Bulk Section.*
N_MLCC	10		Number of Output MLCC Capacitor Used
Co_MLCC [µF]			Output Bulk Capacitor Electrical characteristics.
ESRo_MLCC [mΩ]	3.00		*In case no MLCC are used, fill N_MLCC with "NC".*
L_{ZERO_LOAD} [µH]	1.000		
L_{FULL_LOAD} [µH]	0.900		Inductor Electrical Characteristics (for each phase) @ Zero Load.
DCR [mΩ]	1.300		Inductor Electrical Characteristics (for each phase) @ Full-Load.
DCR MAX [mΩ]	1.600		_TOL are used to define OC accuracy (3sigma values for tolerances...)
DCR_TOL [%]	5.0		
L_TOL [%]	5.0		DCR Derating is the temperature derating factor of the copper from ambient to max operating temp.
DCR Derating	1.20		
C [µF]	2,800		Equivalent Output Filter Characteristics.
ESR [mΩ]	1.40		
ΔI_{ZERO_LOAD} [App]	4.122		Nominal Current Ripple in each inductor @Zero-Load.
ΔI_{FULL_LOAD} [App]	4.580		Nominal Current Ripple in each inductor @Full-Load

Over Current

Over Current Threshold is set fixing the per-phase threshold and the AVG threshold (*See DS for details*).
Setting the OCP threshold must also consider that, in case of OTF-VID support, this threshold must be HIGHER than the maximum deliverable current plus the OTF-VID current required to charge the output filter capacitance at 3mV/µsec.

Parameter	Value	Commercial Value	Description
DVID_Slope [mV/µSec]	3.000		Output Voltage change rate when OTF-VID considered. CPU gives directly the final VID vlaue: the reference steps by LSB increments each clock cycle up to the new programmed value.
Iextra [A]	8.400		Extra current needed to move the output filter during D-VID.
Imax + Iextra [A]	108.400		*D-VID Current is lower than OCP. The system will execute D-VID properly also at full load.(Imax+Iextra<Iocp)*
Iocp [A]	**140.000**		
Iocth [µA]	35.000		Iocth is the per-Phase over current Threshold compared to Iinfox.
Iocth_TOL [%]	2.0		Iocth Tolerance *@ 3sigma*
Phase Shedding Current	NO		Insert the Current Level @ which perform the External Phase Cut 4-->2 *Fill with "NO" or Shedding current threshold*
Shedding Rg [kΩ]	NO SHEDDING		Mount Sheddin Rg when designing 4-->2 (based on DCR_MAX, DCR Thermal Spread and Current Ripple) in order to guarantee the proper operation also when exteranlly sheddin two phases
Rg [kOhm]	1.839	1.859	Rg is designed in order to set the OC threshold per-phase to about 110% of the AVG OC threshold (worst case, 140A). $R_g = \frac{1.1 \cdot DCR_{max} \cdot I_{OCTHmin}}{N \cdot I_{OCTHmin}}$
Rg_TOL [%]	1.0		Rg Accuracy. Used for OC tolerance Calculation

Disclaimer / Revision History / Design_INPUTS / CORE_SECTION_DESIGN / NB_SECTION_DESIGN / Compensation Notes

- Q & A…