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Achieving 5 STAR Energy Efficiency p. 10

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Achieving Five-Star Energy Efficiency in Cell-Phone Chargers

Cell-phone manufacturers are demanding that no-load, offline charger power should be reduced to 30 mW or less. CamSemi's C2160 controller ICs enable designers to achieve that goal.

As product designers are keenly aware, regulators in the US and EC have been busy proposing minimum efficiency requirements for offline power supplies. The first round of regulatory requirements tackles external power supplies, such as those that recharge mobile devices.

At around 70%, the minimum acceptable efficiency during device operation is not hard to meet. Similarly, today's 250- to 300-mW requirements for no-load power dissipation are easy to accommodate, as is the EC's 150-mW specification that begins in 2011. But the 30-mW no-load target representing the new five-star rating system agreed upon by LG Electronics, Motorola, Nokia, Samsung, and Sony Ericsson entirely changes this landscape (*see Table*).

Meeting such a small no-load consumption value is not a trivial job for designers. For instance, one effect of minimizing no-load power consumption can be the creation of large voltage drops and lengthy recovery times when transitioning from no-load mode to full output power. In some cases, the circuit's output voltage falls to zero before beginning a lengthy recovery sequence.

This happens because many controller manufacturers resort to very low switching frequencies to achieve these stringent no-load power requirements, which results in the controller being unable to respond quickly to load-level changes. Designers must ensure that a circuit capable of meeting the 30-mW challenge can also start up quickly and recover well from zero- to full-load conditions.

MINIMIZING NO-LOAD POWER CONSUMPTION

Considering a circuit that meets the 30-mW no-load challenge illustrates some of the problems and solutions. This design employs the C2161PX2 or C2162PX2 controller for maximum output-power levels of 4 and 8 W, respectively. It exploits a primary-side-sensing flyback topology to construct a universal-input converter that achieves tight constant-

No-Load Consumption Score Chart
FIVE STARS = Most Energy Efficient

★★★★★	≤ 0.03 W
★★★★	> 0.03 W to 0.15 W
★★★	> 0.15 W to 0.25 W
★★	> 0.25 W to 0.35 W
★	> 0.35 W to 0.5 W
No Stars	> 0.5 W

current/constant-voltage operation without needing the optoisolator, voltage reference, and associated components that typify secondary-sensing flyback circuits *(Fig. 1)*.

A full-wave rectifier followed by an LC filter smooths and attenuates emissions for the high-voltage dc rail. For optimal performance, capacitors, Cin1 and Cin2, should be low-impedance, low-leakage types, but commodity parts with 105°C ratings are typically acceptable. Low-value resistor, Rin, provides inrush current protection and—depending upon safety-agency requirements—may be a fusible component. The circuit's quasi-resonant switching technique sufficiently reduces conducted EMI so that L1 can be low in inductance and dc resistance values.

The high-voltage rail supplies T1's primary current as well as the start-up current for IC1 via resistor Rht. Because IC1 is built using a 3.3-V CMOS process that requires a maximum 7-µA during start up, Rht can be a very high value; even so, start-up time is less than 1 sec. During operation, IC1 draws a maximum of 2 mA from the primary-side auxiliary winding and internally regulates VDD.

Overall, the power necessary to start up and keep IC1 switching at around 1 kHz under no-load conditions is about 12 to 14 mW. At around 10 mW, dummy-load resistor Rout becomes the next dominant power-consuming term. Its value balances the primary power level and ensures output-voltage stability when no external load is present. Parasitic losses elsewhere, such as in the transformer, amount to around 2 mW for a total no-load consumption of about 25 mW.

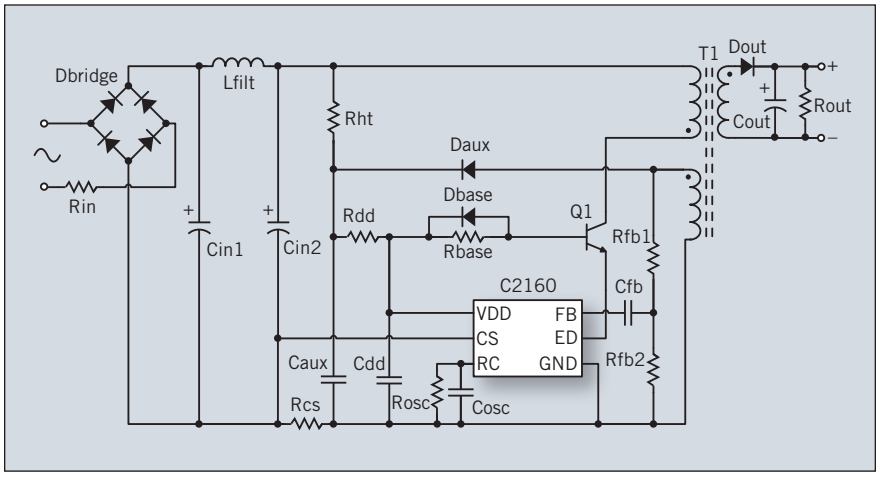

Fig. 1. Basic schematic for a primary-side sensing <30-mW no-load power-consumption design.

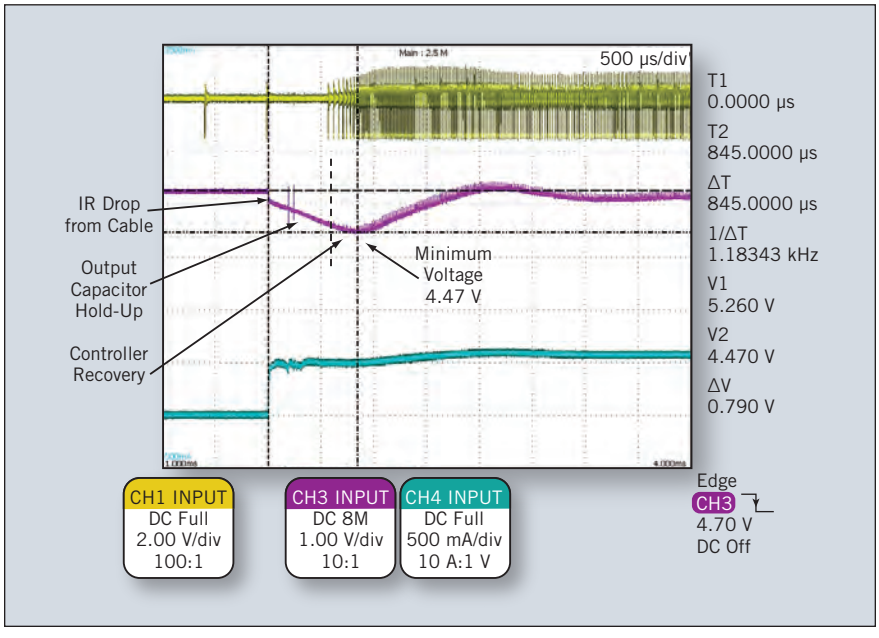

Fig. 2. Cycle-by-cycle sampling enables rapid transient response even from no-load states.

TRANSIENT RESPONSE FROM NO-LOAD CONDITIONS

Because it examines the feedback waveform cycle-by-cycle, CamSemi's tangent detection technique speeds transient response even at low switching frequencies. *Fig. 2* shows an example of the sequence of events that follows a 500-mA no-load to full-load step.

The bottom trace is the load step that creates a temporary output-voltage dip in the voltage trace above it. The first, sharp part of this dip is due to IR losses that depend upon external factors such as cable gauge. The second, slower negative ramp shows the droop due to the output capacitor discharging.

Meanwhile, the controller senses the voltage drop and immediately ramps up its switching frequency, as the top trace shows. Here, the effect

is to constrain the dip to less than 0.8 V, with the output voltage stabilizing within around 4 msec, which is well within the 10-msec maximum recovery time for CamSemi's AD-2971 reference design.

While primary-side sensing circuits are not new, the ±5% voltage and current regulation that this design achieves far exceeds the typical ±10% to ±15% performance of competing designs. The key to its performance is a proprietary, patented method of measuring the circuit's output voltage and current levels. The controller responds to output load changes by adjusting the peak current through the primary switch, Q1, and the switching frequency.

The minimum switching frequency is predominantly a product of the load that the controller and dummy load present under no-load conditions, while Cosc and Rosc determine maximum full-load frequency. For the C2161/2162PX2, this maximum lies within the range of 36 to 66 kHz.

The transformer's turns ratio establishes the maximum duty cycle, which for a universal offline design is typically set to 50% at the minimum high-voltage rail value. Power conversion always occurs in discontinuous conduction mode.

As *Fig. 1* shows, the controller switches T1 by driving Q1's emitter in cascode mode, efficiently driving a low-cost bipolar transistor rather than a relatively expensive MOSFET. Slew-rate limiting on the controller's SD pin minimizes conducted and radiated emissions.

Resistors Rfb1 and Rfb2 scale the waveform that develops across T1's primary sense winding, while Cfb1 provides dc blocking that allows the controller to centre this feedback waveform between the power-supply rail voltages. This allows the chip to examine the entire waveform rather than just the positive-going portion that competing schemes typically sample (*Fig. 3*).

In *Fig. 3*, FB is the waveform at the chip's feedback pin, while Ip and Is represent the current waveforms across the primary-side current-sense resistor, Rcs. It's possible to observe the output voltage only during the flyback time, $t_{DCHARGE}$, which for best accuracy requires sampling at the knee point when current falls to zero, as Is confirms.

Precisely determining the knee point is critical. CamSemi's proprietary tangent-detection technique uses a combination of analog, high-speed sampling, and signal-processing techniques to assess the waveform's rate-of-change (dV/dT) as it transitions from the $t_{DCHARGE}$ state to fall to the zero-crossing point.

In *Fig. 4a* the slope during $t_{DCHARGE}$ is a function of output current and circuit resistance for a given power rating, while the period in *Fig. 4b* between the knee and zero-crossing points is one-quarter of a sinewave whose frequency corresponds to the transformer's resonant frequency. Selecting a reference dV/dT between these two known slopes establishes the sample point *(Fig. 4c)*.

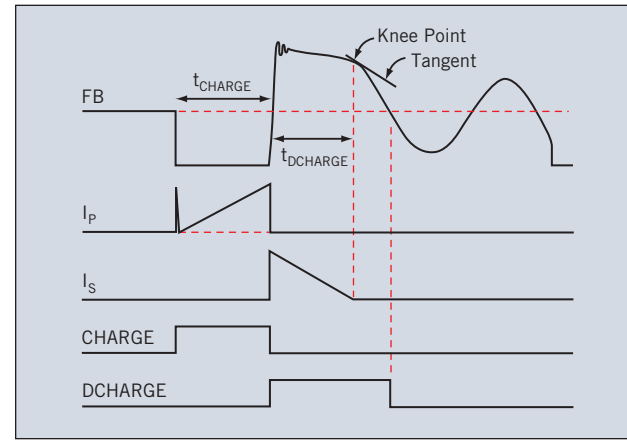

Fig. 3. Feedback and current waveforms and sampling points.

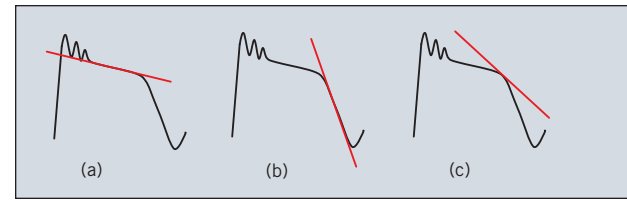

Fig. 4. A proprietary tangent detection technique improves voltage and current regulation accuracy. In Fig. 4a, slope dv/dt is determined by output current and circuit resistance known based on given power rating. In 4b, slope dv/dt is determined by resonant frequency of transformer, known and based on transformer design. Fig. 4c shows that by selecting an on-chip reference (dv/dt) between these two slopes, you know when to sample the output voltage.

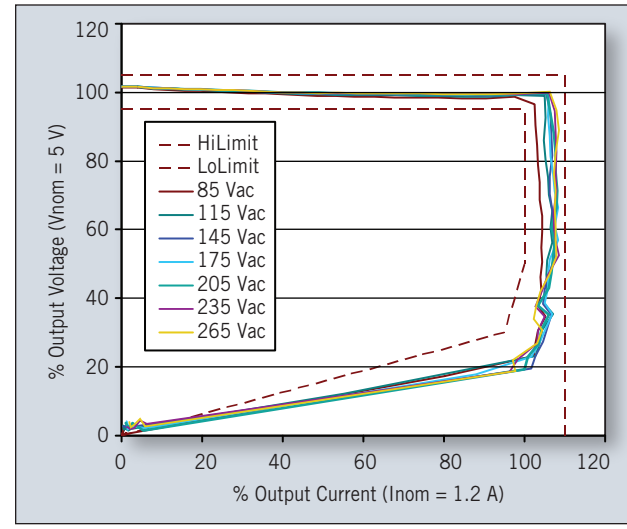

Fig. 5. The C2161PX2 and C2162PX2 achieve ±5% voltage and current regulation with no secondary-side sensing components.

Because FB directly provides the t_{CHARGE} measurement and $t_{DCHARGE}$ is known, it is possible to determine the output-current level by sensing and averaging the voltage, Ip, that current-sense resistor Rcs generates. A short leading-edge blanking period immediately follows, Q1, turning on to

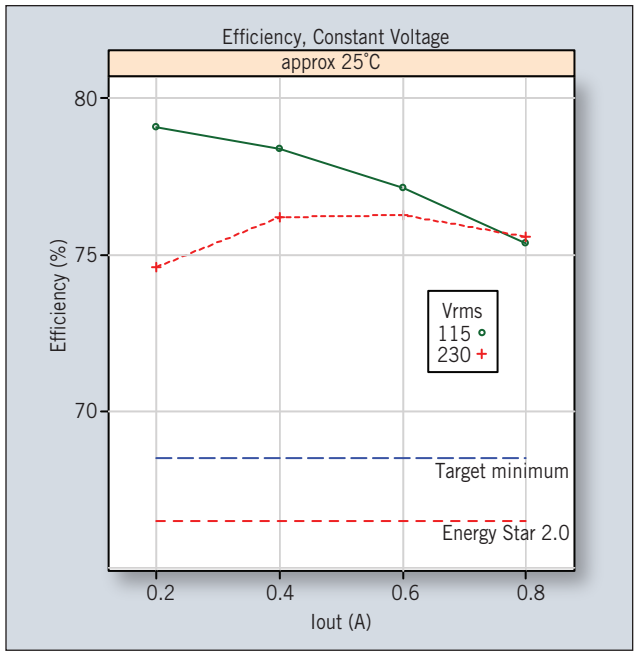

Fig. 6. Four-point efficiency measurements for a 4.8-W charger easily exceeds regulatory requirements.

discard the spike that appears as Ip begins to ramp up.

The secondary current calculation then becomes:

$$I_{OUT} = K \frac{t_{DCHARGE}}{t_{CHARGE}} (I_P) \quad (1)$$

where K is the transformer's turns ratio.

The patented tangent-detection technique is crucial in achieving this best-in-class current-regulation performance. *Fig. 5* shows the typical CC/CV charger output characteristic that the C2161/2162PX2 achieves while constraining output voltage ripple to less than 200 mV peak-to-peak without needing secondary-side sensing components.

Another desirable attribute that tangent detection enables is close-to-zero voltage switching for the transformer's primary current, increasing efficiency and minimizing stress on power-switch components while reducing emissions. The worst-case margin for conducted EMI that the AD-2971 achieves for a universal-input 4.8-W charger is greater than 6 dB below EN 55022 limits, while its four-point average of 75% for constant-voltage mode exceeds Energy Star V2 and EC Code-of-Conduct V4 requirements (*Fig. 6*).