Target Datasheet, Version 0.5, 08 August 2008

ICE1HS01G

Half-Bridge Resonant Controller

Power Management & Supply

Never stop thinking.

ICE1HS01G

Revision History:	**08 August 2008**	Target Datasheet
Previous Version:	0.5	

Page	Subjects (major changes since last revision)

For questions on technology, delivery and prices please contact the Infineon Technologies Offices in Germany or the Infineon Technologies Companies and Representatives worldwide: see our webpage at http://www.infineon.com

CoolMOS™, CoolSET™ are trademarks of Infineon Technologies AG.

Edition 08 August 2008

Published by
Infineon Technologies AG
81726 Munich, Germany

Legal Disclaimer
The information given in this document shall in no event be regarded as a guarantee of conditions or characteristics. With respect to any examples or hints given herein, any typical values stated herein and/or any information regarding the application of the device, Infineon Technologies hereby disclaims any and all warranties and liabilities of any kind, including without limitation, warranties of non-infringement of intellectual property rights of any third party.

Information
For further information on technology, delivery terms and conditions and prices, please contact the nearest Infineon Technologies Office (www.infineon.com).

Warnings
Due to technical requirements, components may contain dangerous substances. For information on the types in question, please contact the nearest Infineon Technologies Office.
Infineon Technologies components may be used in life-support devices or systems only with the express written approval of Infineon Technologies, if a failure of such components can reasonably be expected to cause the failure of that life-support device or system or to affect the safety or effectiveness of that device or system. Life support devices or systems are intended to be implanted in the human body or to support and/or maintain and sustain and/or protect human life. If they fail, it is reasonable to assume that the health of the user or other persons may be endangered.

ICE1HS01G

Half-Bridge Resonant Controller

ICE1HS01G
PG-DSO-8

Product Highlights

- **Minimum number of external components**
- **High accuracy oscillator**
- **Two-level over current protection**
- **Over load/open loop protection**
- **Mains undervoltage protection with adjustable hysteresis**
- **Adjustable blanking time for over load protection and restart**

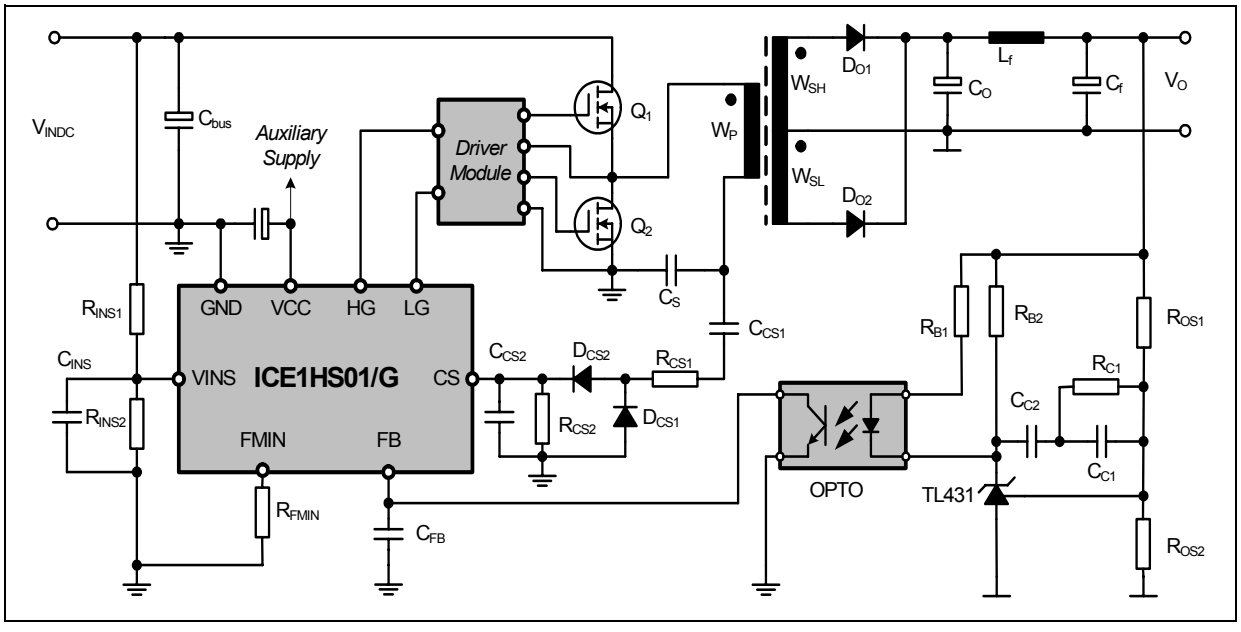
Features

- DSO8 package
- Maximum 600kHz switching frequency
- Adjustable minimum switching frequency with high accuracy
- 50% duty cycle
- Mains input under votlage protection with adjustable hysteresis
- Two levels of overcurrent protection: frequency shift and latch off
- Open-loop/over load protection with extended blanking time
- Built-in digital and nonlinear softstart
- Adjustable restart time during fault protection period

Applications

- LCD/PDP TV
- AC-DC adapter
- Audio SMPS

Typical Application Circuit



Type	Package
ICE1HS01G	PG-DSO-8

Table of Contents Page

1 Pin Configuration and Functionality

1.1 Pin configuration with PG-DSO-8

Pin	Symbol	Function
1	FMIN	Minimum switching frequency
2	CS	Current sense
3	FB	Feedback voltage
4	VINS	Input voltage sense
5	GND	IC ground
6	LG	Low side gate drive
7	HG	High side gate drive
8	VCC	IC power supply

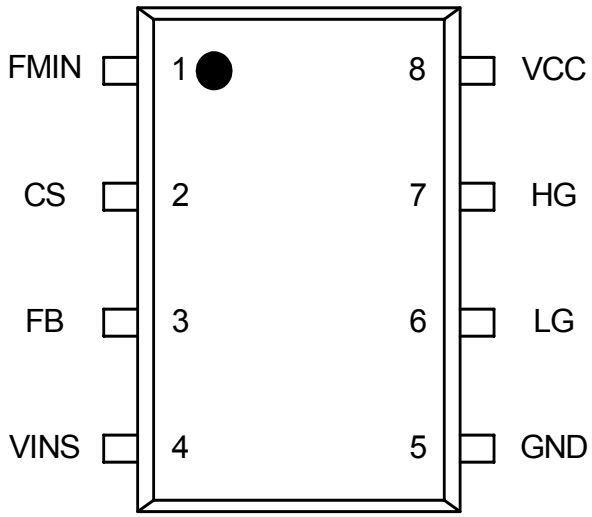


Figure 1 Pin configuration with PG-DSO-8

1.2 Pin Functionality

FMIN (minimum switching frequency)
An external resistor is connected between this pin and the ground. The voltage of this pin is constant during operation and thus the resistance determines the current flowing out of this pin. The minimum switching frequency is determined by this current. The maximum switching frequency and the switching frequency during soft start are also related to the current flowing out of FMIN pin.

CS(current sense)
The current sense signal is fed to this pin. Inside the IC, two comparators are provided. If the voltage on CS pin is higher than the first threshold, IC will increase the switching frequency to limit the maximum output power of the converter. If the voltage on this pin exceeds the second threshold, IC will be latched off immediately.

FB (feedback)
This pin is connected to the collector of the opto-coupler. Internally, during normal operation, this pin is connected to reference voltage source with a pull-up resistor(R_{FB}). The IC uses the voltage on this pin to adjust the switching frequency within the range of maximum and minimum frequency set by FMIN pin. If FB voltage is higher than V_{FBH} for a certain blanking time, an extended timer will be started. If over load/ open loop protection exists longer than the extended blanking time, IC will enter auto-restart mode. An off timer starts from the instant IC stops switching till IC starts another soft start. This off time will be determined by the resistors and capacitor connected to VINS pin.

VINS (mains input voltage sense)
The mains input voltage is fed to this pin via a resistive voltage divider. If the voltage on VINS pin is higher than the threshold V_{INSON}, IC will start to operate with softstart when VCC increases beyond turn on threshold. During operation, if the voltage on this pin falls below the threshold V_{INSON}, IC will stop switching until the voltage on this pin increases again. When IC goes into over load protection mode, it will stop the switches and try to restart after a period of time. The period is adjustable by connectting different capacitors between this pin and ground.

GND (ground)
IC common ground.

LG (low side gate drive)
Low side power MOSFET driver.

HG (high-side gate drive)
Upper side power MOSFET driver.

VCC (IC power supply)
Supply voltage of the IC.

2 Representative Block Diagram

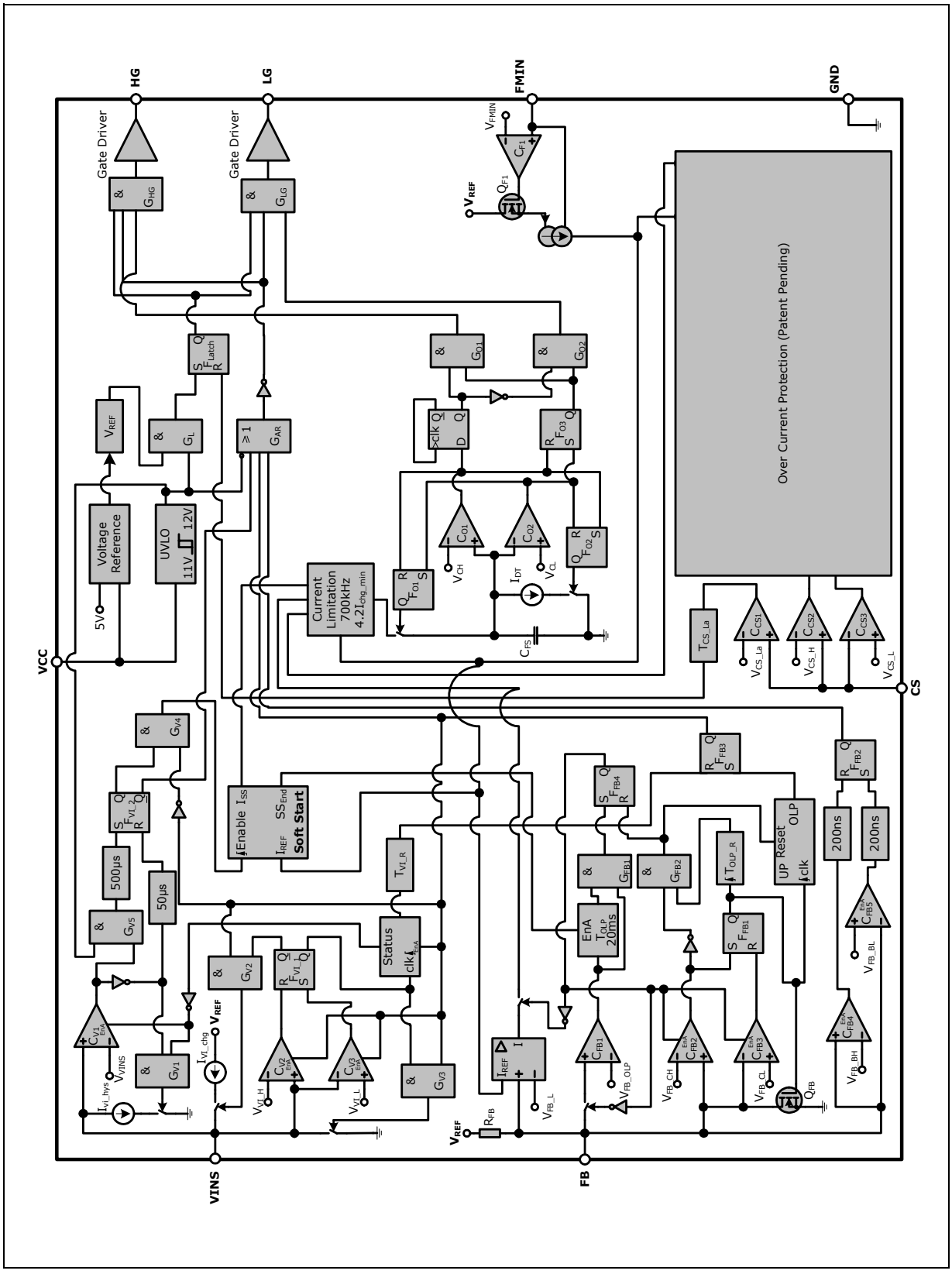


Figure 2 Representative Block Diagram

3 Functional description

The controller ICE1HS01G with two gate outputs is specially designed for LLC resonant half-bridge converters. An oscillator with accurately-programmed frequency range is built inside the IC. The two gate signals are obtained by passing the signal out from the oscillator through a divide-by-two flip-flop. Therefore, two signals are of exactly 50% duty cycle and 180° out of phase. To guarantee the zero-voltage-switching and safe operation in half-bridge topologies, a fixed dead time of 450ns is inserted in each internal when one switch is turned off and the other is turned on.

For LLC resonant half-bridge converter, the output voltage is regulated by changing the switching frequency. ICE1HS01G offers the designer to choose suitable operation frequency range by programming the oscillator with one single resistor.

In addition, ICE1HS01G offers a programmed soft-start function to limit both the inrush current and the overshoot in output voltage.

To protect the system during operation, mains input under-voltage protection and over-current protection are integrated in ICE1HS01G as well.

3.1 Oscillator and Pulse Frequency Modulation

The oscillator is programmed with only one external resistor R_{FMIN} connected to FMIN pin. The trimmed capacitor C_{FS} is built inside the IC with high accuracy. The simplified oscillator circuit is shown in Figure 3.

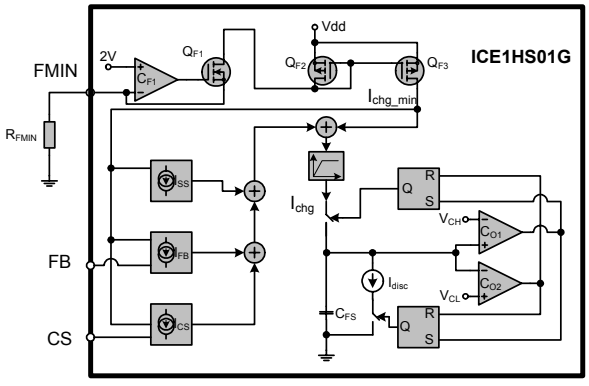


Figure 3 Simiplified oscillator circuit

The charge current I_{chg} is sum of four current which are I_{chg_min}, I_{FB}, I_{CS} and I_{SS}. Everytime the capacitor C_{FS} is charged by I_{chg} to V_{CH}, the upper switch is turned off and C_{FS} will be discharged through I_{disc}. The charge time determines the on time for gate signal. The discharge time determines the dead time during transition from one gate off to another gate on. The switching waveforms of the oscillator and gate signals are shown in Figure 4.

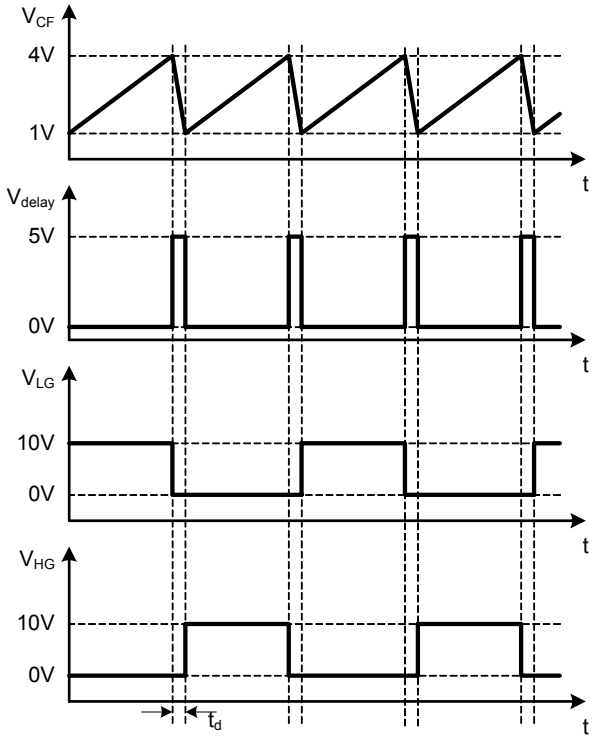


Figure 4 Oscillator waveforms

According to Figures 3 and 4, The on time of each gate can be obtained as

$$T_{on} = \frac{3C_{FS}}{I_{chg}} \quad [1]$$

The switching frequency can be obtained as

$$f_s = \frac{1}{2\left(\frac{3C_{FS}}{I_{chg}} + T_d\right)} \quad [2]$$

where the dead time is fixed to 450ns.

3.1.1 Minimum charge current

The voltage on pin FMIN is a constant of 1.5V during normal operation. The resistor R_{FMIN} determines the current(I_{FMIN}) flowing out from FMIN pin. One-tenth of I_{FMIN} is defined as the minimum charging current(I_{chg_min}), which in turn defines the minimum switching frequency as follows.

However, the minimum charge current can not be decreased further even if R_{FMIN} is higher than 35kΩ. It has a lower limit value, which is correponding to the 45kHZ minimum switching frequency. The relation

between minimum switching frequency and R_{FMIN} is shown in Figure 5.

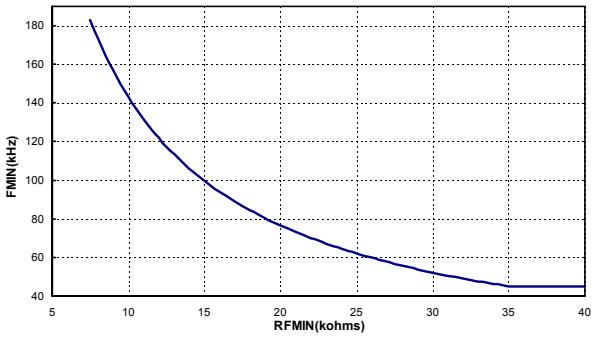


Figure 5 FMIN versus R_{FMIN}

In addition, in order to prevent pin FMIN from being shorted to the ground, IC will be latched in case the R_{FMIN} used is less than 4.8kΩ.

3.1.2 Feedback regulation current I_{FB}

The output information is fed into the controller through feedback voltage. If the output power is higher, the feedback voltage will be higher, which will cause the switching frequency to decrease and vice versa.

The regulation of switching frequency is achieved by changing the charging current. An accurate operational transconductance amplifier (OTA) is used to translate the feedback voltage V_{FB} into to current I_{FB}. The effective range of feedback voltage is from 1V to 4V. The relationship between I_{FB} and V_{FB} is shown in Figure 6.

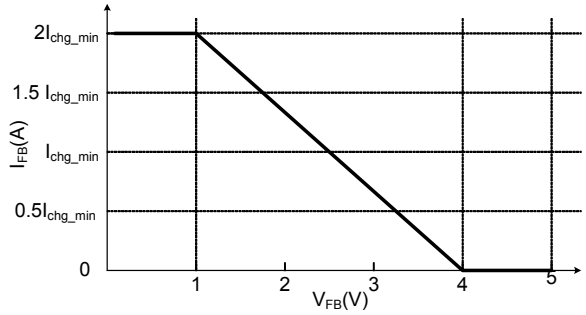


Figure 6 I_{FB} versus V_{FB}

At very light load condition, the frequency may not be high enough to regulate the output voltage. In order to avoid this case, the feedback signal V_{FB} is continuously monitored. When V_{FB} drops below V_{FB_off} , the switching signal will be disabled after a fixed blanking time T_{FB}. V_{FB} will then rise as V_{out} starts to decrease due to no switching signal. Once V_{FB} exceeds the threshold V_{FB_on}, the IC resumes to normal operation.

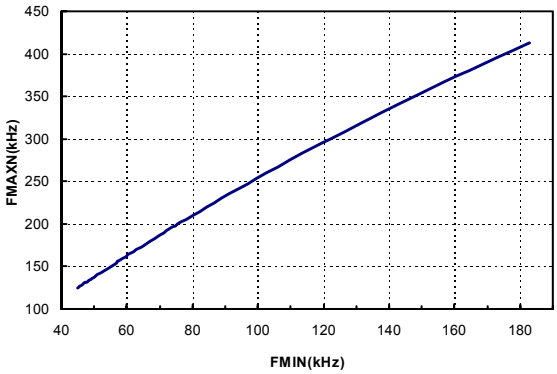


Figure 7 Fmax_n versus Fmin during normal operation

3.1.3 current sense current I_{CS}

In LLC resonant topologies, it is necessary to limit the resonant current in case of short circuit or other fault conditions. It is achieved by adding another current Ics to the charging current. I_{CS} is limited to 3 times of the minimum charge current.

3.1.4 soft start current I_{SS}

To limit the inrush current and output overshoot during start up, the switching frequency shall be necessary high at start up. The switching frequency will change gradually toward the minimum switching frequency until the feedback voltage comes into regulation. The switching frequency will then go to desired value according to load and input conditions. The soft start current also has a upper limit of 3 times of minimum charge current. Details of soft start will be shown later.

3.1.5 Charge current I_{chg}

The charge current I_{chg} is the sum of the four parts including I_{chg_min}, I_{FB}, I_{SS} and I_{CS}. To limit the maximum switching frequency, maximum value of I_{chg} is 4 times of I_{chg_min}. To limit the maximum switching frequency at 500kHz, the charge current will limited at 109μA even if $4I_{chg\_min}$ is higher than this value.

In summary, the maximum charge current during normal operation is $3I_{chg\_min}$ while the maximum charge current during fault contion or softstart is $4I_{chg\_min}$. Figure 7 shows the maximum switching frequency versus minimum switching frequency during normal operation. Figure 8 shows the maximum switching

frequency during fault and startup conditions versus minimum switching frequency.

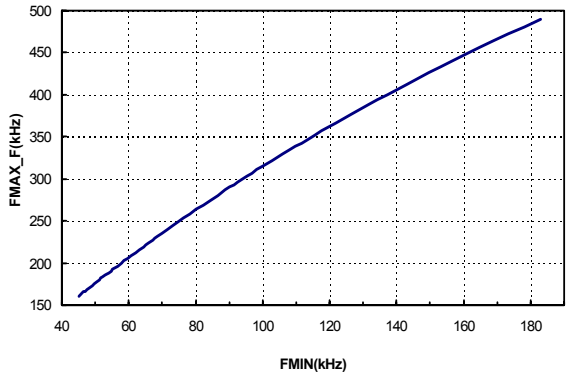


Figure 8 Fmax_f versus Fmin during fault and startup conditions

3.2 IC power supply

The controller ICE1HS01G is targetting at applications with auxiliary power supply. In most cases, a front-end PFC pre-regulator with a PFC controller is used in the same system.

The controller ICE1HS01G starts to operate when the supply voltage V_{VCC} reaches the on-threshold, V_{VCCon} of 12V. The minimum operating voltage after turn-on, V_{VCCoff}, is at 11V. The maximum supply voltage V_{VCCmax} is 18V.

3.3 Soft start

At the beginning of the startup phase, the IC provides a soft start with duration of 32ms with 32 steps. During this period, the switching frequency is controlled internally by changing the current I_{SS}. Figure 9shows how the charging current is changing according to time during soft start.

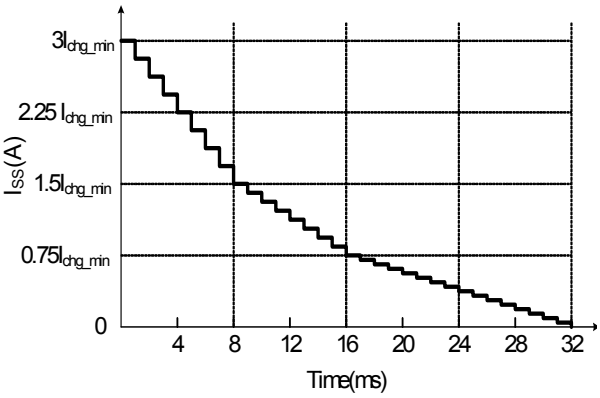


Figure 9 I_{SS} during softstart

During soft start, the overload protection is disabled because FB voltage is high.

3.4 Current sense

Current sense in LLC half bridge converters is for protection purpose. The voltage of resonant capacitor C_S is the sum of the resonant voltage and the dc voltage which is equal to half of the input bus voltage. If resonant current is higher, then the voltage on C_S is higher.The current informations for both primary side and secondary side are almost the same and can be obtained by dividing and filtering the resonant voltage. The circuit is shown in Figure 10.

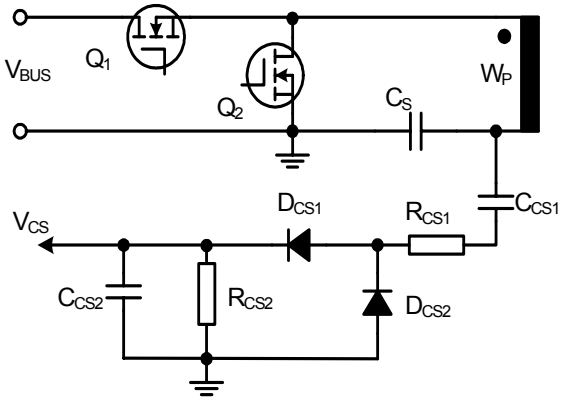


Figure 10 Current sense circuit

3.5 Over current protection

The controller ICE1HS01G incooperates two-level over current protection. In case of over-load condition, the lower level OCP will be triggerred, the switching frequency will be increased according to the duration and power of the over load. The higher level OCP is used to protect the converter if transformer winding is shorted, the IC will be latched immediately.

If V_{CS} is higher than 0.8V, IC will boost up the switching frequency. If Vcs is lower than 0.75V, IC will resume to normal operation gradually. If V_{CS} is always higher than 0.8V for 1.5ms, the frequency will rise to its maximum level. And vice versa.

To sum up, ICE1HS01G will increase the switching frequency to limit the resonant current in case of temporary over-load and will also decrease the switching frequency to its normal value after over-load condition goes away.

3.6 Mains Input Voltage Sense

The working range of mains input voltage needs to be specified for LLC resonant converter. It is important for the controller to have input voltage sensing function and protection features, which lets the IC stop switching when the input voltage falls below the specified range and restarts when the input voltage increases back within the range. The mains input voltage sensing circuit is shown Figure 2. With the

current source I_{hys} connected between VINS and Ground, an adjustable hysteresis between the on and off input voltage can be created as

$$V_{HYS} = R_{INS1} \cdot I_{hys} \quad [3]$$

The mains input voltage is divided by R_{INS1} and R_{INS2}. A current source I_{hys} is connected from VINS pin to ground in the IC. If the on and off threshold for mains voltage is V_{mainon} and $V_{mainoff}$, the resistors can be decided as

$$R_{INS1} = \frac{V_{mainon} - V_{mainoff}}{I_{hys}} \quad [4]$$

$$R_{INS2} = R_{INS1} \cdot \frac{V_{INSON}}{V_{mainoff} - V_{INSON}} \quad [5]$$

3.7 Over load protection

In case of open control loop or output over load fault, the FB voltage will increase to its maximum level. If FB voltage is higher than V_{FBH} and this condition last longer than a fixed blanking time of T_{OLP} (20ms), the IC will start the extended blanking timer. The extended blanking timer is realized by charging and discharging the filter capacitor C_{FB} via the pull up resistor R_{FB} and Q_{FB}. The circuit for extended blanking timer is shown in Figure 11.

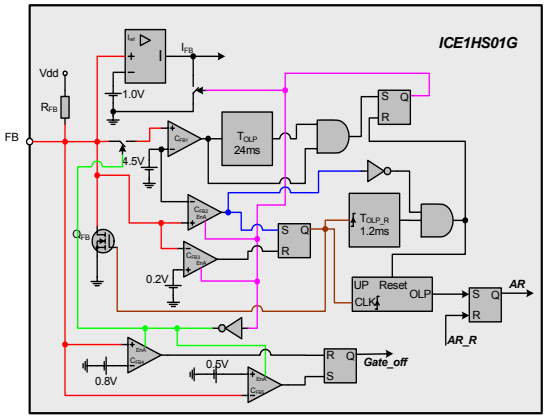


Figure 11 Circuit connected to FB pin

The FB voltage waveform during a OLP period is shown in Figure 12. After FB voltage has been higher than V_{FBH} for the fixed blanking time t1 shown in Figure 11, IC will use internal switch Q_{FB} to discharge V_{FB} to V_{FBL}. After the switch Q_{FB} is released, C_{FB} will be charged up by Vdd through R_{FB}. The time needed for C_{FB} being charged to V_{FBH} can be calculated as

$$t_{chg} = -\ln\left(\frac{V_{dd} - V_{FBH}}{V_{dd} - V_{FBL}}\right) \cdot R_{FB} \cdot C_{FB} \quad [6]$$

If C_{FB} is 10nF, the time is about 439us. After V_{FB} reaches V_{FBH}, an internal counter will increase by 1 and the capacitor is discharged to zero voltage by Q_{FB} again. The charging and discharging process of C_{FB} will be repeated for N_{OLP_E} times if the fault condition still exist. After the last time of N_{OLP_E} the FB voltage is pulled down to zero, IC will stop the switch when FB voltage rises to V_{FBH} again. This is called over load/ open loop proteciton. During the charging and discharging period, the IC will operate with frequency determined by I_{chg_min} and I_{CS}.

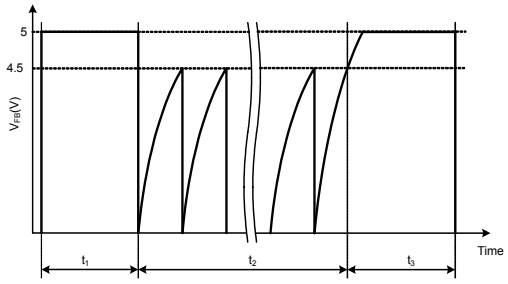


Figure 12 FB voltage waveform during over load protection

If the converter returns to normal operation during the extended blanking time period, FB voltage can not goes up to V_{FBH} again. Therefore, after FB voltage is discharged to zero voltage, if it can not goes up to V_{FBH} within T_{OLP_R}, IC will reset all the fault timer to zero and return to normal operation.

After IC enters into OLP, both switches will be stopped. However, the IC remains active and will try to start with soft start after an adjustable period. This period is realized by charging and discharging the capacitor C_{INS} connected to VINS pin for N_{OLP_R} times. The time is therefore determined by the capacitor C_{INS} and resistor R_{INS1} and R_{INS2}. The circuit implementation of the adjustable off time is shown in Figure 13 and Figure 14 shows the voltage waveform of VINS in this case.

As shown in Figure 14, the C_{INS} is discharged to V_{INS_L} when IC goes into OLP at time t1. After that, an internal constant current source I_{INST} is turned on to charge C_{INS}. Once the voltage on VINS is charged to V_{INS_H}, the current source will be turned off and C_{INS} is discharged by another switch Q3 to V_{INS_L} again. The charging and discharging of C_{INS} is thought as one cycle. The cylce time is also influenced by the bus voltage. The charging time t_{cha} and discharging time t_{disc} can be respectively approximated as

$$t_{cha} = -\ln\left(\frac{\left(V_{BUS} \cdot \frac{R_{eq}}{R_{INS1}}\right) + (I_{INST} \cdot R_{eq}) - V_{INSH}}{\left(V_{BUS} \cdot \frac{R_{eq}}{R_{INS1}}\right) + (I_{INST} \cdot R_{eq}) - V_{INSL}}\right) \cdot R_{eq} \cdot C_{INS} \quad [7]$$

$$t_{disc} = -\ln\left(\frac{V_{BUS}\cdot\frac{R_{eq2}}{R_{INS1}} - V_{INSL}}{V_{BUS}\cdot\frac{R_{eq2}}{R_{INS1}} - V_{INSH}}\right)\cdot R_{eq2}\cdot C_{INS} \quad [8]$$

In [7], R_{eq} is the equivalent resistance for parallelling of R_{INS1} and R_{INS2}. In [8], R_{eq2} is the equivalent resistance for parallelling of R_{INS1}, R_{INS2} and R_{Q3}(500 ohm typically). IC will repeat the charging and discharging process for N_{OLP_R} times. After that, IC will turn off the switches for both charging and discharging. In addition, the current source for hysteresis will be turned on and another blanking time of T_{BL_VINS}, the time between t2 and t3 as shown in Fiugre 14, will be added so that VINS pin fully recovers and represents the bus voltage information. IC will start the soft start after the additional blanking time in case V_{VINS} is higher than the V_{VINSon}.

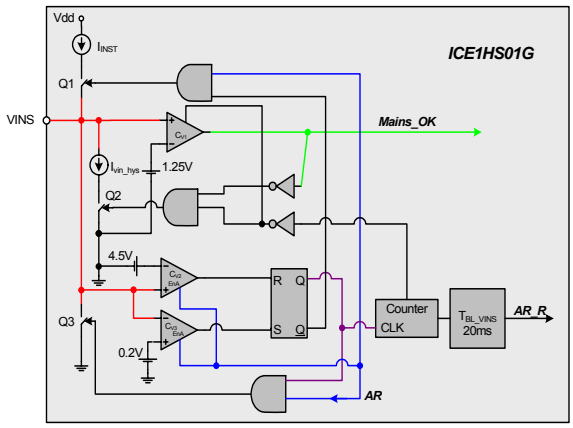


Figure 13 Circuit connected to VINS pin

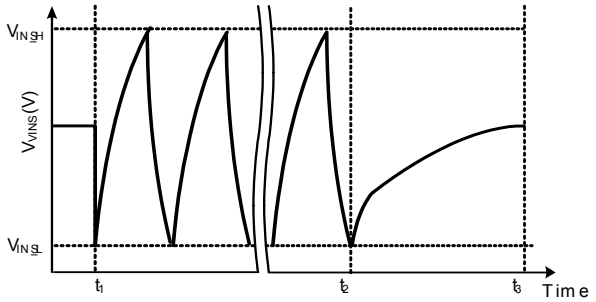


Figure 14 VINS voltage waveform during blanking time after OLP and before IC restarts

4 Electrical Characteristics

Note: All voltages are measured with respect to ground (Pin 8). The voltage levels are valid if other ratings are not violated.

4.1 Absolute Maximum Ratings

Note: Absolute maximum ratings are defined as ratings, which when being exceeded may lead to destruction of the integrated circuit. For the same reason make sure, that any capacitor that will be connected to pin 7 (VCC) is discharged before assembling the application circuit.

Parameter	Symbol	Limit Values		Unit	Remarks
		min.	max.		
VCC Supply Voltage	V_{VCC}	-0.3	18	V	
V_{HG} Voltage	V_{LG}	-0.3	18	V	
V_{LG} Voltage	V_{LG}	-0.3	18	V	
CS voltage	V_{CS}	-0.3	5	V	
FB voltage	V_{FB}	-0.3	5	V	
VINS voltage	V_{VINS}	-0.3	5	V	
FMIN voltage	V_{FMIN}	-0.3	5	V	
Maximum source current on FMIN	I_{FMIN}		2.5	mA	
Junction Temperature	T_j	-40	125	°C	
Storage Temperature	T_S	-55	150	°C	
Thermal Resistance Junction-Ambient for PG-DSO-8	R_{thJA}(DSO)	-	185	K/W	PG-DSO-8
ESD Capability	V_{ESD}	-	2	kV	Human body model[1)]

1) According to EIA/JESD22-A114-B (discharging a 100pF capacitor through a 1.5kΩ series resistor)

4.2 Operating Range

Note: Within the operating range the IC operates as described in the functional description.

Parameter	Symbol	Limit Values		Unit	Remarks
		min.	max.		
VCC Supply Voltage	V_{VCC}	10.2	18	V	
Junction Temperature	T_{jCon}	-25	125	°C	

4.3 Characteristics

4.3.1 Supply Section

Note: The electrical characteristics involve the spread of values guaranteed within the specified supply voltage and junction temperature range T_J from – 25 °C to 125°C. Typical values represent the median values, which are related to 25°C. If not otherwise stated, a supply voltage of V_{CC} = 15 V is assumed.

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Start up Current	$I_{VCCstart}$	-	300		µA	V_{VCCon}-0.1V
Supply Current in operation with inactive gate	I_{VCCop}	-		3	mA	no switching;
Supply Current in normal operation with active gate	$I_{VCCactive}$	-	7		mA	Freq=75kHz R_{FMIN}=20kΩ V_{FB}=4.2V, V_{CS}=0V V_{VCC}=15V
VCC Turn-On Threshold	V_{VCCon}	11.3	12	12.7	V	
VCC Hysteresis	V_{VCChys}	0.9	1	1.1	V	
VCC Turn-Off Threshold	V_{VCCoff}	-	V_{VCCon} - V_{VCChys}	-	V	
Trimmed Reference Voltage	V_{REF}	4.90	5.0	5.10	V	I_{FB}=0

4.3.2 Oscillator Section

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Minimum switching frequency	F_{MIN}	49.5	51	52.5	kHz	R_{FMIN}=30kΩ;
Maximum switching frequency during normal operation	F_{MAX_N}	ND	140	ND	kHz	R_{FMIN}=30kΩ;V_{FB}=4.2V, V_{CS}=0V, after softstart
Maximum switching frequency during protection	F_{MAX_P}		180		kHz	R_{FMIN}=30kΩ;V_{FB}=4.2V, V_{CS}=1V, soft start first cycle
Absolute Minimum switching frequency	F_{MIN_abs}	42.3	45	47.7	kHz	R_{FMIN}=36kΩ,V_{FB}=4.2V, V_{CS}=0V, after softstart
Maximum FMIN resistance	R_{FMIN_MAX}		35		kΩ	Not subject to test
Minimum FMIN resistance	R_{FMIN_MIN}		5.1		kΩ	Not subject to test
Absolute Maximum switching frequency	F_{MAX_abs}	560	600	640	kHz	R_{FMIN}=6.2kΩ, V_{FB}=0.9V, V_{CS}=1V, soft start first cycle
Reference voltage on FMIN	V_{OSCRef}	1.44	1.5	1.56	V	
Dead time	T_d	340	380	420	ns	
Oscillation duty cycle	D	48	50	52	%	based on calculation

4.3.3 Input voltage sense

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Input voltage on threshold	V_{VINSon}	1.2	1.25	1.3	V	
Bias current on VINS pin	I_{hys}	9	12	15	µA	
Blankint time for leaving mains undervoltage protection	T_{VINS_out}		500		µs	
Blanking time for entering mains under voltage protection	T_{VINS_in}		50		µs	

4.3.4 Current sense

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
overcurrent protection low	V_{CSL}		0.8		V	
Hysteresis voltage for overcurrent protection low			50		mV	
overcurrent protection high	V_{CSH}		1.6		V	
Blanking time for OCP latch	T_{OCP_L}	_	300	_	ns	
Maximum switching frequency during protection	F_{MAX_C}		180		kHz	R_{FMIN}=30kΩ;V_{FB}=4.2V, V_{CS}=1V, after soft start and 2ms after V_{CS} higher than 0.8V
Counter input voltage high	V_{CS_CH}		4.5		V	Not subject to test
Counter input voltage low level	V_{CS_CL}		0.5		V	Not subject to test
Blanking time after each gate is turned on	T_{LEB}		250		ns	Not subject to test

Note: *ND means “not defined” at current stage.*

4.3.5 Soft start

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
soft start timer	T_{SS}	-	1	-	ms	Test as a 32ms softstart time
soft start steps	N_{SS}		32			
ratio of I_{SS} over I_{chgmin}		-	3	-		Not subject to test
soft start frequency	F_{ss_step}	162	179	197	kHz	R_{FMIN}=30kΩ; Td=450ns; first cycle softstart

4.3.6 Feedback

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Feedback voltage below which there is no regulation	V_{FB_min}		1		V	
Feedback voltage above which there is no regulation	V_{FB_max}		4		V	
Pull up resistance	R_{FB}	15	20	25	kΩ	
Feedback voltage below which there is no switch	V_{FB_off}		0.2		V	
Feedback voltage above which IC resumes switch	V_{FB_on}		0.3		V	
Blanking time for switch on and off	T_{FB}		200		ns	

Note: *The trend of all the voltage levels in the Control Unit is the same regarding the deviation except* V_{VCCOVP}

4.3.7 Over load/Open loop protection

Feedback voltage for open loop/over load protection	V_{FBH}		4.5		V	
Feedback votlage high level for extended timer	V_{FB_CH}		4.5		V	
Feedback votlage low level for extended timer	V_{FB_CL}		0.5		V	
Fixed Blanking time for open loop/over load protection	T_{OLP_F}	-	20	-	ms	
Maximum time for FB voltage to goes up to V_{FBH} during extended blanking timer	T_{OLP_R}	-	1.28	-	ms	
Extended counter	N_{OLP_E}		512			
Charging current on VINS pin for restart time	I_{INST}		650		µA	
Maximum voltage on VINS pin charged by I_{INST}	V_{INS_H}		4.5		V	
Minimum voltage on VINS pin pulled down by Q_{R_L}	V_{INS_L}			0.5	V	
Restart counter number	N_{OLP_R}		2048			
Blanking time before IC restarts after restart counter reaches 2048	T_{BL_VINS}	-	20	-	ms	

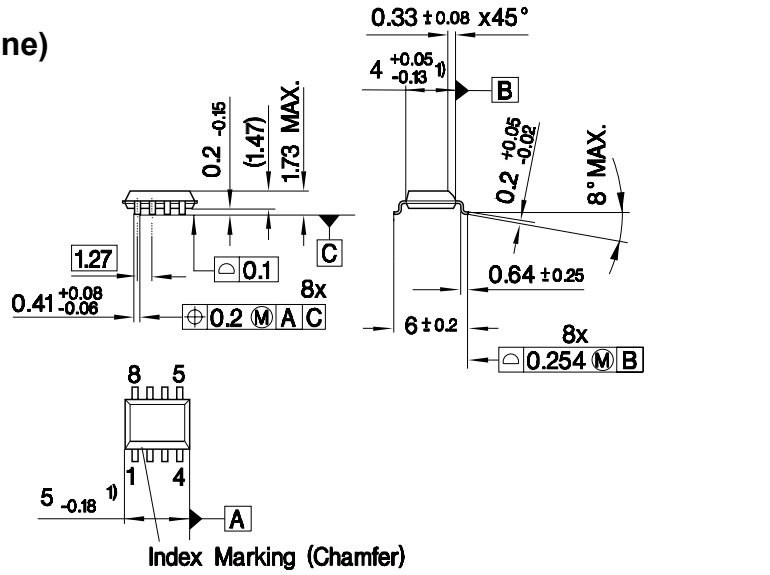
4.3.8 Gate driver

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Output voltage at logic low	$V_{GATElow}$		-	1.5	V	V_{VCC}=5V I_{OUT} = 20mA
Output voltage at logic high	$V_{GATEhigh}$		9		V	V_{VCC}=V_{VCCoff}+0.2V C_L=2.2nF
Output voltage active shut down	$V_{GATEasd}$		1.0		V V	V_{VCC} = 5V I_{OUT} = 20mA
Rise Time	t_{rise}	-	100	-	ns	C_L = 2.2nF
Fall Time	t_{fall}	-	25	-	ns	C_L = 2.2nF
GATE current, Peak Rising Edge	I_{GATE_R}	1		-	A	C_L = 2.2nF[1)]
GATE current, Peak Falling Edge	I_{GATE_F}	-	-	1.5	A	C_L = 2.2nF[1)]

1) Design characteristics (not meant for production testing)

5 Outline Dimension

PG-DSO-8
(Plastic Dual Small Outline)



1) Does not include plastic or metal protrusion of 0.15 max. per side

Figure 15 PG-DSO-8

*Dimensions in mm

Total Quality Management

Qualität hat für uns eine umfassende Bedeutung. Wir wollen allen Ihren Ansprüchen in der bestmöglichen Weise gerecht werden. Es geht uns also nicht nur um die Produktqualität – unsere Anstrengungen gelten gleichermaßen der Lieferqualität und Logistik, dem Service und Support sowie allen sonstigen Beratungs- und Betreuungsleistungen.

Dazu gehört eine bestimmte Geisteshaltung unserer Mitarbeiter. Total Quality im Denken und Handeln gegenüber Kollegen, Lieferanten und Ihnen, unserem Kunden. Unsere Leitlinie ist jede Aufgabe mit „Null Fehlern“ zu lösen – in offener Sichtweise auch über den eigenen Arbeitsplatz hinaus – und uns ständig zu verbessern.

Unternehmensweit orientieren wir uns dabei auch an „top“ (Time Optimized Processes), um Ihnen durch größere Schnelligkeit den entscheidenden Wettbewerbsvorsprung zu verschaffen.

Geben Sie uns die Chance, hohe Leistung durch umfassende Qualität zu beweisen.

Wir werden Sie überzeugen.

Quality takes on an allencompassing significance at Semiconductor Group. For us it means living up to each and every one of your demands in the best possible way. So we are not only concerned with product quality. We direct our efforts equally at quality of supply and logistics, service and support, as well as all the other ways in which we advise and attend to you.

Part of this is the very special attitude of our staff. Total Quality in thought and deed, towards co-workers, suppliers and you, our customer. Our guideline is “do everything with zero defects”, in an open manner that is demonstrated beyond your immediate workplace, and to constantly improve.

Throughout the corporation we also think in terms of Time Optimized Processes (top), greater speed on our part to give you that decisive competitive edge.

Give us the chance to prove the best of performance through the best of quality – you will be convinced.

http://www.infineon.com

Published by Infineon Technologies AG