SINOPEX ELECTRONICS CO. LTD.
尚 栢 電 子 有 限 公 司
Tel:852 - 2348 8233 Fax: 852 - 2348 8030 E-mail: sales@sinopex-ent.com

CR6224

Current Mode PWM Power Switch

Feature

- Power on Soft Start Reducing MOSFET Vds Stress
- Frequency shuffling for EMI
- Burst Mode Control For Improved Efficiency and Minimum Standby power Design
- Audio Noise Free Operation
- Fixed 50 KHz Switching Frequency
- Internal Synchronized Slope Compensation
- Low VDD Startup Current and Low Operating Current
- Leading Edge Blanking on Current Sense Input
- Compatible with OB2353/OB2354
- Pb-Free SOP-8L& DIP-8L
- Good Protection Coverage With Auto Self-Recovery
  - VDD Over Voltage Clamp and Under Voltage Lockout with Hysteresis (UVLO)
  - Line Input Compensated Cycle-by-Cycle Over-current Threshold Setting For Constant Output Power Limiting Over Universal Input Voltage Range
  - Overload Protection (OLP)
  - Over Voltage Protection (OVP)

Applications

- Battery Charger
- Digital Cameras and camcorder Adaptor
- VCR, SVR, STB, DVD & DVCD Player SMPS
- Set-Top Box (STB) Power
- Auxiliary Power Supply for PC and Server
- Open-frame SMPS

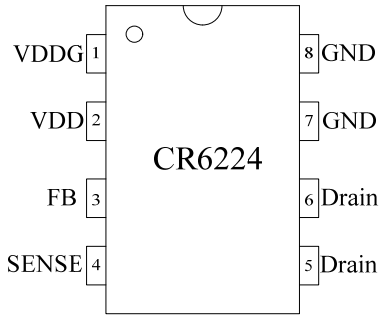
General Description

CR6224 combines a dedicated current mode PWM controller with a high voltage power MOSFET. It is optimized for high performance, low standby power, and cost effective off-line flyback converter applications in sub 20W range.

CR6224 offers complete protection coverage with automatic self-recovery feature including Cycle-by-Cycle current limiting (OCP), over load protection (OLP), VDD over voltage clamp and under voltage lockout (UVLO). Excellent EMI performance is achieved with frequency shuffling technique together with soft switching control at he totem pole gate drive output.

The tone energy at below 20 KHz is minimized in the design and audio noise is eliminated during operation. CR6224 is offered in DIP-8L & SOP-8L package.

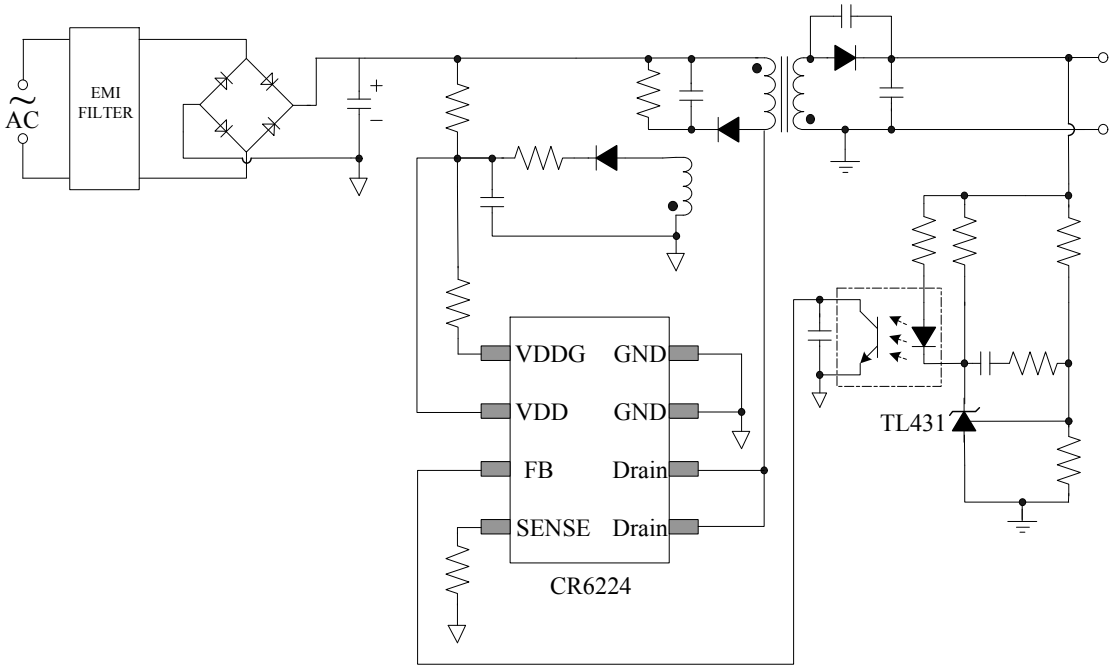
Pin Assignment （DIP-8L & SOP-8L）



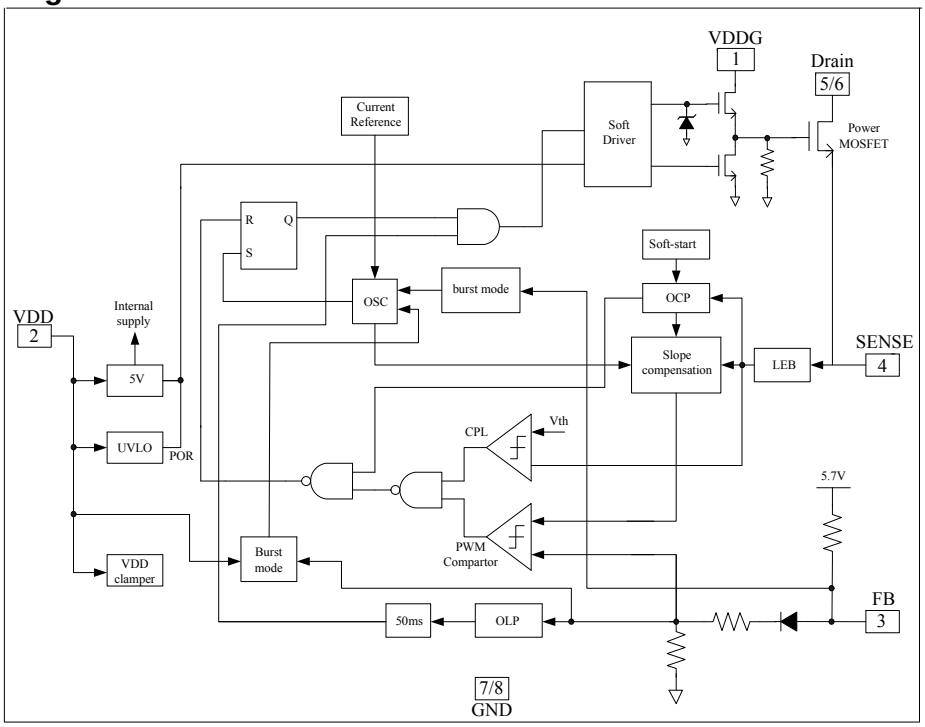
Pin Descriptions

Pin Name	I/O	Description
GND	P	Ground
FB	I	Feedback input pin. The PWM duty cycle is determined by voltage level into this pin and the current-sense signal at Pin 4.
VDD-G	P	Internal Gate Driver Power Supply
SENSE	I	Current sense input
VDD	P	IC DC power supply Input
Drain	O	HV MOSFET Drain Pin. The Drain pin is connected to the primary lead of the transformer.

TYPICAL APPLICATION



Block Diagram



Simplified Internal Circuit Architecture

Absolute Maximum Ratings

Parameter	Value
Drain Voltage (off state)	-0.3V to 650V
VDD Voltage	-0.3V to 30V
VDD-G Input Voltage	-0.3V to 30V
VDD Clamp Continuous Current	10 mA
FB Input Voltage	-0.3V to 7V
Sense Input Voltage	-0.3V to 7V
Min/Max Operating junction Temperature T_J	-20℃ to 150℃
Min/Max Storage Temperature T_{stg}	-55℃ to 160℃
Lead Temperature (Soldering, 10secs)	260℃

Note: Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. Exposure to absolute maximum-rated conditions for extended periods may affect device reliability.

Output Power Table

Package	230VAC ±15%	85-265VAC
	Open Frame[1]	Open Frame[1]
SOP-8L	12W	10W
DIP-8L	21W	16W

Notes:

1. Maximum practical continuous power in an open frame design with sufficient drain pattern as a heat sink, at 50℃ ambient.

Electrical Characteristics

(**Ta=25°C unless otherwise noted, V_{DD} = 16V**)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
Supply Voltage (VDD)						
$I_{startup}$	VDD Start up Current	VDD=14.5V, Measure Leakage current into VDD		5	20	uA
I_VDD (Operation)	Operation Current	V_{FB}=3V		1.6		mA
UVLO(ON)	VDD Under Voltage Lockout Enter		8.7	9.7	10.7	V
UVLO(OFF)	VDD Under Voltage Lockout Exit(Recovery)		14.6	15.8	17.0	V
OVP(ON)	Over voltage protection voltage	CS=0V, FB=3V Ramp up VDD until gate clock is off	27.0	28.5	30.0	V
VDD_Clamp	VDD Zener clamp Voltage	I_{DD}=10mA		30		V
Feedback Input Section(FB pin)						
V_{FB}_Open	V_{FB} Open Loop Voltage		5.4	5.7	6.0	V
I_{FB}_Short	FB pin short circuit current	Short FB pin to GND and measure current		1.45		mA
V_{TH}_0D	Zero Duty Cycle FB Threshold Voltage			0.8		V
V_{TH}_PL	Power Limiting FB Threshold Voltage			3.7		V
T_D_PL	Power Limiting Debounce Time			50		mS
Z_{FB}_IN	Input Impedance			4		KΩ
Current Sense Input(Sense Pin)						
Soft start time				4		ms
T_blanking	Leading edge blanking time			270		ns
Z_{SENSE}_IN	Input Impedance			40		KΩ
T_D_OC	Over Current Detection and Control Delay	From Over Current Occurs till the Gate drive output start to turn off		120		nS

V_{TH}_OC	Internal Current Limiting Threshold Voltage	FB=3.3V	0.72	0.77	0.82	V
Oscillator						
Fosc	Normal Oscillation Frequency		45	50	55	KHz
△f_Temp	Frequency Temperature Stability			5		%
△f_VDD	Frequency Voltage Stability			5		%
D_max	Maximum duty cycle	FB=3.3V, CS=0V	70	80	90	%
F_Burst	Burst Mode Base Frequency			22		KHz
Power MOSFET Section						
BV_{dss}	MOSFET Drain Source Breakdown Voltage	V_{GS}=0V, I_{DS}=250uA	600	650		V
RDS(on)	Static Drain to Source On Resistance	V_{GS}=10V, I_{DS}=1A	4.5	5.0	11	Ω
Frequency						
△f_VDD	Frequency Modulation range /Base frequency		-4		4	%

OPERATION DESCRIPTION

The CR6224 is a low power off-line SMPS Switcher optimized for off-line flyback converter applications in sub 20W power range. The burst mode control greatly reduces the standby power consumption and helps the design easily to meet the international power conservation requirements.

Startup Current and Start up Control

Startup current of CR6224 is designed to be very low so that VDD could be charged up above UVLO threshold level and device starts up quickly. A large value startup resistor can therefore be used to minimize the power loss yet achieve a reliable startup in application. For AC/DC adaptor with universal input range design, a 2 MΩ, 1/8 W startup resistor could be used together with a VDD capacitor to provide a fast startup and yet low power dissipation design solution.

Operation current

The Operation current of CR6224 is low at 2 mA. Good efficient is achieved with CR6224 low operating current together with the 'Extended burst mode' control features.

Soft Start

CR6224 features an internal 4 ms soft start to soften the electrical stress occurring in the power supply during startup. It is activated during the power on sequence. As soon as VDD reaches UVLO(OFF), the peak current is gradually increased from nearly zero to the maximum level of 0.77V. Every restart up is followed by a soft start.

Frequency shuffling for EMI improvement

The frequency shuffling (switching frequency modulation) is implemented in CR6224. The oscillation frequency is modulated so that the tone energy is spread out. The spread spectrum minimizes the conduction band EMI and therefore eases the system design.

Extended Burst Mode Operation

At light load or zero load condition, most of the power dissipation in a switching mode power supply is from switching loss on the mosfet, the core loss of the transformer and the loss on the snubber circuit. The magnitude of power loss is in proportion to the switching frequency. Lower switching frequency leads to the reduction on the power loss and thus conserves the energy.

The switching frequency is internally adjusted at no load or light load condition. The switch frequency reduces at light/no load condition to improve the conversion efficiency. At light load or no load condition, the FB input drops below burst mode threshold level and device enters Burst Mode control. The Gate drive output switches only when VDD voltage drops below a preset level and FB input is active to output an on state to minimize the switching loss and reduce the standby power consumption to the greatest extend.

The switching frequency control also eliminates the audio noise at any loading conditions.

Oscillator Operation

The switching frequency of CR6224 is internally fixed at 50 KHz. No external frequency setting components are required for PCB design simplification.

Current Sensing and Leading Edge Blanking

Cycle-by-Cycle current limiting is offered in CR6224 current mode PWM control. The switch current is detected by sense resistor into the sense pin. An internal leading edge blank circuit chops off the sensed voltage spike at initial internal power MOSFET on state due to snubber diode reverse recovery and surge gate current of internal power MOSFET so that the external RC filtering on

sense input is no longer needed. The current limiting comparator is disabled and cannot turn off the internal power MOSFET during the blanking period. The PWM duty cycle is determined by the current sense input voltage and the FB input voltage.

Internal synchronized Slope Compensation

Built-in slope compensation circuit adds voltage ramp onto the current sense input voltage for PWM generation. This greatly improves the close loop stability at CCM and prevents the sub-harmonic oscillation and thus reduces the output ripple voltage.

Drive

The internal power MOSFET in CR6224 is driven by a dedicated gate driver for power switch control. Too weak the gate drive strength results in higher conduction and switch loss of MOSFET while too strong gate drive results the compromise of EMI.

A good tradeoff is achieved through the built-in totem pole gate design with right output strength and dead time control. The low idle loss and good EMI system design is easier to achieve with this dedicated control scheme.

In addition to the gate drive control scheme mentioned, the gate drive strength can also be adjusted externally by a resistor connected between VDD and VDDG, the falling edge of the Drain output can be well controlled. It provides great flexibility for system EMI design.

Protection Controls

Good power supply system reliability is achieved with its rich protection features including Cycle-by-Cycle current limiting (OCP), Over load Protection (OLP) and over voltage clamp, Under Voltage Lockout on VDD (UVLO).

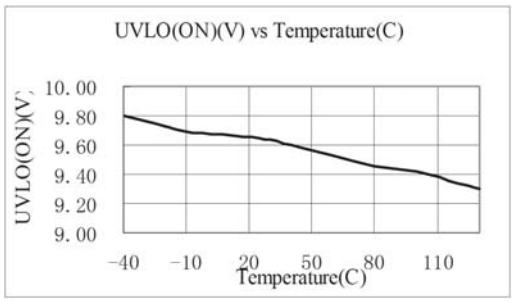
With On-Bright Proprietary technology, the OCP is line voltage compensated to achieve constant output power limit over the universal input voltage range.

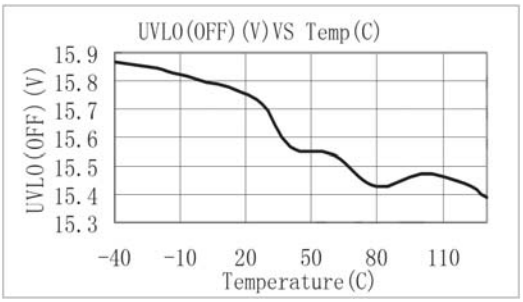
At overload condition when FB input voltage exceeds power limit threshold value for more than TD_PL, control circuit reacts to shut down the switcher .Switcher restarts when VDD voltage drops below UVLO limit.

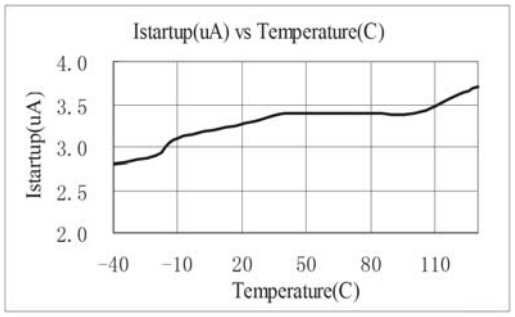
VDD is supplied by transformer auxiliary winding output. It is clamped when VDD is higher than 30V. The output of CR6224 is shut down when VDD drops below UVLO(ON) limit and Switcher enters power on start-up sequence thereafter.

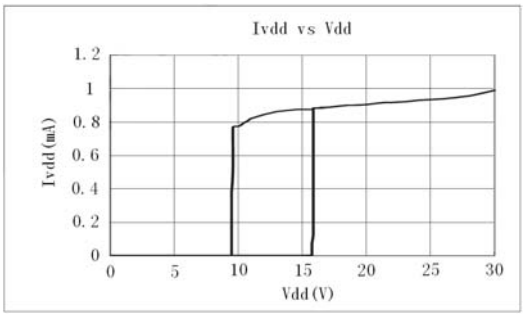
CHARACTERIZATION PLOTS

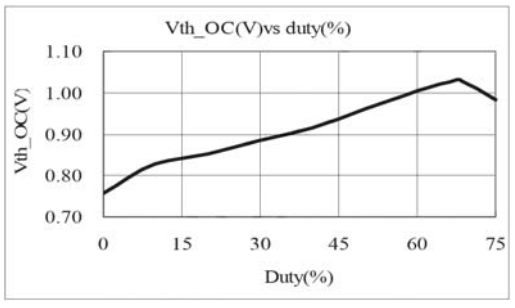
The characteristic graphs are normalized at T_A=25℃.

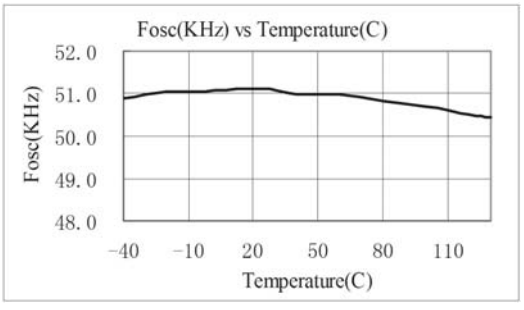






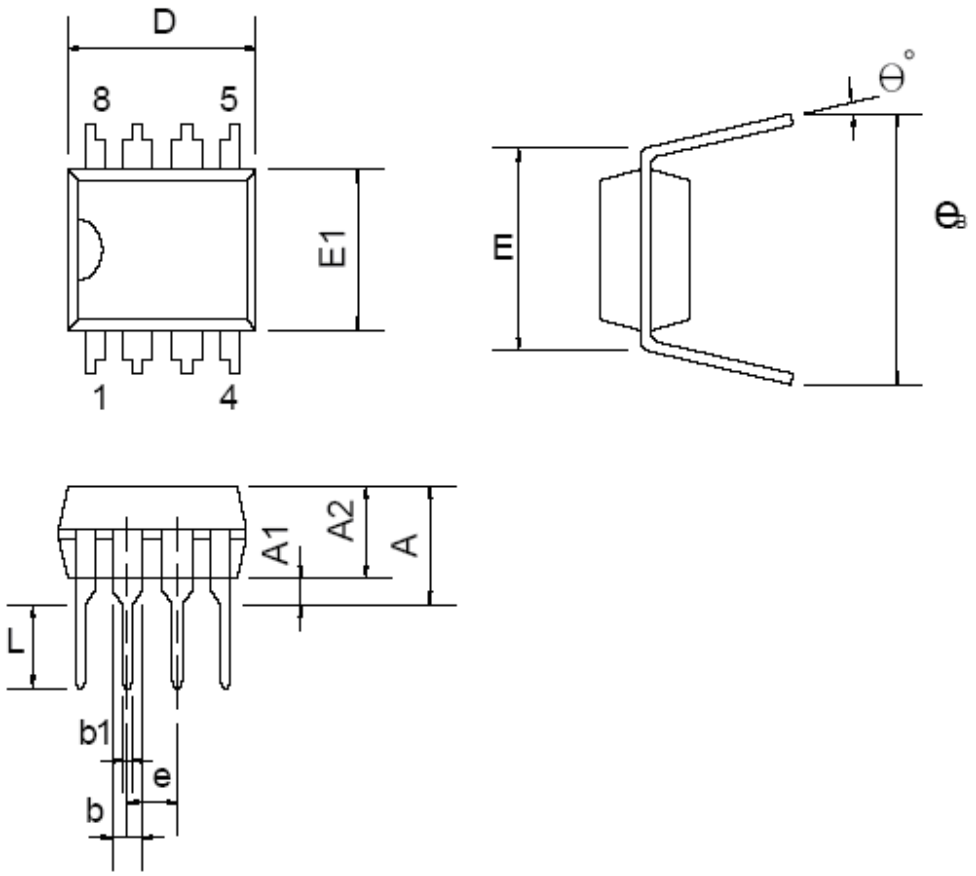






PACKAGE DEMENSIONS

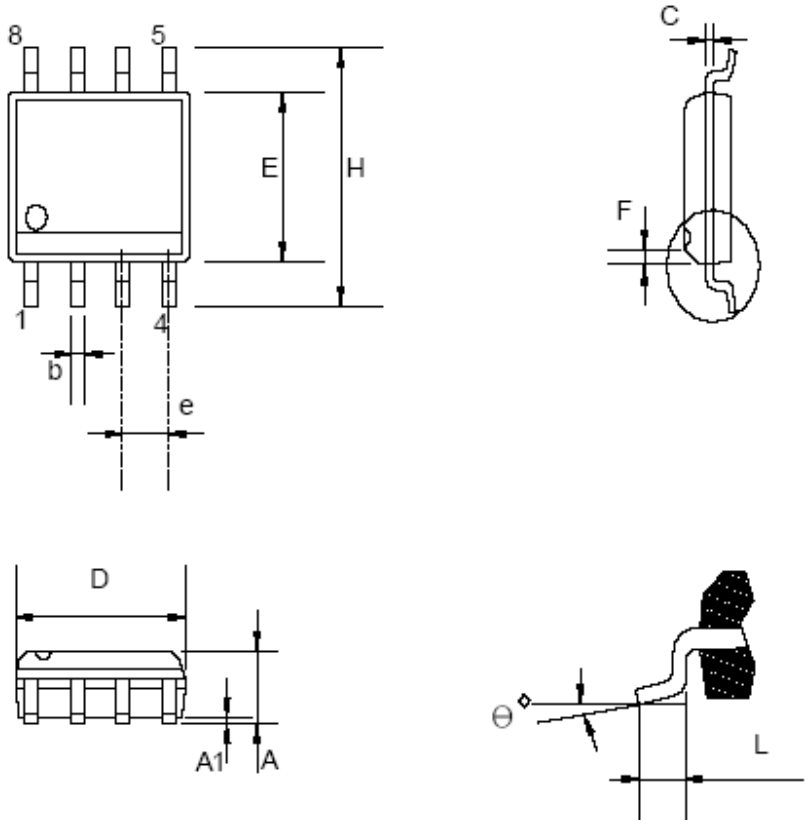
DIP-8L



Dimensions

Symbol	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			5.334			0.210
A1	0.381			0.015		
A2	3.175	3.302	3.429	0.125	0.130	0.135
b		1.524			0.060	
b1		0.457			0.018	
D	9.017	9.271	10.160	0.355	0.365	0.400
E		7.620			0.300	
E1	6.223	6.350	6.477	0.245	0.250	0.255
e		2.540			0.100	
L	2.921	3.302	3.810	0.115	0.130	0.150
eB	8.509	9.017	9.525	0.335	0.355	0.375
θ°	0°	7°	15°	0°	7°	15°

SOP-8L



Dimensions DISCLAIMERS

Symbol	Millimeter			Inch		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	1.346		1.752	0.053		0.069
A1	0.101		0.254	0.004		0.010
b		0.406			0.016	
c		0.203			0.008	
D	4.648		4.978	0.183		0.196
E	3.810		3.987	0.150		0.157
e	1.016	1.270	1.524	0.040	0.050	0.060
F		0.381X45°			0.015X45°	
H	5.791		6.197	0.228		0.244
L	0.406		1.270	0.016		0.050
θ°	0°		8°	0°		8°