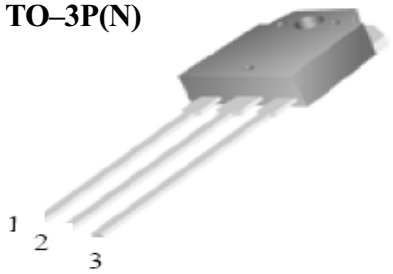
General Description：

FTW20N50A, the silicon N-channel Enhanced VDMOSFETs, is obtained by the self-aligned planar Technology which reduce the conduction loss, improve switching performance and enhance the avalanche energy. The transistor can be used in various power switching circuit for system miniaturization and higher efficiency. The package form is TO-3P(N), which accords with the RoHS standard..

V_{DSS}	500	V
I_D	20	A
P_D (T_C=25℃)	230	W
$R_{DS(ON)}$	0.26	Ω

TO–3P(N)

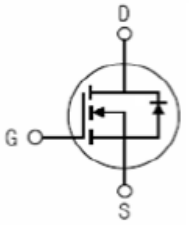


1.Gate 2.Drain 3.Source

Features：

- **Fast Switching**
- **Low ON Resistance(Rdson≤0. 3 Ω)**
- **Low Gate Charge (Typical Data:130nC)**
- **Low Reverse transfer capacitances(Typical:65pF)**
- **100% Single Pulse avalanche energy Test**

Inner Equivalent Principium Chart



Applications：

Power switch circuit of electron ballast and adaptor.

Absolute（Tc= 25℃ unless otherwise specified）：

Symbol	Parameter	Rating	Units
V_{DSS}	Drain-to-Source Voltage	500	V
I_D	Continuous Drain Current	20	A
	Continuous Drain Current T_C = 100 °C	12	A
I_{DM} [a1]	Pulsed Drain Current	80	A
V_{GS}	Gate-to-Source Voltage	±30	V
E_{AS} [a2]	Single Pulse Avalanche Energy	950	mJ
E_{AR} [a1]	Avalanche Energy ,Repetitive	90	mJ
I_{AR} [a1]	Avalanche Current	14	A
dv/dt [a3]	Peak Diode Recovery dv/dt	4.0	V/ns
P_D	Power Dissipation	230	W
	Derating Factor above 25°C	1.85	W/℃
T_J， T_{stg}	Operating Junction and Storage Temperature Range	150，–55 to 150	℃
T_L	MaximumTemperature for Soldering	300	℃

Electrical Characteristics（Tc= 25℃ unless otherwise specified）：

OFF Characteristics						
Symbol	Parameter	Test Conditions	Rating			Units
			Min.	Typ.	Max.	
V_{DSS}	Drain to Source Breakdown Voltage	V_{GS}=0V, I_D=250μA	500	--	--	V
$\Delta BV_{DSS}/\Delta T_J$	Bvdss Temperature Coefficient	ID=250uA,Reference25℃	--	0.55	--	V/℃
I_{DSS}	Drain to Source Leakage Current	V_{DS} = 500V, V_{GS}= 0V, T_a = 25℃	--	--	10	μA
		V_{DS} =400V, V_{GS}= 0V, T_a = 125℃			100	
$I_{GSS(F)}$	Gate to Source Forward Leakage	V_{DS} =0V, V_{GS}= 30V	--	--	100	nA
$I_{GSS(R)}$	Gate to Source Reverse Leakage	V_{DS} =0V, V_{GS}= -30V	--	--	-100	nA

ON Characteristics						
Symbol	Parameter	Test Conditions	Rating			Units
			Min.	Typ.	Max.	
$R_{DS(ON)}$	Drain-to-Source On-Resistance	V_{GS}=10V,I_D=10A	--	0.26	0.3	Ω
$V_{GS(TH)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 250μA	2.0	--	4.0	V
Pulse width tp≤380μs, δ ≤2%						

Dynamic Characteristics						
Symbol	Parameter	Test Conditions	Rating			Units
			Min.	Typ.	Max.	
g_{fs}	Forward Transconductance	V_{DS}=15V, I_D =10A	13	17	--	S
C_{iss}	Input Capacitance	V_{GS} = 0V V_{DS} = 25V f = 1.0MHz	--	4500	6000	pF
C_{oss}	Output Capacitance		--	350	460	
C_{rss}	Reverse Transfer Capacitance		--	65	80	

Resistive Switching Characteristics						
Symbol	Parameter	Test Conditions	Rating			Units
			Min.	Typ.	Max.	
$t_{d(ON)}$	Turn-on Delay Time	I_D =20A V_{DD} = 250V R_G = 25Ω	--	55	120	ns
tr	Rise Time		--	145	310	
$t_{d(OFF)}$	Turn-Off Delay Time		--	280	770	
t_f	Fall Time		--	135	370	
Q_g	Total Gate Charge	I_D =20A V_{DD} =400V V_{GS} = 10V	--	130	170	nC
Q_{gs}	Gate to Source Charge		--	20		
Q_{gd}	Gate to Drain (“Miller”)Charge		--	45		

Source-Drain Diode Characteristics						
Symbol	Parameter	Test Conditions	Rating			Units
			Min.	Typ.	Max.	
I_S	Continuous Source Current (Body Diode)		--	--	20	A
I_{SM}	Maximum Pulsed Current (Body Diode)		--	--	80	A
V_{SD}	Diode Forward Voltage	I_S=20A,V_{GS}=0V	--	--	1.5	V
trr	Reverse Recovery Time	I_S=20A,T_j = 25° C	--	480	--	ns
Qrr	Reverse Recovery Charge	dI_F/dt=100A/us, V_{GS}=0V	--	7.7	--	nC
Pulse width tp≤380μs, δ ≤2%						

Symbol	Parameter	Max.	Units
$R_{\theta JC}$	Junction-to-Case	0.54	℃/W
$R_{\theta JA}$	Junction-to-Ambient	40	℃/W

[a1]: Repetitive rating; pulse width limited by maximum junction temperature
[a2]: L=10.0mH, I_D=20A, Start T_J=25℃
[a3]: I_{SD} =20A,di/dt ≤300A/us,V_{DD}≤$BV_{DS,}$ Start T_J=25℃

Characteristics Curve:

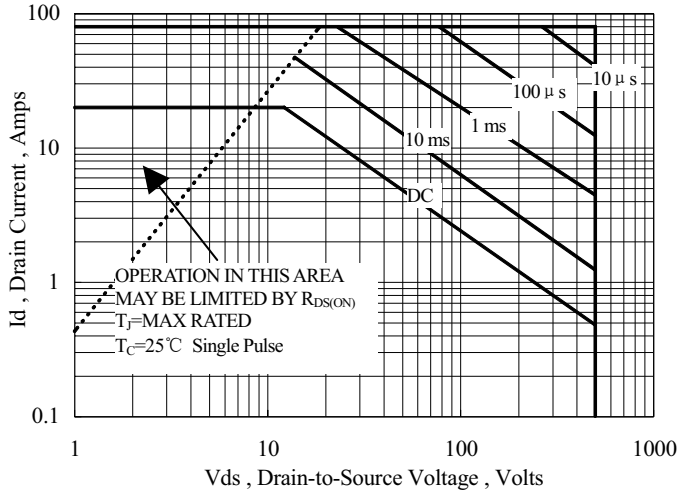


Figure 1 Maximun Forward Bias Safe Operating Area

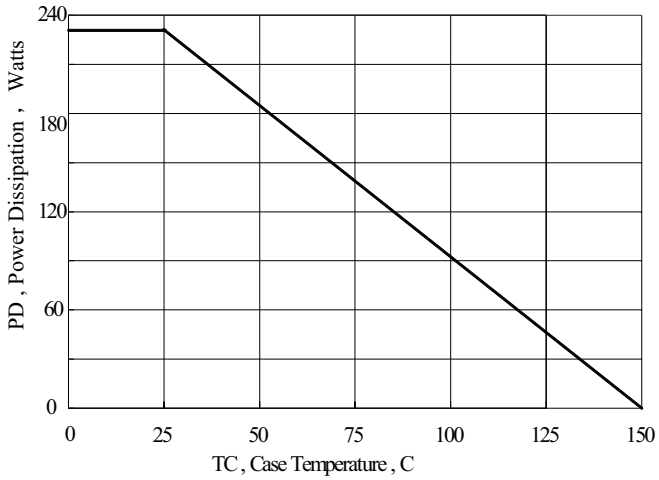


Figure 2 Maximun Power Dissipation vs Case Temperature

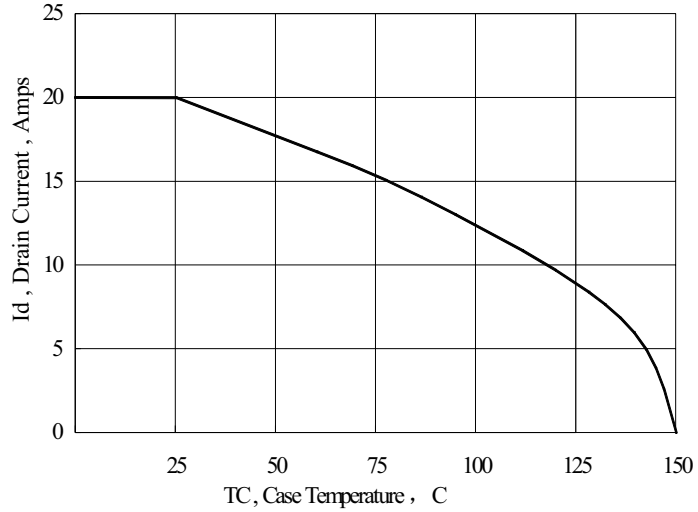


Figure 3 Maximum Continuous Drain Current vs Case Temperature

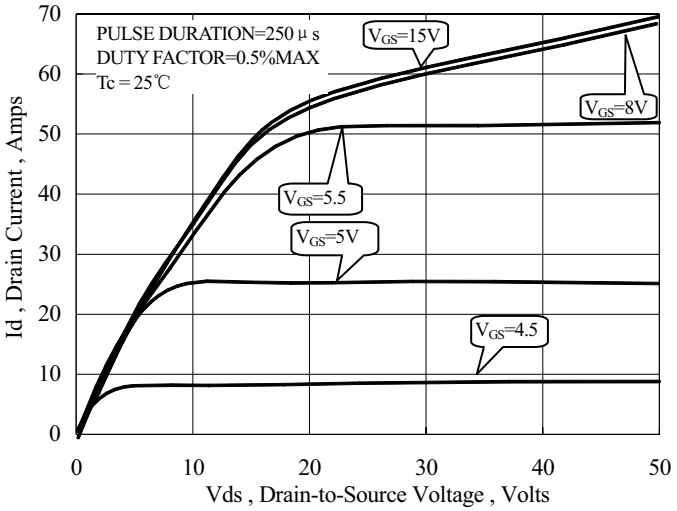


Figure 4 Typical Output Characteristics

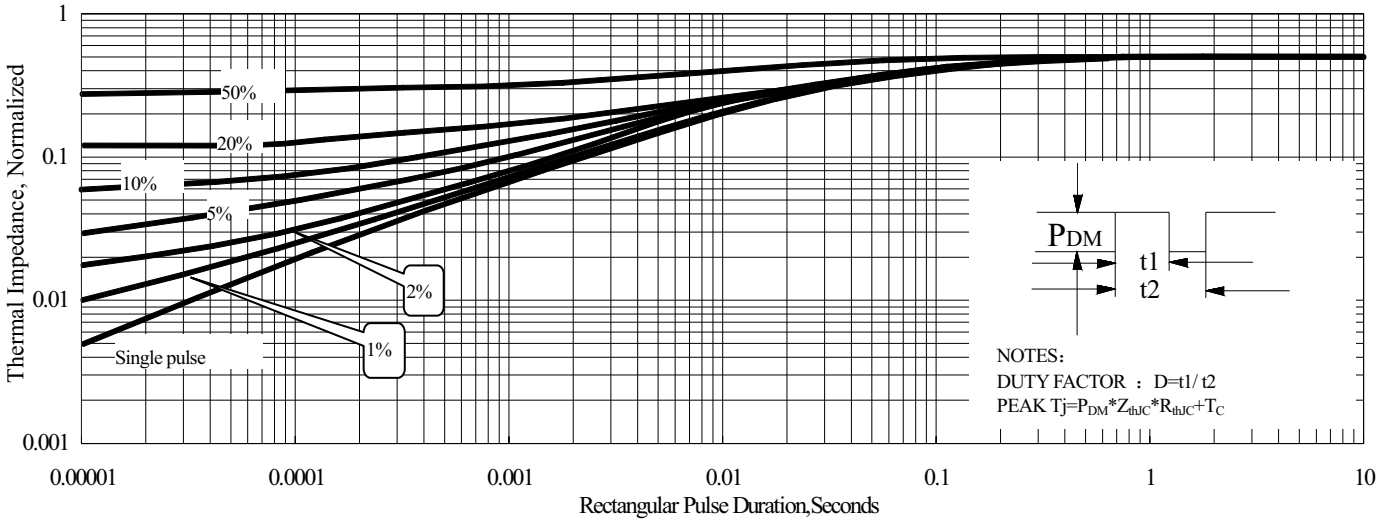


Figure 5 Maximum Effective Thermal Impendance , Junction to Case

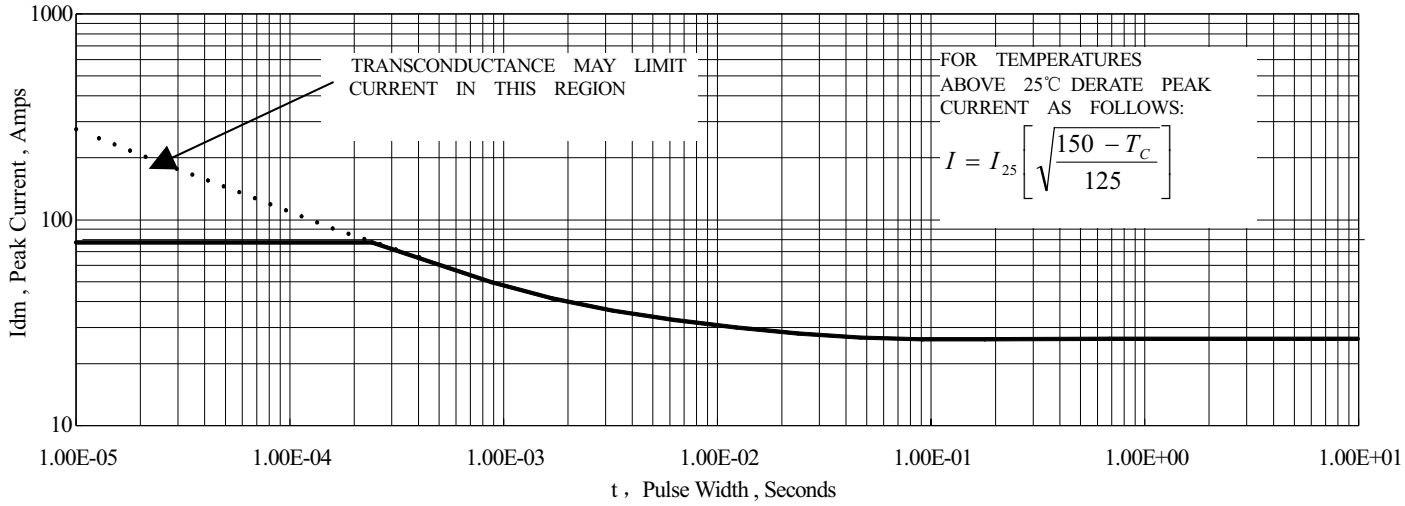


Figure 6 Maximun Peak Current Capability

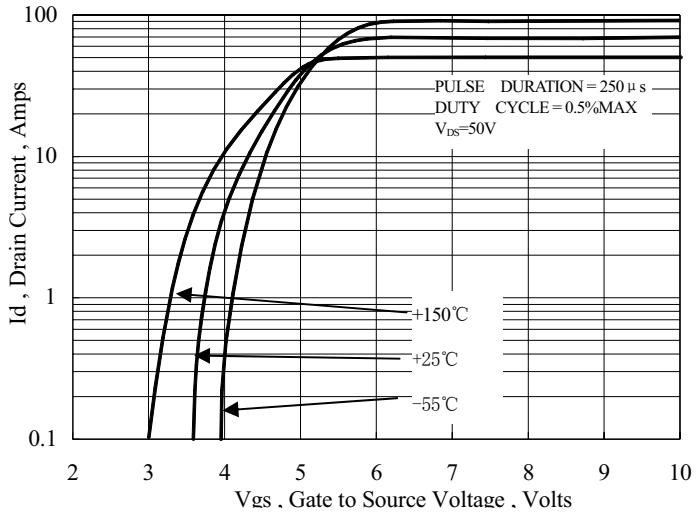


Figure 7 Typical Transfer Characteristics

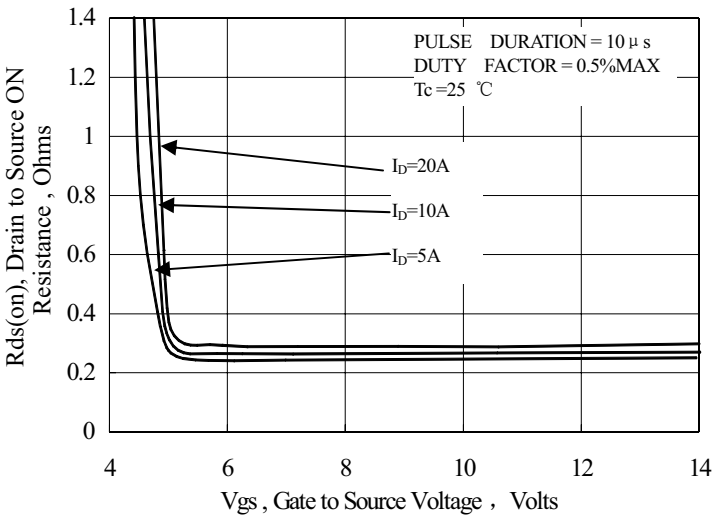


Figure 8 Typical Drain to Source ON Resistance vs Gate Voltage and Drain Current

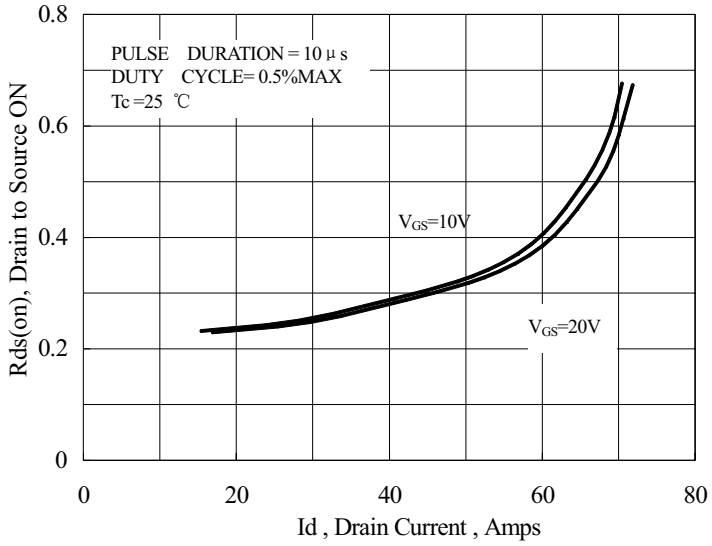


Figure 9 Typical Drain to Source ON Resistance vs Drain Current

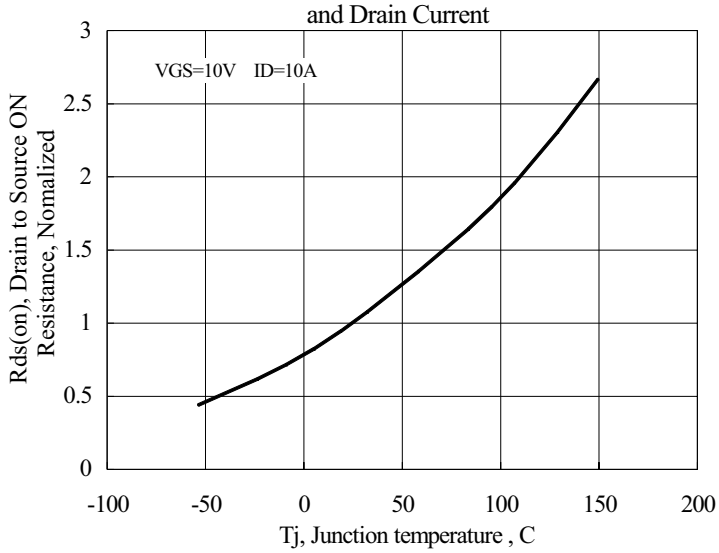


Figure 10 Typical Drian to Source on Resistance vs Junction Temperature

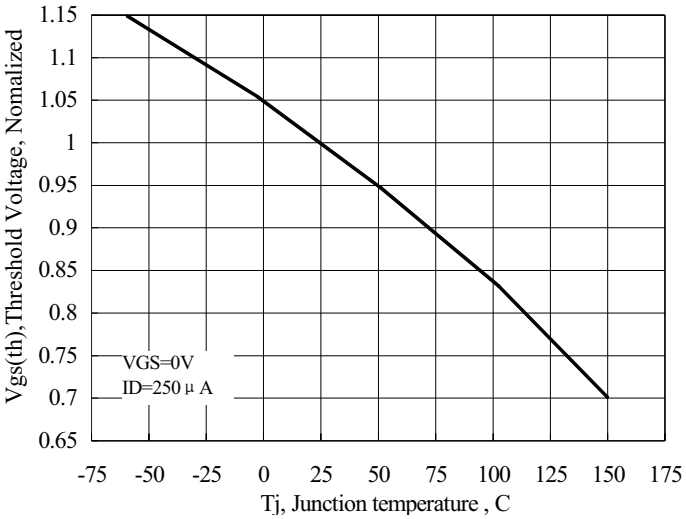


Figure 11 Typical Theshold Voltage vs Junction Temperature

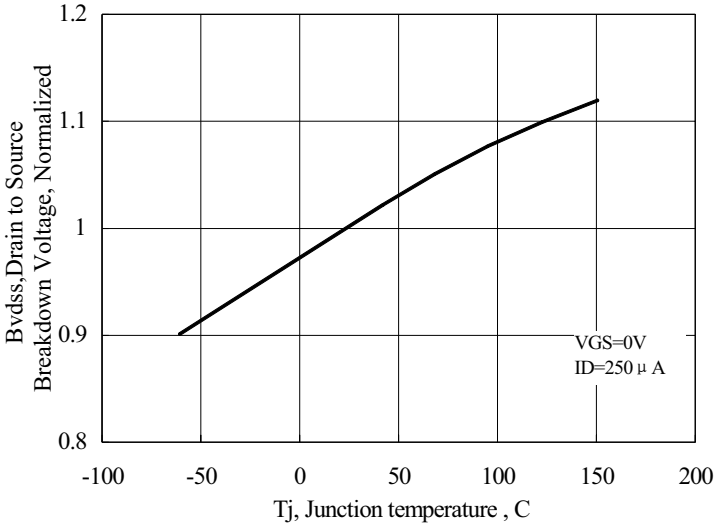


Figure 12 Typical Breakdown Voltage vs Junction Temperature

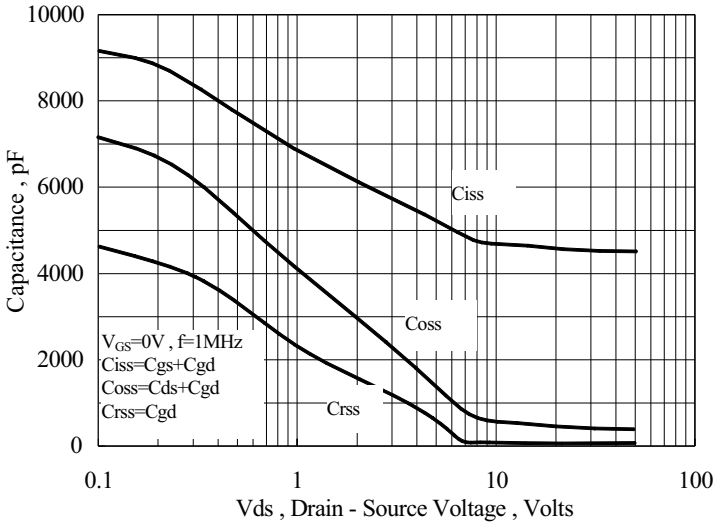


Figure 13 Typical Capacitance vs Drain to Source Voltage

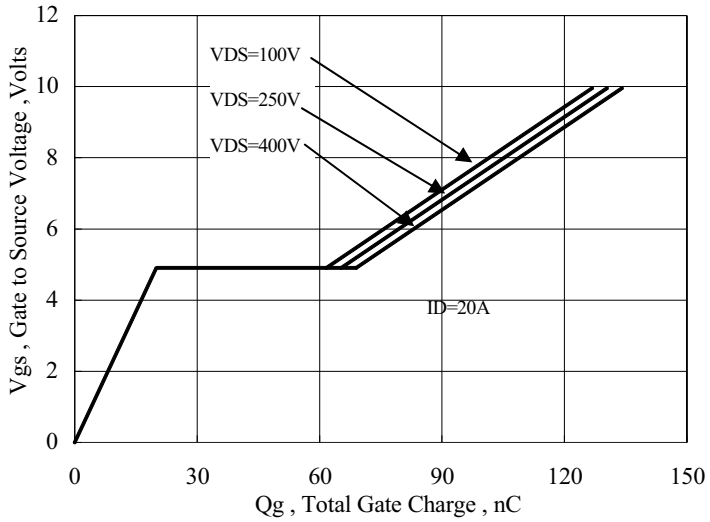


Figure 14 Typical Gate Charge vs Gate to Source Voltage

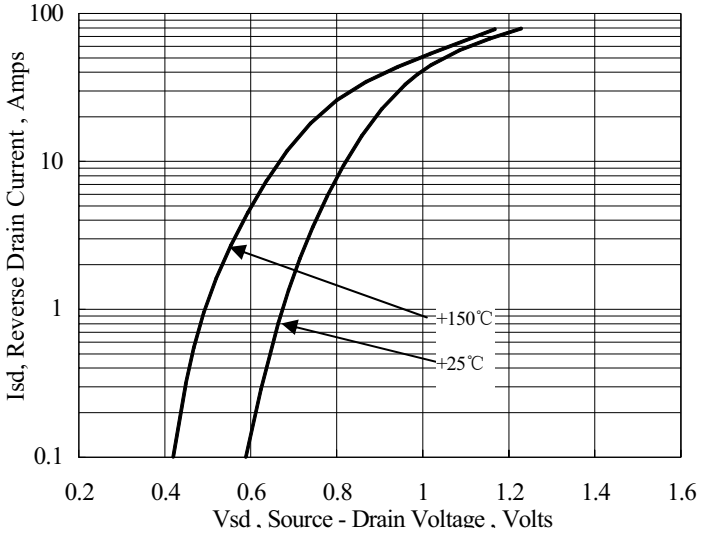


Figure 15 Typical Body Diode Transfer Characteristics

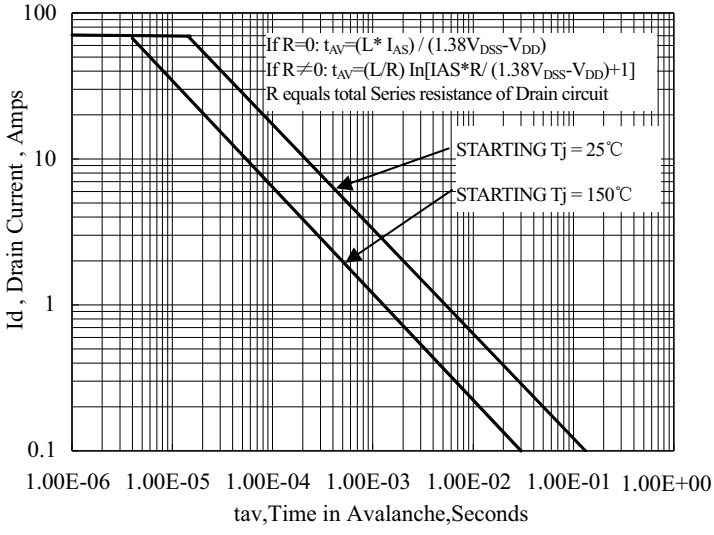
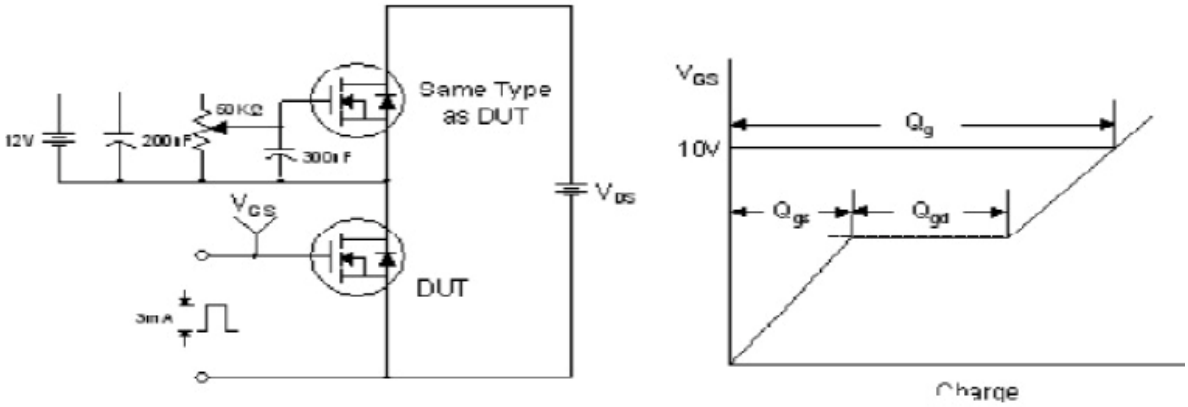
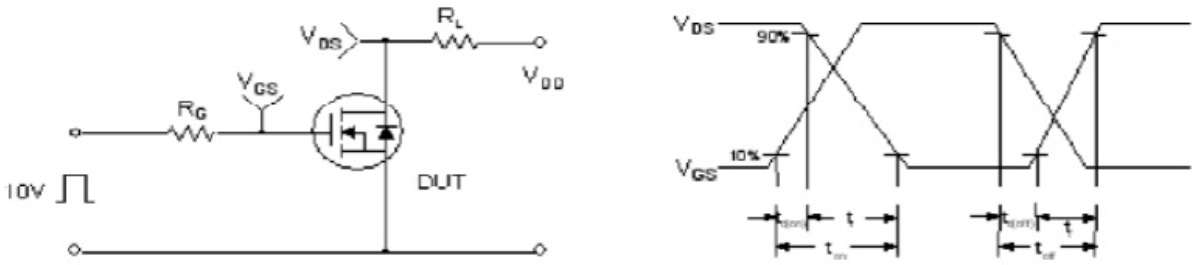


Figure 16 Unclamped Inductive Switching Capability

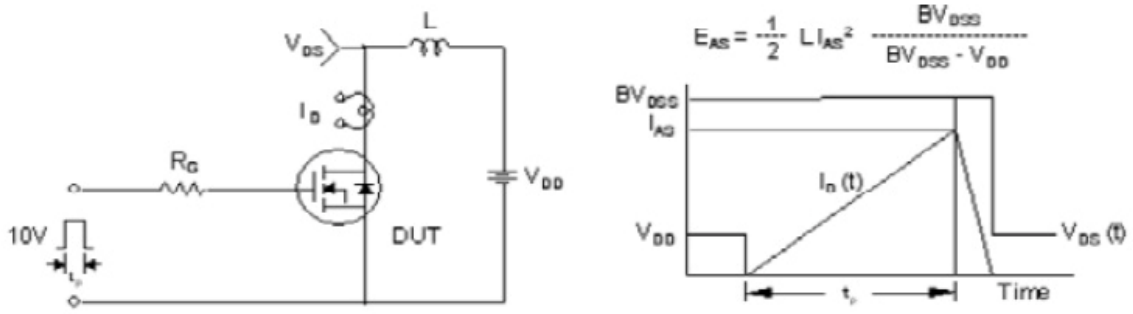
TestCircuitandWaveform



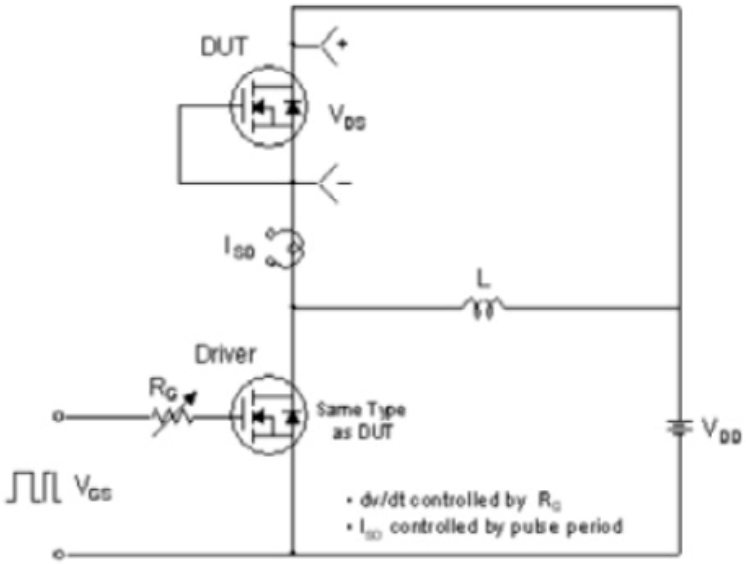
Gate Charge Test Circuit and Waveform

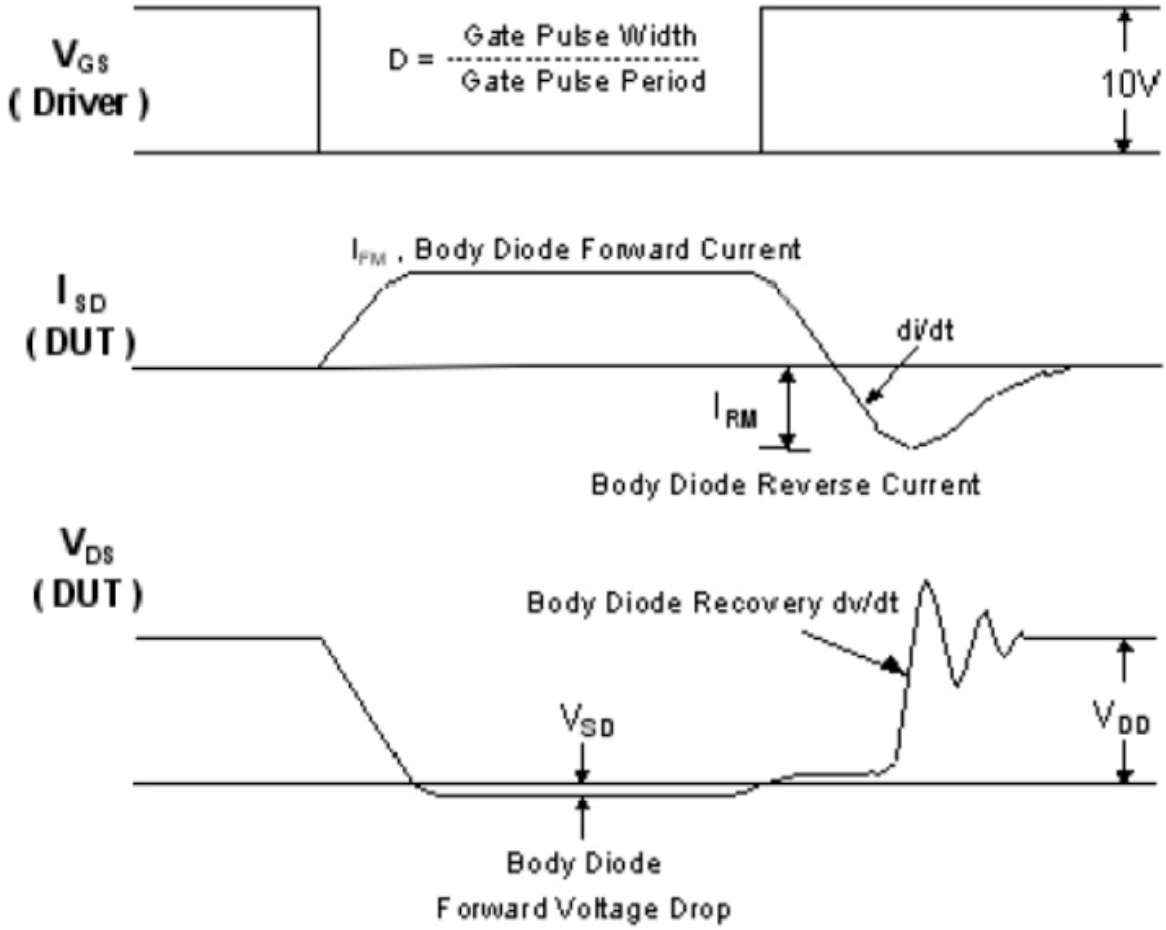


Resistive Switching Test Circuit and Waveform



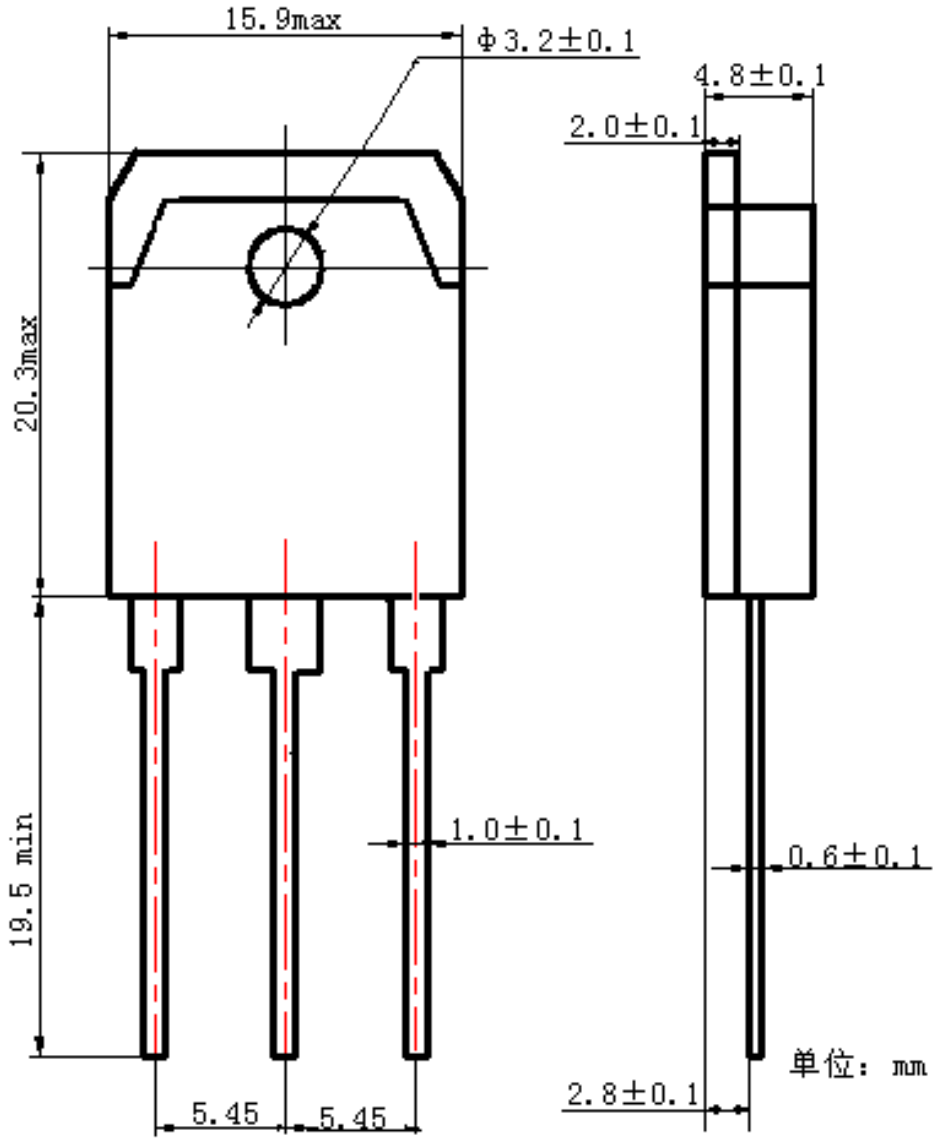
Unclamped Inductive Switching Test Circuit and Waveform





Diode Reverse Recovery Test Circuit and Waveform

Package Information：



TO-3P(N) Package

The name and content of poisonous and harmful material in products

Part's Name	Hazardous Substance					
	Pb	Hg	Cd	Cr(VI)	PBB	PBDE
Limit	≤0.1%	≤0.1%	≤0.01%	≤0.1%	≤0.1%	≤0.1%
Lead Frame	○	○	○	○	○	○
Molding Compound	○	○	○	○	○	○
Chip	○	○	○	○	○	○
Wire Bonding	○	○	○	○	○	○
Solder	○	○	○	○	○	○
Note	○： means the hazardous material is under the criterion of SJ/T11363-2006. ×： means the hazardous material exceeds the criterion of SJ/T11363-2006.					

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