iW3610

AC/DC Digital Power Controller for Dimmable LED Drivers

iWatt

1.0 Features

- Isolated AC/DC offline 100 V_{ac} / 230 V_{ac}
- Line frequency ranges from 47 Hz to 64 Hz
- Intelligent wall dimmer detection
  - » Leading-edge
  - » Trailing-edge
  - » No-dimmer detected
  - » Unsupported dimmer
- Hybrid dimming scheme
- Wide dimming range from 2% up to 100%
- No visible flicker
- Resonant control to achieve high efficiency, 85% without dimmer
- Meets Harmonic Requirement, high power factor (0.9) without dimmer
- Temperature control to adjust LED brightness
- Small size design
  - » small size input bulk capacitor
  - » small size output capacitor
  - » smallest transformer
- Primary-side sensing eliminates the need for opto-isolator feedback and simplifies design
- Tight LED current regulation ± 5%
- Fast start-up, typically 10 µA start-up current
- Up to 45 W
- Precise LED current control
- Multiple protection features:
  - » LED open protection
  - » Single-fault protection
  - » Over-current protection
  - » LED short circuit protection
  - » Current sense resistor short protection
  - » Over-temperature protection

2.0 Description

The iW3610 is a high performance AC/DC offline power supply controller for dimmable LED luminaires, which uses advanced digital control technology to detect the dimmer type and phase. The dimmer conduction phase controls the LED brightness. The LED brightness is modulated by PWM-dimming. The dimming frequency is selectable via product options. iW3610's unique digital control technology eliminates visible flicker.

iW3610 can operate with all dimmer schemes including: leading-edge dimmer, trailing-edge dimmer, as well as other dimmer configurations such as R-type, R-C type or R-L type. When a dimmer is not present, the controller can automatically detect that there is no dimmer.

iW3610 operates in quasi-resonant mode to provide high efficiency. Also the iW3610 provides a number of key built-in features. Since the iW3610 uses iWatt's advanced primary-side sensing technology, it achieves excellent line and load regulation without secondary feedback circuitry. In addition, iW3610's pulse-by-pulse waveform analysis allows for accurate LED current regulation. The iW3610 also maintains stability over all operating conditions without the need for loop compensation components. Therefore, the iW3610 minimizes external component count, simplifies EMI design and lowers overall bill of materials cost.

3.0 Applications

- Dimmable LED luminaries

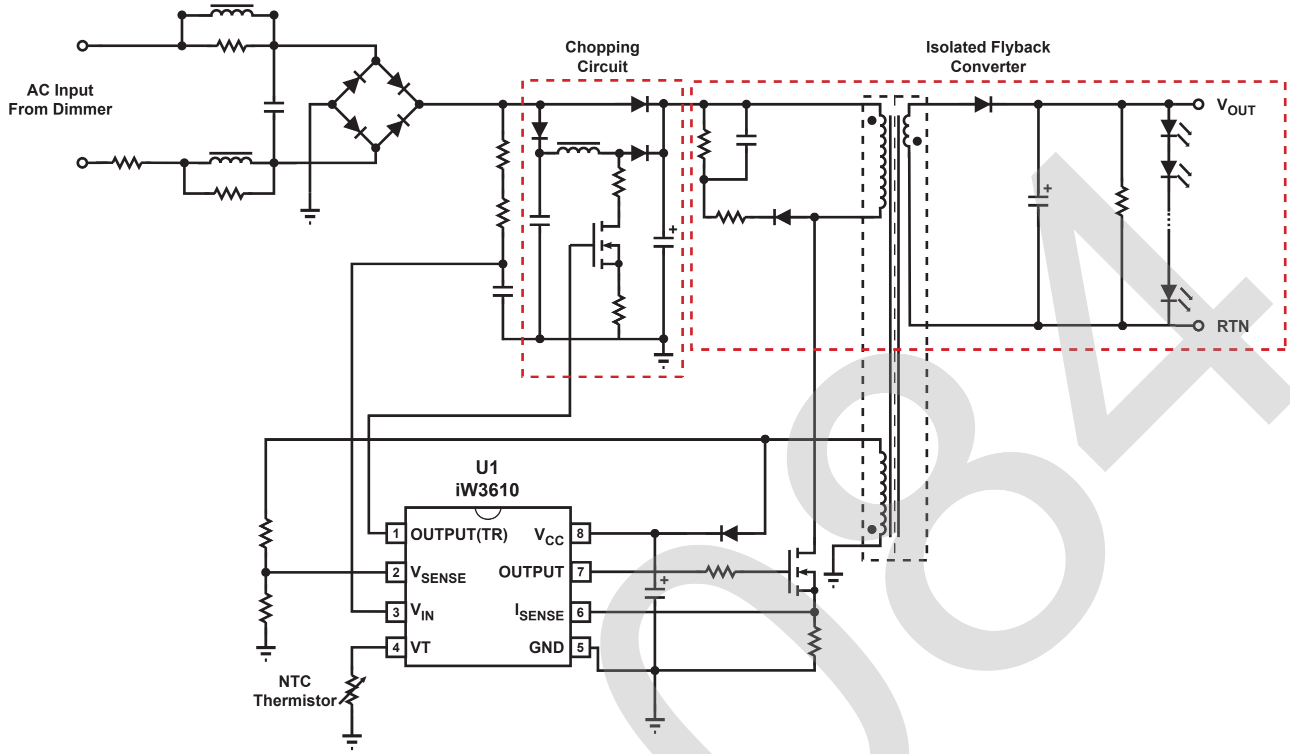
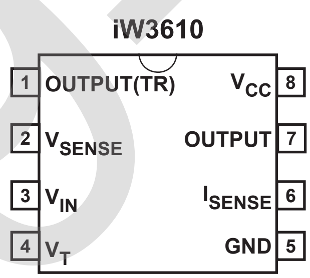


Figure 3.1 : Typical Application Circuit

4.0 Pinout Description



Pin #	Name	Type	Pin Description
1	OUTPUT(TR)	Output	Gate drive for chopping MOSFET switch
2	V_{SENSE}	Analog Input	Auxiliary voltage sense (used for primary side regulation and ZVS)
3	V_{IN}	Analog Input	Rectified AC line average voltage sense
4	V_{T}	Analog Input	External shutdown control
5	GND	Ground	Ground
6	I_{SENSE}	Analog Input	Primary current sense (used for cycle-by-cycle peak current control and limit)
7	OUTPUT	Output	Gate drive for external main MOSFET switch
8	V_{CC}	Power Input	Power supply for control logic and voltage sense for power-on reset circuitry

5.0 Absolute Maximum Ratings

Absolute maximum ratings are the parameter values or ranges which can cause permanent damage if exceeded. For maximum safe operating conditions, refer to Electrical Characteristics in Section 6.0.

Parameter	Symbol	Value	Units
DC supply voltage range (pin 8, I_{CC} = 20mA max)	V_{CC}	-0.3 to 18	V
DC supply current at V_{CC} pin	I_{CC}	20	mA
Output (pin 7)		-0.3 to 18	V
Output(TR) (pin 1)		-0.3 to 18	V
V_{SENSE} input (pin 2, I_{Vsense} ≤ 10 mA)		-0.7 to 4.0	V
V_{IN} input (pin 3)		-0.3 to 18	V
I_{SENSE} input (pin 6)		-0.3 to 4.0	V
V_T input (pin 4)		-0.3 to 4.0	V
Power dissipation at T_A ≤ 25°C	P_D	526	mW
Maximum junction temperature	$T_{J\ MAX}$	125	°C
Storage temperature	T_{STG}	–65 to 150	°C
Lead temperature during IR reflow for ≤ 15 seconds	T_{LEAD}	260	°C
Thermal Resistance Junction-to-PCB Board Surface Temperature	Ψ_{JB} (Note 1)	70	°C/W
ESD rating per JEDEC JESD22-A114		2,000	V
Latch-Up test per JEDEC 78		±100	mA

Notes:

Note 1. Ψ_{JB} [Psi Junction to Board] provides an estimation of the die junction temperature relative to the PCB [**B**oard] surface temperature. This data is measured at the ground pin (pin 5) without using any thermal adhesives. See Section 9.12 for more information.

6.0 Electrical Characteristics

V_{CC} = 12 V, -40°C ≤ T_A ≤ 85°C, unless otherwise specified (Note 1)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
V_{IN} SECTION (Pin 3)						
Start-up current	I_{INST}	V_{IN} = 10 V, C_{VCC} = 10 µF		10	15	µA
Input impedance	Z_{IN}	After start-up		2.5		kΩ
V_{IN} Range	V_{IN}		0		1.8	V
V_{SENSE} SECTION (Pin 2)						
Input leakage current	I_{BVS}	V_{SENSE} = 2 V			1	µA
Nominal voltage threshold	$V_{SENSE(NOM)}$	T_A=25°C, negative edge	1.523	1.538	1.553	V
Output OVP threshold	$V_{SENSE(MAX)}$	T_A=25°C, negative edge	1.683	1.7	1.717	V
OUTPUT SECTION (Pin 7)						
Output low level ON-resistance	$R_{DS(ON)LO}$	I_{SINK} = 5 mA		30		Ω
Output high level ON-resistance	$R_{DS(ON)HI}$	I_{SOURCE} = 5 mA		60		Ω
Rise time (Note 2)	t_R	T_A = 25°C, C_L = 330 pF 10% to 90%		50		ns
Fall time (Note 2)	t_F	T_A = 25°C, C_L = 330 pF 90% to 10%		30		ns
Maximum switching frequency (Note 3)	$f_{SW(MAX)}$			200		kHz
V_{CC} SECTION (Pin 8)						
Maximum operating voltage	$V_{CC(MAX)}$				16	V
Start-up threshold	$V_{CC(ST)}$	V_{CC} rising	11	12	13	V
Undervoltage lockout threshold	$V_{CC(UVL)}$	V_{CC} falling	7	7.5	8	V
Operating current	I_{CCQ}	C_L = 330 pF, V_{SENSE} = 1.5 V		3.9	4.5	mA
Zener diode clamp voltage	$V_{Z(CLAMP)}$			19		V

6.0 Electrical Characteristics (cont.)

V_{CC} = 12 V, -40°C ≤ T_A ≤ 85°C, unless otherwise specified (Note 1)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
I_{SENSE} SECTION (Pin 6)						
Over current limit threshold	V_{OCP}		1.83	1.89	1.95	V
Isense short protection reference	V_{RSNS}			0.16		V
CC regulation threshold limit (Note 2)	$V_{REG\text{-}TH}$			1.8		V
V_T SECTION (Pin 4)						
Shutdown threshold (Note 2)	$V_{SH\text{-}TH}$			0.09		V
Input leakage current	I_{BVS}	V_{SD} = 1.0 V			1	μA
Pull up current source	I_{SD}		90	100	110	μA
OUTPUT(TR) SECTION (Pin 1)						
Output low level ON-resistance	$R_{DS\text{-}TR(ON)LO}$	I_{SINK} = 5 mA		100		Ω
Output high level ON-resistance	$R_{DS\text{-}TR(ON)HI}$	I_{SOURCE} = 5 mA		200		Ω

Notes:

Note 1. Adjust V_{CC} above the start-up threshold before setting at 12 V.

Note 2. These parameters are not 100% tested, guaranteed by design and characterization.

Note 3. Operating frequency varies based on the line and load conditions, see Theory of Operation for more details.

7.0 Typical Performance Characteristics

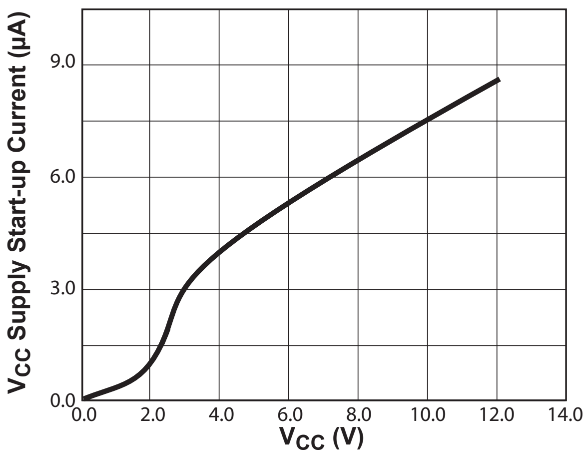


Figure 7.1 : V_{CC} vs. V_{CC} Supply Start-up Current

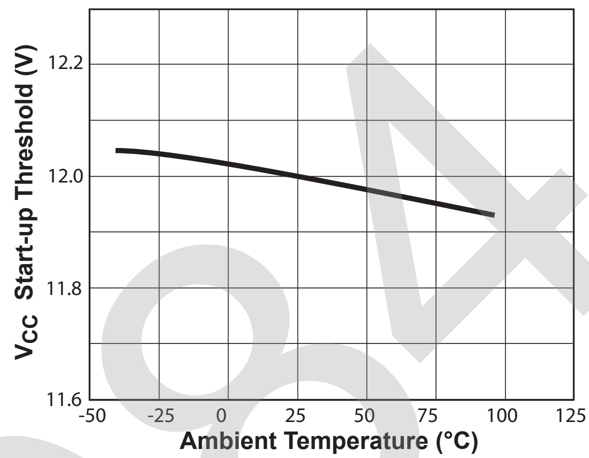


Figure 7.2 : Start-Up Threshold vs. Temperature

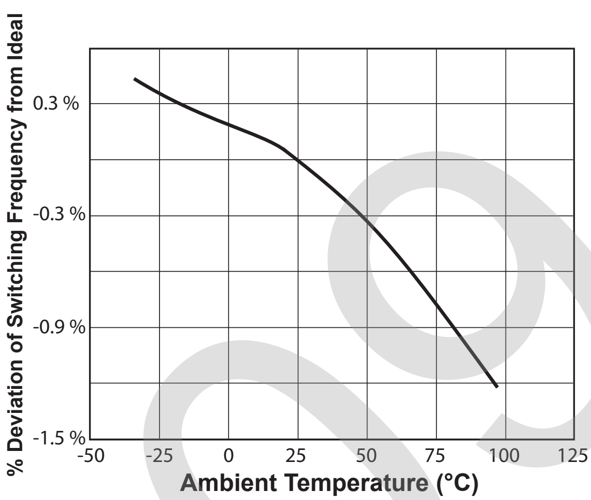


Figure 7.3 : % Deviation of Switching Frequency to Ideal Switching Frequency vs. Temperature

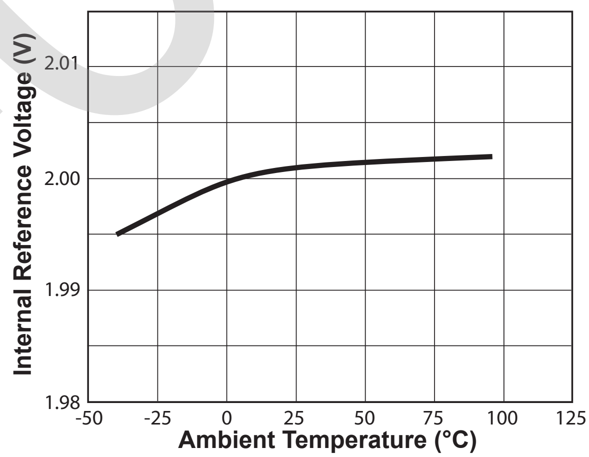


Figure 7.4 : Internal Reference vs. Temperature

8.0 Functional Block Diagram

iW3610 combines two functions: 1) wall dimmer type detection and dimmer phase measurement; and 2) output LED light dimming. It uses iWatt proprietary digital control technology, which consists of: 1) chopping circuit, which helps to increase the power factor and serves as a dynamic impedance to load the dimmer and 2) isolated flyback converter. The iW3610 provides a low cost solution which enables LED bulb to dim with typical wall dimmers. This allows LED bulbs to directly replace conventional incandescent bulbs with ease. The iW3610 works with a wide range of dimmers. It can detect and operate with leading-edge, and trailing-edge dimmers as well as no-dimmer. The controller operates in critical conduction mode (CCM) to achieve high power efficiency, as well as minimum EMI. It incorporates proprietary primary-feedback constant current control technology to achieve tight LED current regulation.

Figure 3.1 shows a typical iW3610 application schematic. Figure 8.1 shows the functional block diagram. The advanced digital control mechanism reduces system design time and improves reliability. Start-up algorithms makes sure the V_{CC} supply voltage is ready before powering up the IC.

The iW3610 provides multiple protection features for current limit, over voltage protection, and over temperature protection. The V_T function provides temperature drift compensation for the LED. The external NTC senses the LED temperature, when the temperature is high, the controller dims the LED light. When the temperature is over limit, the controller turns off.

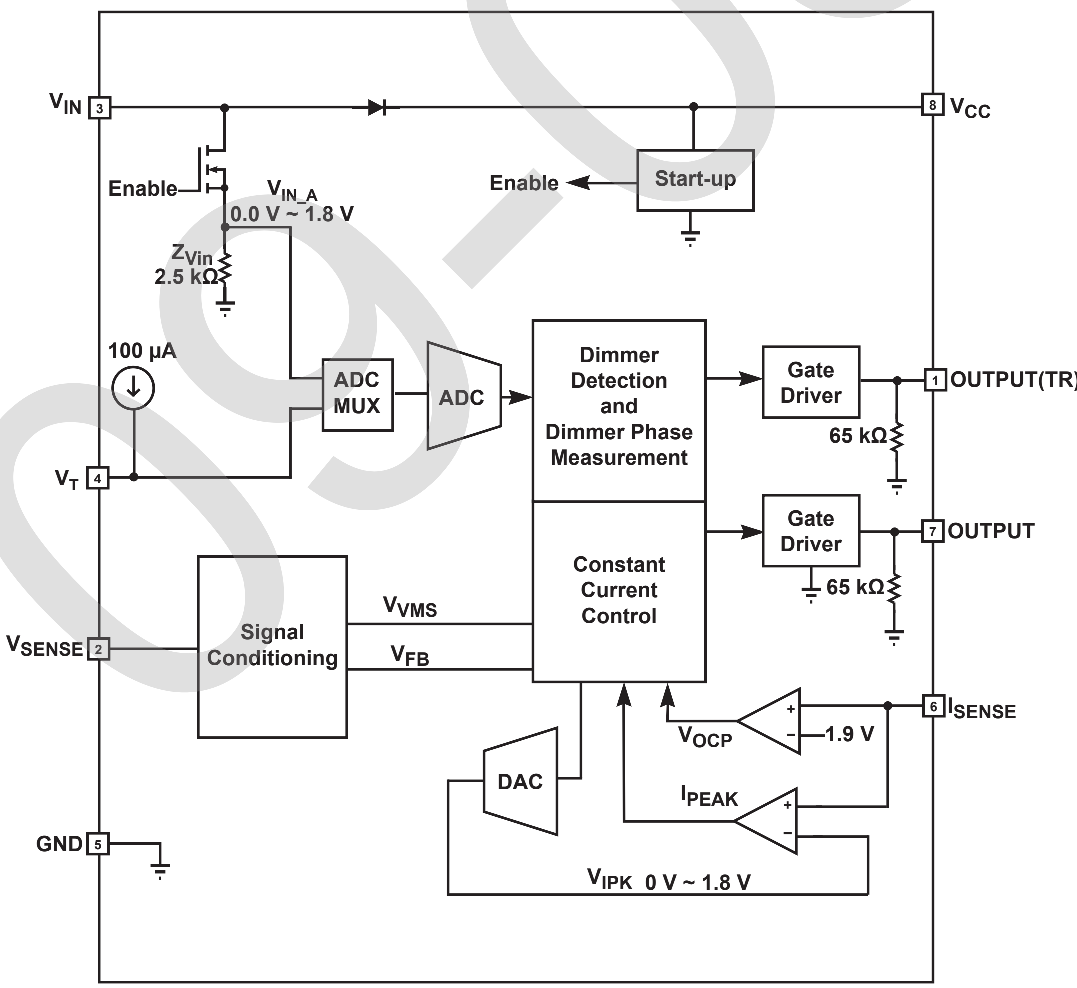


Figure 8.1 : iW3610 Functional Block Diagram

9.0 Theory of Operation

The iW3610 is a high performance AC/DC off-line power supply controller for dimmable LED luminaries, which uses advanced digital control technology to detect the dimmer type and dimmer phase. The dimmer conduct phase controls the LED brightness. A PWM-dimming scheme is used to modulate LED with dimming frequency of 900 Hz (default) or selectable. The iW3610 eliminates visible flicker. iW3610 can work with all types of wall dimmers including leading-edge dimmer, trailing-edge dimmer, as well as dimmer configurations such as R-type, R-C type or R-L type. The controller can also work when no dimmer is connected.

iW3610 operates in quasi-resonant mode to provide high efficiency and simplify EMI design. In addition, the iW3610 includes a number of key built-in protection features. Using iWatt's state-of-the-art primary-feedback technology, the iW3610 removes the need for secondary feedback circuitry while achieving excellent line and load regulation. iW3610 eliminates the need for loop compensation components while maintaining stable overall operating conditions. Pulse-by-pulse waveform analysis allows for accurate LED current regulations. Hence, iW3610 solutions are high performance, while maintaining minimal external component count and low bill of materials.

9.1 Pin Detail

Pin 1 – OUTPUT(TR)

Gate drive for the chopping circuit MOSFET switch.

Pin 2 – V_{SENSE}

Sense signal input from auxiliary winding. This provides the secondary voltage feedback used for output regulation.

Pin 3 – V_{IN}

Sense signal input from the rectified line voltage. V_{IN} is used for dimmer phase detection. The input line voltage is scaled down using a resistor network. It is used for input undervoltage and overvoltage protection. This pin also provides the supply current to the IC during start-up.

Pin 4 – V_T

External shutdown control. If the shutdown control is not used, this pin should be connected to GND via a resistor.

Pin 5 – GND

Ground.

Pin 6 – I_{SENSE}

Primary current sense. Used for cycle by cycle peak current control.

Pin 7 – OUTPUT

Gate drive for the external MOSFET switch.

Pin 8 – V_{CC}

Power supply for the controller during normal operation. The controller will start up when V_{CC} reaches 12 V (typical) and will shut-down when the V_{CC} voltage is below 7.5 V (typical). A decoupling capacitor should be connected between the V_{CC} pin and GND.

9.2 Wall Dimmer Detections

There are two types of wall dimmers: leading-edge dimmer and trailing-edge dimmer.

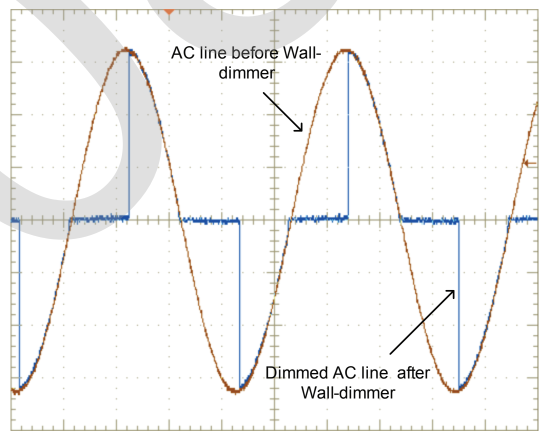


Figure 9.1 : Leading-Edge Wall Dimmer Waveforms

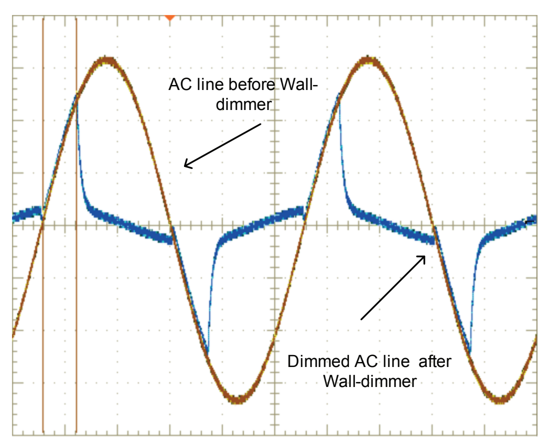


Figure 9.2 : Trailing-Edge Wall Dimmer Waveforms

Dimmer detection, or discovery, takes place during the third cycle after start-up. The controller does this in two stages. The first stage determines whether a dimmer is present, and the second stage uses measurements to determine if the dimmer (if present) is a leading-edge dimmer or a trailing-edge dimmer.

V_{CROSS} is internally generated by comparing the digitalized V_{IN} signal to the threshold of 0.1 V. During the first stage, the time t_{ZERO}, when V_{IN} is below a threshold of 0.1 V, is measured. If t_{ZERO} exceeds the time threshold of 600 µs, then the controller determines that a dimmer is present.

If stage one determines there is no dimmer present, then the controller sets the dimmer type to 'no dimmer'. If a dimmer is detected, then the controller uses the filtered derivatives to decide which type of dimmer is present. Since a leading-edge dimmer is easier to identify using derivatives than a trailing-edge dimmer, we look for the leading-edge dimmer signature. If this signature is found, then the controller decides that a leading-edge dimmer is present, otherwise it decides, by default, that a trailing-edge dimmer is present.

During the dimmer detection stage, the OUTPUT(TR) keeps high to turn on the switch FET in the chopping circuit. This creates a pure resistive load for the wall dimmer.

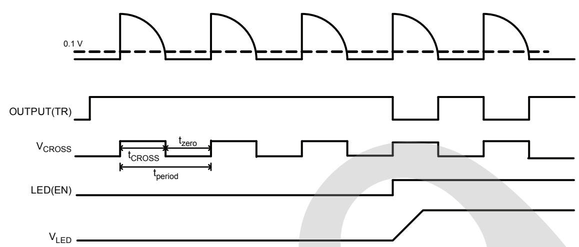


Figure 9.3 : Dimmer Detection

9.3 Dimmer Tracking and Phase Measurements

The dimmer detection algorithm and the dimmer tracking algorithm both depend on an accurate input voltage period measurement. The V_{IN} period is measured during the second cycle of the dimmer discovery process and is latched for use thereafter. It measures the AC half-cycle period with a resolution of 16 µs, such that a 50Hz mains voltage would nominally yield a period of $\frac{1}{2}\times\frac{1}{50Hz\cdot16\mu s}=625$. Using the measured V_{IN} period in subsequent calculations rather than a constant allows for automatic 50 Hz/60 Hz operation and allows for a 10% frequency variation.

Dimmer tracking and phase measurement are similar with respect to the different dimmer types. One significant difference has to do with how the falling edge of the dimmer is measured, and when the load is applied at the end of the cycle. Some minor differences include: the difference in the fixed offset that is added to the measured dimmer phase value prior to its use in the PWM processing chain, and the unfiltered input voltage which is used to determine the start of a cycle (rising threshold), in the case of a leading-edge dimmer.

The phase measurement starts when the rising threshold is exceeded and counts input voltage samples, with a resolution of 16 µs, until the next rising threshold.

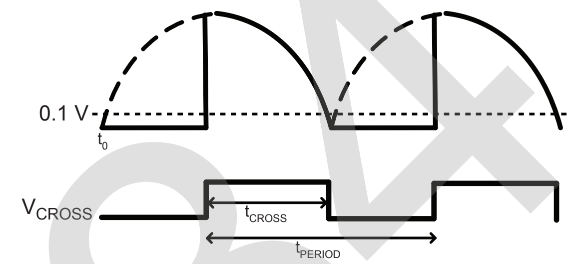


Figure 9.4 : Dimmer Phase Measurement

The dimmer phase is calculated as:

$$\text{Dimmer Phase} = \frac{t_{CROSS}}{t_{PERIOD}} \qquad (9.1)$$

The calculated dimmer phase is used to generate the signal D_{RATIO}. If the dimmer phase is less than 0.15 then the D_{RATIO} is clamped at 0.14, if the dimmer phase is greater than 0.8 then D_{RATIO} is clamped at 1.0, otherwise D_{RATIO} is calculated by equation 9.2.

$$D_{RATIO} = \text{Dimmer Phase} \times K_1 - K_2 \qquad (9.2)$$

Where, K_1 is set at 1.63 and K_2 is set at 0.3.

LED power output is modulated by D_{RATIO}. When D_{RATIO} is 1, the converter outputs 100% nominal power to LED. If D_{RATIO} is 0.1, the converter output 10% of nominal power to LED. The V_{Isense}, which modulate the output LED current, is set at the nominal value. V_{Isense} is modulated as:

$$V_{Isense} = V_{Isense(NOM)} \times D_{RATIO} \qquad (9.3)$$

9.4 Chopping Operation

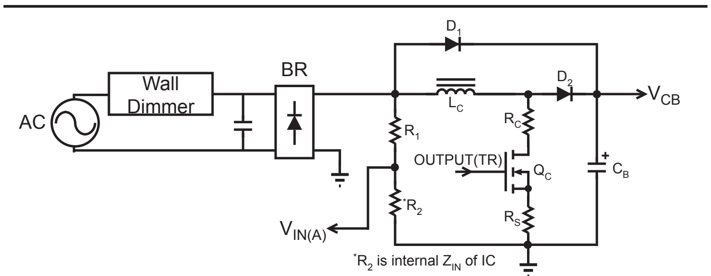


Figure 9.5 : Chopping Schematic

Chopping circuit provides the dynamic impedance for the dimmer and builds the energy to the LED power converter. It consists of L_C, Q_C, R_C, R_S, D_1, D_2, R_1 and R_2, as well as C_B. L_C is the chopping inductor. During the chopping period, L_C is used to store the energy when the Q_C is on, and then release the energy to C_B when Q_C is off. The on-time of Q_C during the chopping period is calculated by the following equation:

$$T_{ON(Qc)} = 4\mu s - 2.2\,{}^{\mu s}\!/\!_{V} \times V_{IN(A)} \qquad (9.4)$$

The period of Q_C is calculated by:

$$T_{PERIOD(Qc)} = 12.2\mu s + 8.8\,{}^{\mu s}\!/\!_{V} \times V_{IN(A)} \qquad (9.5)$$

$V_{IN(A)}$ is the scale voltage of V_{IN}. V_{CB} is the voltage across C_B. t_{CROSS} is generated by the internal digital block (refer to figure 9.6). When $V_{IN(A)}$ is higher than the predefined threshold of V_{IN} and the rising edge of V_{IN} is detected, t_{CROSS} is set to high. When the falling-edge of V_{IN} is detect, t_{CROSS} is reset to zero. When t_{CROSS} is low, Q_C is always on. When t_{CROSS} is zero, Q_C operates with the chopping period.

During the chopping period, the average current of L_C is in phase with the input AC line voltage, so it inherently generates a high power factor. D_1 in the chopping circuit is used to charge C_B when the voltage of C_B is lower than the input line voltage. This helps reduce the inrush current when the TRIAC is fired.

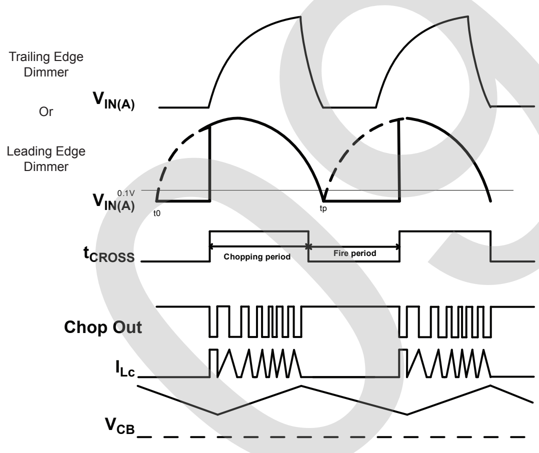


Figure 9.6 : Signals of Chopping Circuit

9.5 Start-up

Prior to start-up the V_{IN} pin charges up the V_{CC} capacitor through a diode between V_{IN} and V_{CC}. When V_{CC} is fully charged to a voltage higher than the start-up threshold $V_{CC(ST)}$, the ENABLE signal becomes active and enables the control logic, shown by Figure 9.7. When the control logic is enabled, the controller enters into normal operation mode. During the first 3 half AC cycles, OUTPUT(TR) keeps high. After the dimmer type and AC line period are measured, the constant current stage is enabled and the output voltage starts to ramp up. When the output voltage is above the forward voltage of LED, the controller begins to operate in constant current mode.

An adaptive soft-start control algorithm is applied during start-up state, where the initial output pulses are small and gradually get larger until the full pulse width is achieved. The peak current is limited cycle by cycle by the I_{PEAK} comparator.

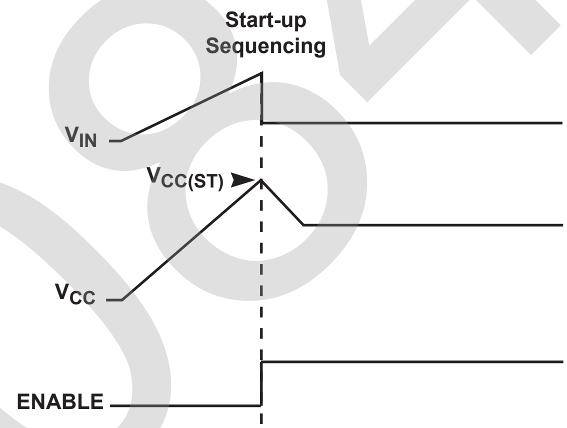


Figure 9.7 : Start-up Sequencing Diagram

9.6 Understanding Primary Feedback

Figure 9.8 illustrates a simplified flyback converter. When the switch Q_1 conducts during $t_{ON}(t)$, the current $i_g(t)$ is directly drawn from rectified sinusoid $v_g(t)$. The energy $E_g(t)$ is stored in the magnetizing inductance L_M. The rectifying diode D_1 is reverse biased and the load current I_O is supplied by the secondary capacitor C_O. When Q_1 turns off, D_1 conducts and the stored energy $E_g(t)$ is delivered to the output.

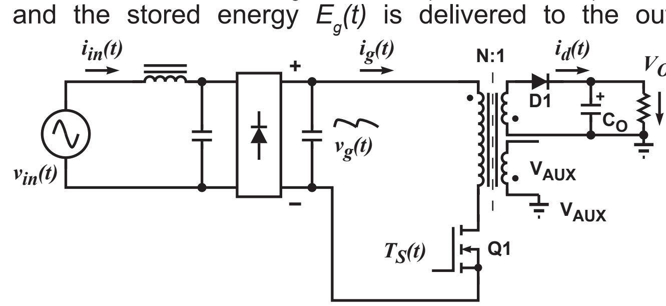


Figure 9.8 : Simplified Flyback Converter

In order to tightly regulate the output voltage, the information about the output voltage and load current needs to be accurately sensed. In the DCM flyback converter, this information can be read via the auxiliary winding or the primary magnetizing inductance (L_M). During the Q_1 on-time, the load current is supplied from the output filter capacitor C_O.

The voltage across L_M is $v_g(t)$, assuming the voltage dropped across Q_1 is zero. The current in Q_1 ramps up linearly at a rate of:

$$\frac{di_g(t)}{dt} = \frac{v_g(t)}{L_M} \tag{9.6}$$

At the end of on-time, the current has ramped up to:

$$i_{g\_peak}(t) = \frac{v_g(t) \times t_{ON}}{L_M} \tag{9.7}$$

This current represents a stored energy of:

$$E_g = \frac{L_M}{2} \times i_{g\_peak}(t)^2 \tag{9.8}$$

When Q_1 turns off, $i_g(t)$ in L_M forces a reversal of polarities on all windings. Ignoring the communication-time caused by the leakage inductance L_K at the instant of turn-off, the primary current transfers to the secondary at a peak amplitude of:

$$i_d(t) = \frac{N_P}{N_S} \times i_{g\_peak}(t) \tag{9.9}$$

Assuming the secondary winding is master and the auxiliary winding is slave.

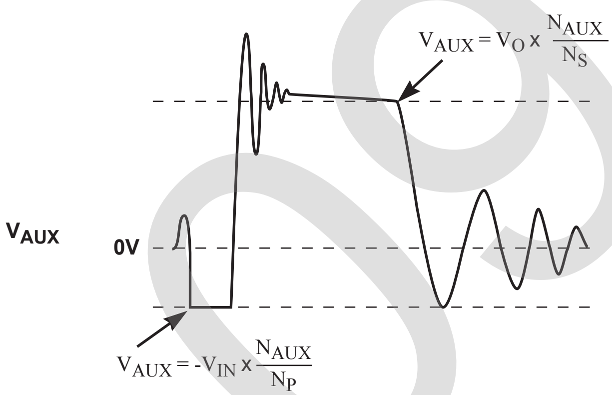


Figure 9.9 : Auxiliary Voltage Waveforms

The auxiliary voltage is given by:

$$V_{AUX} = \frac{N_{AUX}}{N_S}(V_O + \Delta V) \tag{9.10}$$

and reflects the output voltage as shown in Figure 9.9.

The voltage at the load differs from the secondary voltage by a diode drop and IR losses. The diode drop is a function of current, as are IR losses. Thus, if the secondary voltage is always read at a constant secondary current, the difference between the output voltage and the secondary voltage will be a fixed *ΔV*. Furthermore, if the voltage can be read when the secondary current is small; for example, at the knee of the auxiliary waveform (see Figure 9.9), then *ΔV* will also be small. With the iW3610, *ΔV* can be ignored.

The real-time waveform analyzer in the iW3610 reads the auxiliary waveform information cycle by cycle. The part then generates a feedback voltage V_{FB}. The V_{FB} signal precisely represents the output voltage and is used to regulate the output voltage.

9.7 Valley Mode Switching

In order to reduce switching losses in the MOSFET and EMI, the iW3610 employs valley mode switching when during constant output current operation. So, the EMI and switching losses are still minimized during CC mode. In valley mode switching, the MOSFET switch is turned on at the point where the resonant voltage across the drain and source of the MOSFET is at its lowest point (see Figure 9.10). By switching at the lowest V_{DS}, the switching loss will be minimized.

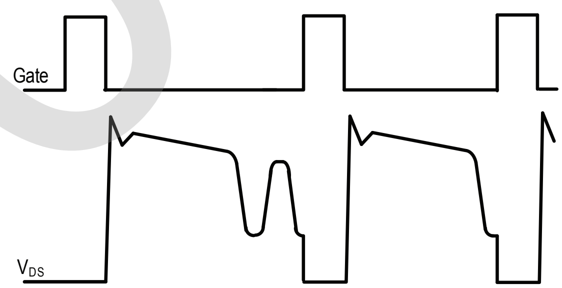


Figure 9.10 : Valley Mode Switching

Turning on at the lowest V_{DS} generates lowest dV/dt, thus valley mode switching can also reduce EMI. To limit the switching frequency range, the iW3610 can skips valleys (seen in the first cycle in Figure 9.10) when the switching frequency becomes too high.

At each of the switching cycles, the falling edge of V_{SENSE} is checked. If the falling edge of V_{SENSE} is not detected, the off-time will be extended until the falling edge of V_{SENSE} is detected. The maximum allowed transformer reset time is 120 µs. When the transformer reset time reaches this maximum reset time, the iW3610 immediately shuts off.

9.8 Constant LED Current Operation

iW3610 incorporates a patented primary-side only constant current regulation technology. The iW3610 regulates the output current at a constant level regardless of the output voltage, while avoiding continuous conduction mode. To achieve this regulation the iW3610 senses the load current indirectly through the primary current. The primary current is detected by the ISENSE pin through a resistor from the MOSFET source to ground.

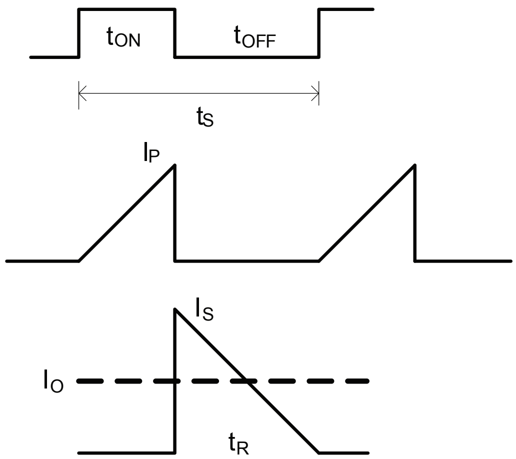


Figure 9.11 : Constant LED Current Regulation

The I_{SENSE} resistor determines the maximum current output of the power supply. The output current of the power supply is determined by:

$$I_{OUT} = \frac{1}{2} \times N_{PS} \times \frac{V_{IPK}}{R_{SENSE}} \times \frac{t_R}{t_S} \tag{9.11}$$

9.9 V_{IN} Resistors

V_{IN} resistors are chosen primarily to scale down the input voltage for the IC. The scale factor for the input voltage in the IC is 0.0043 for high line, and 0.0086 for low line; the internal impedance of this pin is 2.5 kΩ. Therefore, the V_{IN} resistors should equate to:

$$R_{Vin} = \frac{2.5k\Omega}{0.0043} - 2.5k\Omega = 463k\Omega \tag{9.12}$$

9.10 Voltage Protection Functions

The iW3610 includes a function that protects against an output overvoltage (OVP).

The output voltage is monitored by the V_{SENSE} pin. If the voltage at this pin exceed its overvoltage threshold the iW3610 shuts down immediately. However, the IC remains biased which discharges the V_{CC} supply. Once V_{CC} drops below the UVLO threshold, the controller resets itself and then initiates a new soft-start cycle. The controller continues attempting start-up until the fault condition is removed.

9.11 PCL, OC and SRS Protection

Peak-current limit (PCL), over-current protection (OCP) and sense-resistor short protection (SRSP) are features built-into the iW3610. With the I_{SENSE} pin the iW3610 is able to monitor the primary peak current. This allows for cycle by cycle peak current control and limit. When the primary peak current multiplied by the I_{SENSE} sense resistor is greater than 1.89 V over current is detected and the IC will immediately turn off the gate drive until the next cycle. The output driver will send out switching pulse in the next cycle, and the switching pulse will continue if the OCP threshold is not reached; or, the switching pulse will turn off again if the OCP threshold is still reached.

If the I_{SENSE} sense resistor is shorted there is a potential danger of the over current condition not being detected. Thus the IC is designed to detect this sense-resistor-short fault after the start up, and shutdown immediately. The V_{CC} will be discharged since the IC remains biased. Once V_{CC} drops below the UVLO threshold, the controller resets itself and then initiates a new soft-start cycle. The controller continues attempting start-up, but does not fully start-up until the fault condition is removed.

9.12 Thermal Design

The iW3610 is typically installed inside a small enclosure, where space and air volumes are constrained. Under these circumstances θ_{JA} (thermal resistance, junction to ambient) measurements do not provide useful information for this type of application. Instead we have provided ψ_{JB} which estimates the increase in die junction temperature relative to the PCB surface temperature. Figure 9.12 shows the PCB surface temperature is measured at the IC's GND pin pad.

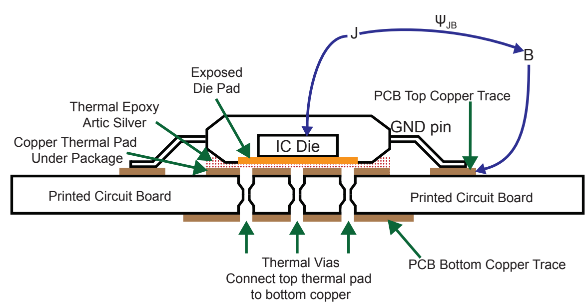


Figure 9.12 : Ways to Improve Thermal Resistance

Using ψ_{JB} the junction temperature (T_J) of the IC can be found using the equation below.

$$T_J = T_B + P_H \cdot \Psi_{JB} \tag{9.13}$$

where, T_B is the PCB surface temperature and P_H is the power applied to the chip or the product of V_{CC} and I_{CCQ}.

The iW3610 uses an exposed pad package to reduce the thermal resistance of the package. Although just by using an exposed package can provide some thermal resistance improvement, more significant improvements can be obtained with simple PCB layout and design. Figure 9.12 demonstrates some recommended techniques to improve thermal resistance, which are also highlighted below.

Ways to Improve Thermal Resistance

- Increase PCB area and associated amount of copper interconnect.
- Use thermal adhesive to attach the package to a thermal pad on PCB.
- Connect PCB thermal pad to additional copper on PCB.

Environment	Ψ_{JB}
No glue	70 °C/W
Use thermal glue to pad	63 °C/W
Use thermal glue to pad with thermal vias	49 °C/W

Table 9.1 : Improvements in ψ_{JB} Based on Limited Experimentation

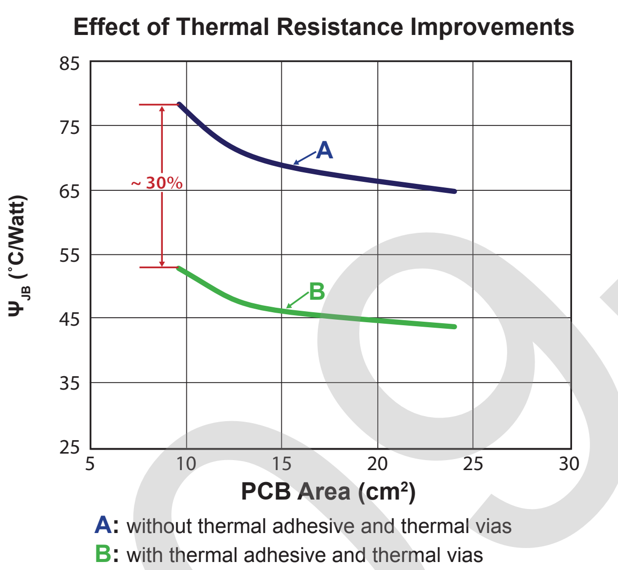


Figure 9.13 : Effect of Thermal Resistance Improvements

Figure 9.13 shows improvement of approximately 30% in thermal resistance across different PCB sizes when the exposed pad is attached to PCB using a thermal adhesive and thermal vias connect the pad to a larger plate on the opposing side of the PCB.

10.0 Performance Characteristics

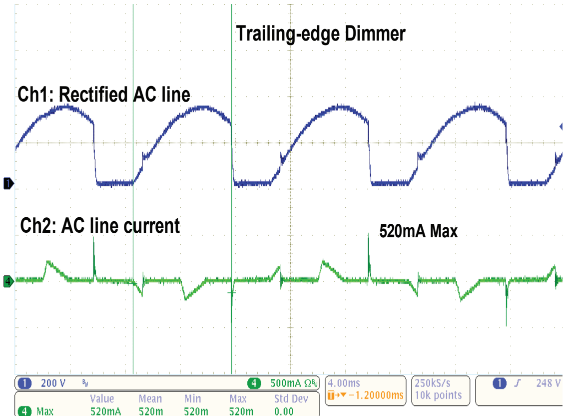


Figure 10.1 : Trailing Edge Dimmer 1

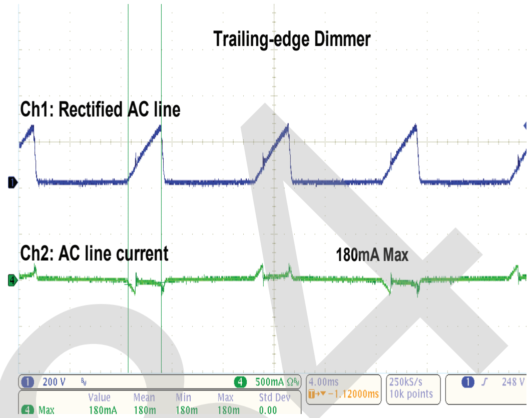


Figure 10.2 : Trailing Edge Dimmer 2

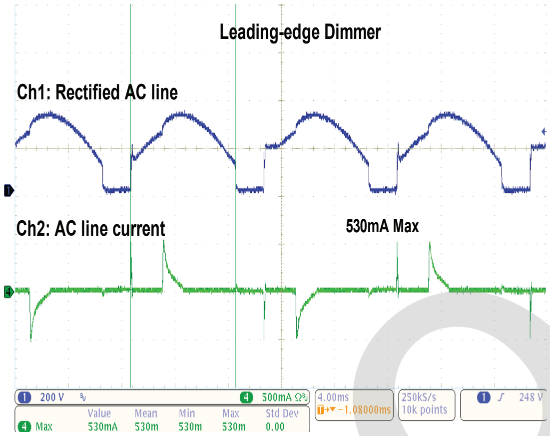


Figure 10.3 : Leading Edge Dimmer 1

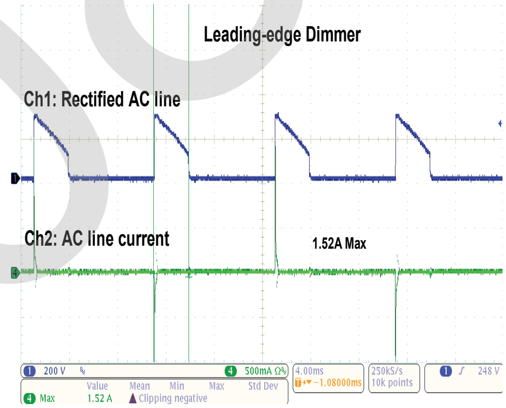


Figure 10.4 : Leading Edge Dimmer 2

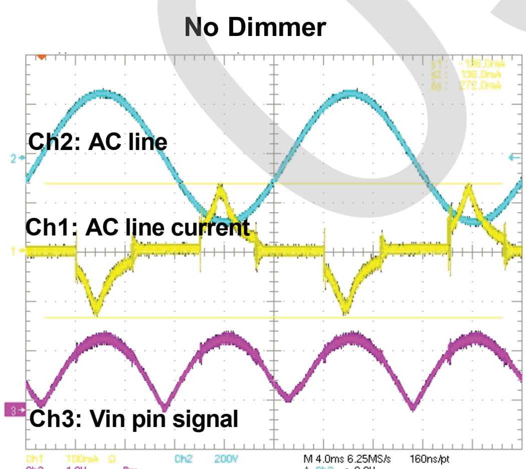


Figure 10.5 : No Dimmer

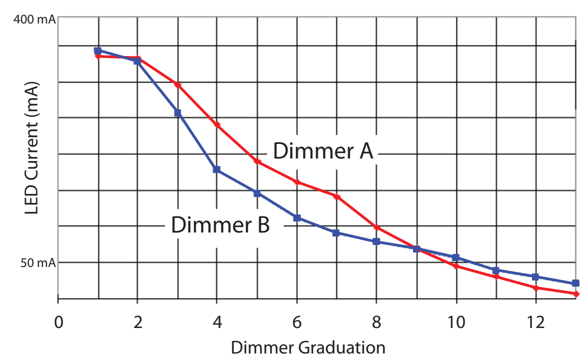


Figure 10.6 : Dimmer Graduation

11.0 Typical Application Schematic

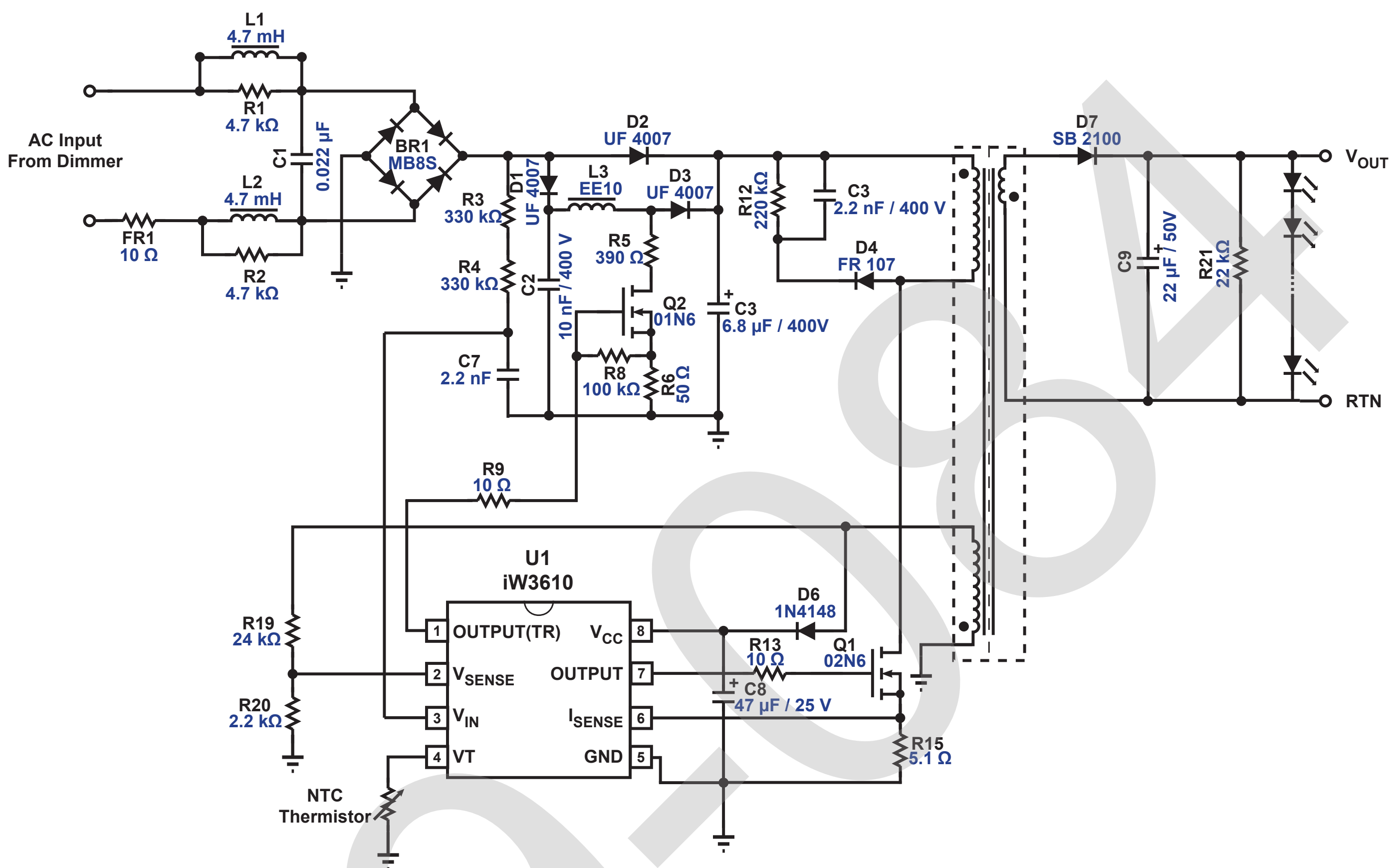
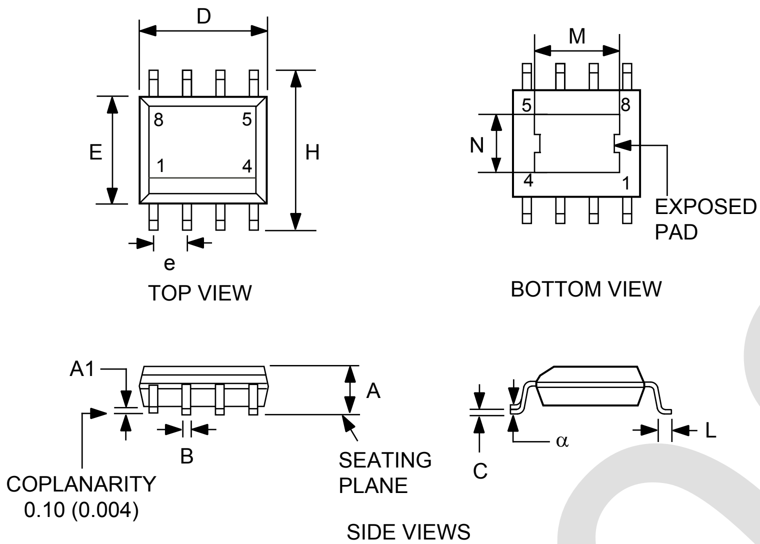


Figure 11.1 : iW3610 Typical Application Schematic

12.0 Physical Dimensions

8-Lead Small Outline (SOIC) Package



Symbol	Inches		Millimeters	
	MIN	MAX	MIN	MAX
A	0.051	0.067	1.30	1.70
A1	0.0020	0.0060	0.05	0.150
B	0.014	0.019	0.36	0.48
C	0.007	0.010	0.18	0.25
D	0.189	0.197	4.80	5.00
E	0.150	0.157	3.81	3.99
e	0.050 BSC		1.27 BSC	
H	0.228	0.244	5.79	6.20
N	0.086	0.094	2.18	2.39
M	0.118	0.126	3.00	3.20
L	0.016	0.050	0.41	1.27
α	0°	8°		

Figure 11.2 : Physical dimensions, 8-lead SOIC package

Compliant to JEDEC Standard MS12F

Controlling dimensions are in inches; millimeter dimensions are for reference only

This product is RoHS compliant and Halide free.

Soldering Temperature Resistance:
[a] Package is IPC/JEDEC Std 020D Moisture Sensitivity Level 1
[b] Package exceeds JEDEC Std No. 22-A111 for Solder Immersion Resistance; package can withstand 10 s immersion < 270˚C

Dimension D does not include mold flash, protrusions or gate burrs. Mold flash, protrusions or gate burrs shall not exceed 0.15 mm per end. Dimension E does not include interlead flash or protrusion. Interlead flash or protrusion shall not exceed 0.25 mm per side.

The package top may be smaller than the package bottom. Dimensions D and E are determined at the outermost extremes of the plastic bocy exclusive of mold flash, tie bar burrs, gate burrs and interlead flash, but including any mismatch between the top and bottom of the plastic body.

13.0 Ordering Information

Part Number	Options	Package	Description
iW3610-00		SOIC-8	Tape & Reel[1]

Note 1: Tape & Reel packing quantity is 2,500/reel.

About iWatt

iWatt Inc. is a fabless semiconductor company that develops intelligent power management ICs for computer, communication, and consumer markets. The company's patented *pulseTrain*™ technology, the industry's first truly digital approach to power system regulation, is revolutionizing power supply design.

Trademark Information

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