FAIRCHILD SEMICONDUCTOR®

April 2009

FSR510

Highly Integrated Synchronous Rectification Combination Controller for Quasi-Resonant PWM Controller

Features

- Highly Integrated Synchronous Rectification (SR) Combination Controller, Combining MOSFET and SR Controller
- Built-In Ultra-Low R_{DS-ON} MOSFET
- Internal Linear-Predict Timing Control is Specially Designed for Quasi-Resonant (QR) and Discontinuous Conduction Mode (DCM) Operation
- Internal Green-Mode Operation for Better No-Load Power Consumption
- PWM Frequency Tracking with Secondary-Side Winding Detection
- Ultra-Low V_{DD} Operating Voltage (5.3~25V) for Various Output Voltage Applications
- Ultra-Low Green-Mode Operating Current: 0.8mA (Typical)
- V_{DD} Pin Over-Voltage Protection
- Gate Driver Clamp: 12V (Typical)
- TO220-6L Package

Applications

- AC/DC Notebook Adapters
- Open-Frame SMPS
- Battery Charger

Description

The highly integrated FSR510 combines a low R_{DS-ON} MOSFET and synchronous rectification (SR) controller. Its high-level of integration allows design of a cost-effective power supply with fewer external components.

The proprietary, innovative, linear-predict timing control technique provides synchronous rectification control for flyback converters operating in Quasi-Resonant (QR) mode and Discontinuous Conduction Mode (DCM). The benefits of this technique include simple control method, no current-sense circuitry, and PWM frequency tracking with secondary-side winding detection. At light-load condition, the FSR510 enters green mode, where FSR510 stops switching operation and shuts down the major internal block to maintain the power consumption at minimum level.

The FSR510 can be used with flyback converters using existing QR PWM controllers (FAN6300, FAN692x).

Related Application Notes

- *AN6085- Secondary Synchronous Rectifier for Quasi-Resonant Controllers*

Ordering Information

Part Number	Operating Temperature Range	MOSFET R_{DS-ON}	MOSFET BV_{DSS}	Package	Eco Status	Packing Method
FSR510R09GZ	-40 to +105°C	9mΩ	100V	TO-220-6L	RoHS	Tube

For Fairchild's definition of Eco Status, please visit: http://www.fairchildsemi.com/company/green/rohs_green.html.

Application Diagram

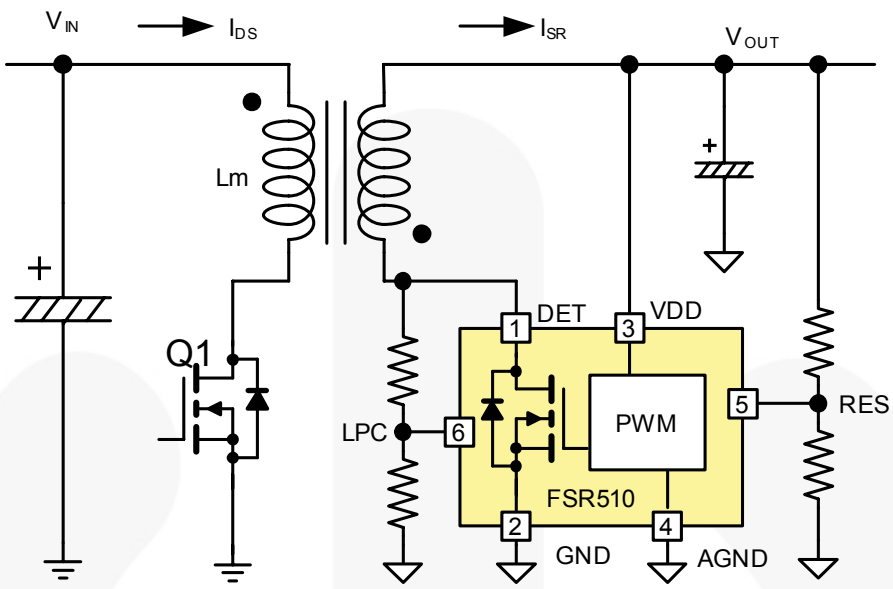


Figure 1. Typical Application Circuit

Block Diagram

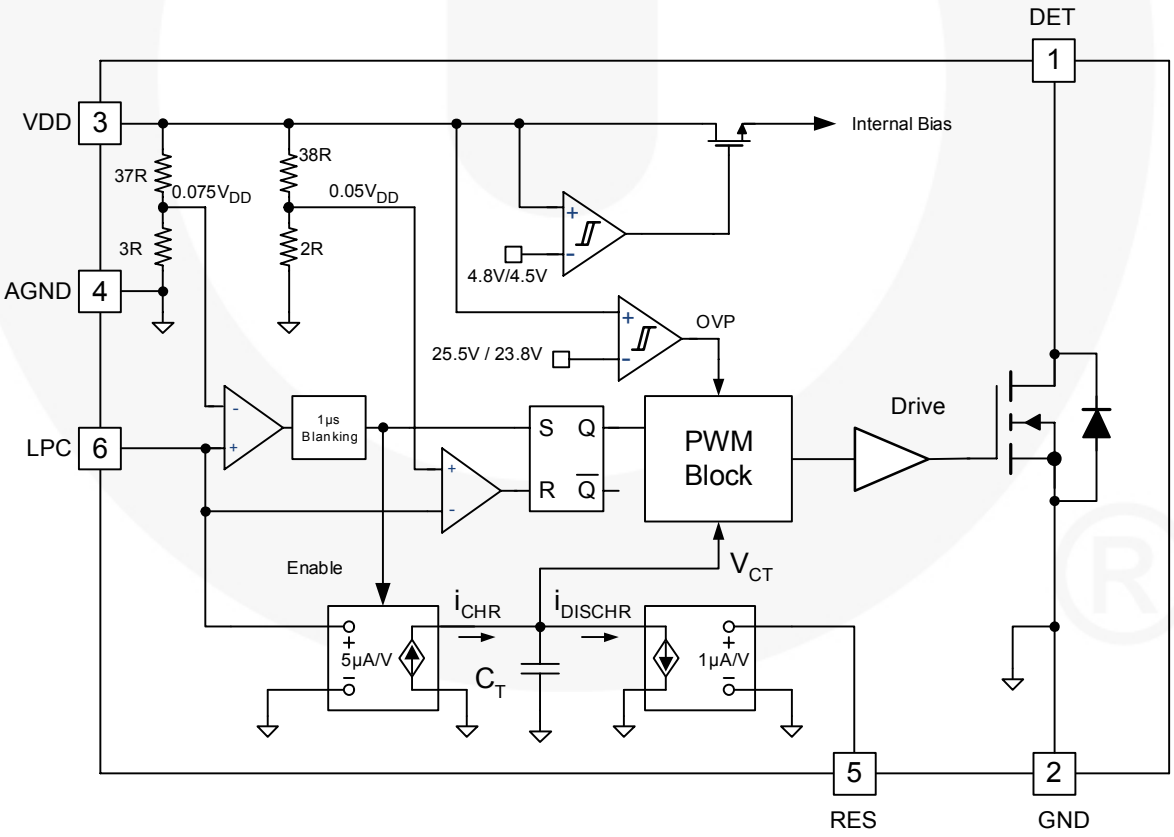
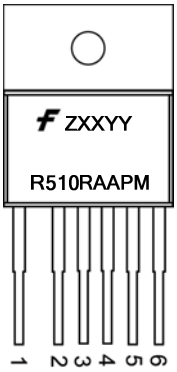


Figure 2. Functional Block Diagram

Marking Information



F: Fairchild Logo
Z: Plant Code
XX: Year Code
YY: Week Code
AA: MOSFET R_{DS-ON}
P: Z=Pb Free
M: Manufacture Flow Code

Figure 3. Marking Diagram

Pin Configuration

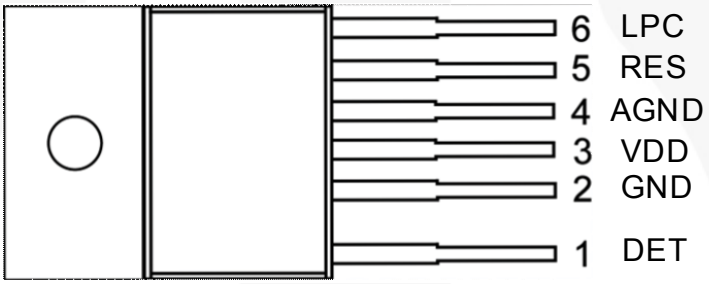


Figure 4. Pin Configuration

Pin Definitions

Pin #	Name	Description
1	DET	**Drain Terminal**. High-voltage MOSFET drain connection.
2	GND	**Ground**. MOSFET source connection.
3	VDD	**Supply Voltage**. The supply voltage pin for internal controller. The threshold voltages for startup and turn-off are 4.8V and 4.5V, respectively. The operating current is lower than 8mA under normal operation.
4	AGND	**Signal Ground**.
5	RES	**Reset Control of Linear Predict**. RES pin is used to detect output voltage level through a voltage divider. An internal current source, I_{DISCHR} is modulated by this voltage level on the RES pin.
6	LPC	**Control of Linear Predict**. The LPC pin is used to detect the voltage on the secondary winding during the primary-side MOSFET turn-on period. An internal current, I_{CHR} is modulated by the voltage level on the LPC pin.

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter	Min.	Max.	Unit
V_{DD}	DC Supply Voltage		30	V
V_{HV}	DET		100	V
V_L	LPC, RES	-0.3	7.0	V
P_D	Power Dissipation		45	W
T_J	Operating Junction Temperature		+150	°C
T_{STG}	Storage Temperature Range	-55	+150	°C
T_L	Lead Temperature (Soldering, 10 Seconds)		+260	°C
ESD	Human Body Model, JESD22-A114		4.00	kV
	Charged Device Model, JESD22-C101		1.25	

Note:
1. All voltage values, except differential voltages, are given with respect to GND pin.

Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to Absolute Maximum Ratings.

Symbol	Parameter	Min.	Max.	Unit
T_A	Operating Ambient Temperature	-40	+105	°C

Electrical Characteristics

V_{DD}=15V and T_A=25°C, unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
V_{OP}	Continuously Operating Voltage		V_{DD-OFF}		25	V
V_{DD-ON}	Turn-On Threshold Voltage		4.3	4.8	5.3	V
V_{DD-OFF}	Turn-Off Threshold Voltage		4.0	4.5	5.0	V
$I_{DD-OP-1}$	Operating Current	V_{DD}=15V, DET=50KHz, MOSFET C_{ISS}=6185pF		7	8	mA
$I_{DD-GREEN}$	Operating Current in Green Mode	V_{DD}=15V,		0.8	1.0	mA
I_{DD-ST}	Startup Current	V_{DD}< V_{DD-ON}		150	200	µA
V_{DD-OVP}	V_{DD} Over-Voltage Protection			25.5		V
$V_{DD-OVP-HYST}$	Hysteresis Voltage for V_{DD} OVP		1.2	1.7	2.2	V
$t_{VDD-OVP}$	V_{DD} OVP Debounce Time		20	50	80	µs
Output Driver for Internal SR MOSFET Section						
V_Z	Output Voltage Maximum (Clamp)			12	14	V
V_{OL}	Output Voltage Low	V_{DD}=6V, I_O=50mA			0.5	V
V_{OH}	Output Voltage High	V_{DD}=6V, I_O=50mA	4			V
t_R	Rising Time	V_{DD}=12V, C_L=6nF, Out=2V~9V	30	70	120	ns
		V_{DD}=6V, C_L=6nF, Out=0.4V~4V	70	120	170	
t_F	Falling Time	V_{DD}=12V, C_L=6nF, Out=9V~2V	30	50	100	ns
		V_{DD}=6V, C_L=6nF, Out=4V~0.4V	50	90	130	
$t_{PD-HIGH-LPC}$	Propagation Delay to Out High	t_R: 0V~2V, V_{DD}=12V	200	250	300	ns
$t_{PD-LOW-LPC}$	Propagation Delay to Out Low	t_F: 100%~90%, V_{DD}=12V	130	180	230	ns
t_{ON-MAX}	Maximum On Time		20	22	24	µs
$t_{INHIBIT}$	Gate Inhibit Time			2.5		µs
LPC SECTION						
$V_{LPC-SOURCE}$	Lower Clamp Voltage	Source I_{LPC}=1µA		0.35		V
$I_{LPC-SOURCE}$	LPC Source Current	V_{LPC}=0V	80	100	120	µA
V_{LPC}	Linear Operation Range of LPC Pin Voltage	V_{DD}>5V	0.8		4.4	V
$Ratio_{LPC}$	LPC Transfer Ratio to I_{LPC}		4.5	5.0	5.5	µA/V
V_{LPC-EN}	SR Enabled Threshold Voltage	0.075•V_O+0.1, V_O=15V, V_O=V_{DD}	1.125	1.225	1.325	V
$V_{LPC-TH-HIGH}$	Threshold Voltage on LPC Rising Edge	0.05•V_O+0.1, V_O=15V, V_O=V_{DD}	0.75	0.85	0.95	V
t_{LPC-EN}	Minimum LPC Time to Enable the SR Gate V_{DET}>$V_{DET-TH-HIGH}$	V_{LPC-EN} according to V_{DD}	0.85	1	1.15	µs

Continued on the following page…

Electrical Characteristics

V_{DD}=15V and T_A=25°C, unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
RES SECTION						
V_{RES-EN}	The Threshold Voltage of V_{RES} to enable SR MOS			0.5		V
$t_{RES-LOW}$	The Debounce Time for Disable RES Function			50		µs
V_{RES}	Linear Operation Range of RES Pin Voltage	V_{DD}>5V	0.8		4.4	V
$Ratio_{RES}$	V_{RES} Transfer Ratio to I_{RES}		0.9	1.0	1.1	µA/V
$Ratio_{LPC-RES}$	Ratio between LPC and RES Pin		4.75	5.00	5.25	
GREEN MODE SECTION						
$t_{GREEN-OFF}$	Discharge Time t_{DISCHR} to Leave Green-Mode		5.1	5.8	6.5	µs
$t_{GREEN-ON}$	Discharge Time t_{DISCHR} to Enter Green-Mode		4.3	4.8	5.3	µs
$t_{GREEN-TIME}$	Cycle Time to Enter/Leaving Green-Mode[2]			9		times
MOSFET Section						
B_{VDSS}	Drain-Source Breakdown Voltage	I_{DET}=250µA, V_{DD}=0V, T_C=25°C	100			V
$\Delta B_{VDSS}/\Delta T_J$	Breakdown Voltage Temperature Coefficient	I_{DET}=250µA, Referenced to 25°C		0.1		V/°C
$R_{DS(ON)}$	Static Drain-Source On-Resistance	V_{DD}=15V, I_{DET}=75A		7.2	9.0	mΩ
I_{DSS}	Drain-Source Leakage Current	$V_{DET-GND}$=100V, V_{DD}=0V			1	A
		$V_{DET-GND}$=100V, V_{DD}=0V, T_C=150°C			500	
t_{D-ON}	Turn-On Delay Time	$V_{DET-GND}$=50V, I_D=75A V_{DD}=10V[3,4]		107	224	ns
t_R	Turn-On Rise Time			322	655	
t_{D-OFF}	Turn-Off Delay Time			166	342	
t_F	Turn-Off Fall Time			149	309	

Notes:

2. Guaranteed by design.
3. Pulse test: pulse width≦300µs, duty cycle≦2%.
4. Essentially independent of operating temperature typical characteristics.

Functional Description

Basic Operation Principle of QR flyback converter with FSR510

Figure 5 shows the simplified circuit diagram of flyback converter using FSFR510. Typical waveforms are shown in Figure 6.

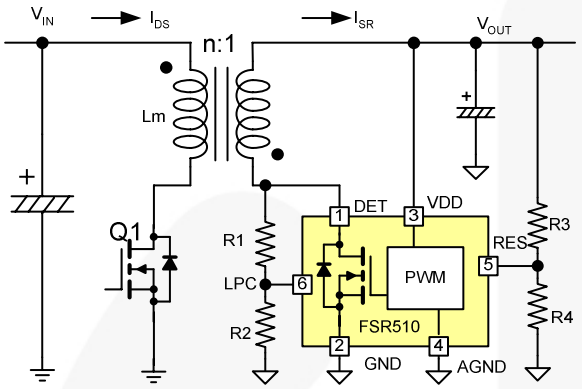


Figure 5. Typical Application Circuit

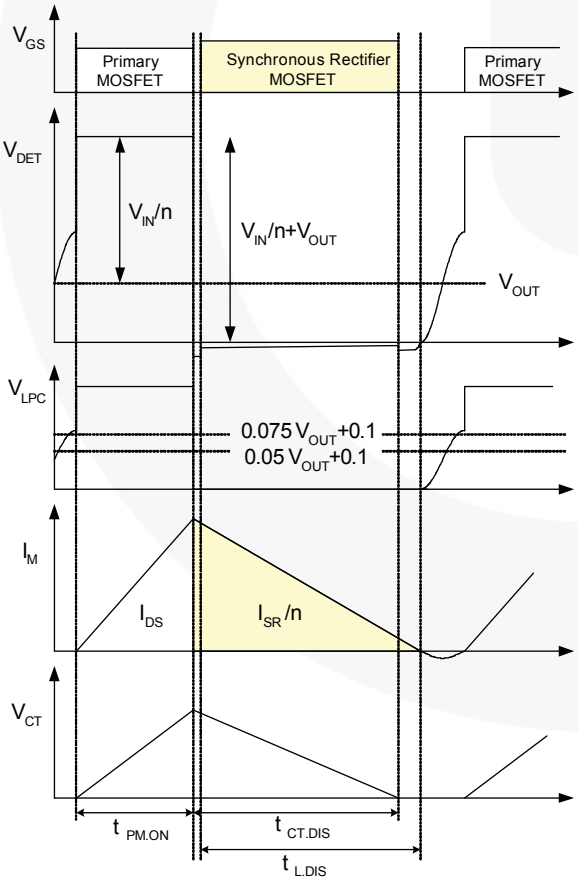


Figure 6. Typical Waveforms

The basic operations of quasi-resonant flyback converter with SR are:

- During the primary-side MOSFET ON time ($t_{PM.ON}$), input voltage (V_{IN}) is applied across the primary-side inductor (L_m). Then MOSFET current (I_{DS}) increases linearly from zero to the peak value. During this time, the DET pin voltage is the sum of output voltage (V_{OUT}) and the reflected input voltage (V_{IN}/n).

- When the primary-side MOSFET is turned off, the energy stored in the inductor forces the body diode of SR MOSFET to be turned on. Then the DET voltage drops to almost zero and the SR controller turns on SR MOSFET. During this period, the current through SR linearly decreases to zero. By linear predict control, the SR MOSFET is turned off just before the SR current reaches zero and the current continues flowing through the body diode of SR MOSFET until it reaches zero.

- When the SR MOSFET body diode current reaches zero, SR MOSFET body diode is naturally reverse biased and DET voltage begins to oscillate by the resonance between the primary-side inductor (L_m) and effective capacitance loaded across MOSFET with an amplitude of output voltage, as shown in the second waveform of Figure 6. The QR flyback converter turns on the primary-side MOSFET when DET voltage reaches its peak by resonance.

Linear Predict Timing Control

The SR MOSFET is turned on when the SR MOSFET body diode starts conducting and DET voltage drops to zero. FSR510 uses LPC pin with a voltage divider to sense the DET voltage and the threshold voltage for LPC to trigger SR MOSFET is $0.05V_{OUT}+0.1$, as shown in the third waveform of Figure 6.

The SR MOSFET is turned off just before the SR current reaches zero by linear predict timing control. To guarantee the proper operation SR, it is important to turn off SR MOSFET just before SR current reaches zero so that the body diode of SR MOSFET is naturally turned off. Figure 7 shows the internal block for linear predict timing control.

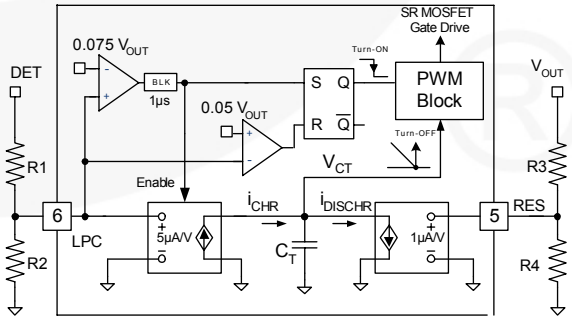


Figure 7. Linear Predict Block

The linear predict timing control circuit generates a replica (V_{CT}) of magnetizing current of flyback transformer using internal timing capacitor (C_T), as shown in Figure 7. Using the internal capacitor voltage, the inductor discharge time ($t_{L.DIS}$) can be detected indirectly, as shown in the last waveform of Figure 6. When C_T is discharged to zero, the SR controller turns off the SR MOSFET.

The voltage-second balance equation for the primary side inductance of flyback converter is given as

$$V_{IN} \cdot t_{PM.ON} = n \cdot V_{OUT} \cdot t_{L.DIS} \quad (1)$$

Then, the inductor current discharge time is given as:

$$t_{L.DIS} = \frac{V_{IN} \cdot t_{PM.ON}}{n \cdot V_{OUT}} \quad (2)$$

When the voltage scale-down ratio between RES and LPC is defined as K as below:

$$K = \frac{R_3 / (R_3 + R_4)}{R_2 / (R_1 + R_2)} \quad (3)$$

The current-second balance equation for internal timing capacitor (C_T) is obtained as:

$$(\frac{5}{K} \cdot (\frac{V_{IN}}{n} + V_{OUT}) - V_{OUT}) \cdot t_{PM.ON} = V_{OUT} \cdot t_{CT.DIS} \quad (4)$$

Then, the discharge time of C_T is given as:

$$t_{CT.DIS} = \frac{(\frac{5}{K} \cdot (\frac{V_{IN}}{n} + V_{OUT}) - V_{OUT}) \cdot t_{PM.ON}}{V_{OUT}} \quad (5)$$

When the voltage scale-down ratio between RES and LPC (K) is 5, the discharge time of C_T ($t_{CT.DIS}$) is same as inductor current discharge time ($t_{L.DIS}$). However, considering the tolerance of voltage divider resistors and internal circuit, the scale-down ratio (K) should be larger than 5 to guarantee that $t_{CT.DIS}$ is shorter than $t_{L.DIS}$. It is typical to set K around 5.5~6.

Since the voltage-to-current conversion circuit for the LPC pin is enabled only when LPC voltage goes above $0.075V_{OUT}$+0.1, as shown in the third waveform of Figure 7, the voltage divider for LPC should be determined so that it can satisfy:

$$\frac{R_2}{R_1 + R_2} \cdot (\frac{V_{IN.MIN}}{n} + V_{OUT}) > 0.075V_{OUT} + 0.1 \quad (6)$$

where $V_{IN.MIN}$ is the minimum input voltage of the flyback converter.

When designing the voltage divider networks for LPC and RES, the linear operation range of LPC and RES (1~4V) should be also considered as:

$$\frac{R_2}{R_1 + R_2} \cdot (\frac{V_{IN.MAX}}{n} + V_{OUT}) < 4 \quad (7)$$

$$\frac{R_4}{R3 + R_4} \cdot V_{OUT} > 4 \quad (8)$$

DCM Operation

FSR510 can be also used for Discontinuous Conduction Mode (DCM) or extended quasi-resonant operation (valley switching). In DCM operation, the DET voltage continues resonating until the primary-side MOSFET is turned on, as depicted in Figure 8. While DET voltage is resonating, DET voltage and LPC voltage drop to zero by resonance, which can trigger the turn-on of the SR MOSFET. To prevent fault triggering of the SR MOSFET in DCM operation, blanking time is introduced for LPC voltage. The SR MOSFET is not turned on even when LPC voltage drops below $0.05V_{OUT}$+0.1 unless LPC voltage stays above $0.075V_{OUT}$ +0.1 longer than the blanking time (1μs). The turn-on of the SR MOFET is inhibited for 2.5μs once the SR MOSFET is turned off to prevent fault triggering.

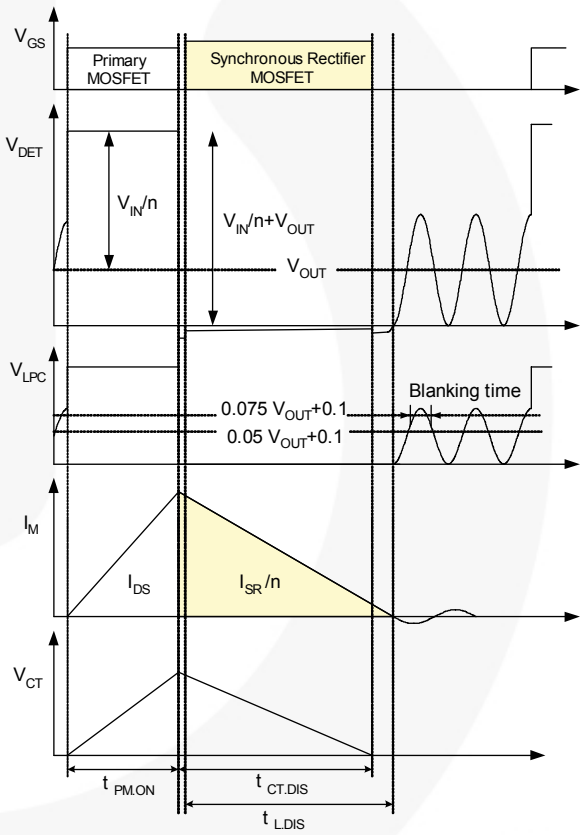


Figure 8. DCM Operation of FSR510

Green-Mode Operation

To minimize the power consumption at light-load condition, the SR circuit is disabled when the load decreases. As illustrated in Figure 9, the discharge times of inductor and internal timing capacitor decrease as load decreases. When the discharge time of internal timing capacitor is shorter than $t_{GREEN-ON}$ (around 4.8μs) for more than nine cycles, the SR circuit enters green mode, as shown in Figure 9. Once FSR510 enters green mode, the SR MOSFET stops switching and the major internal block is shut down to further reduce operating current of the SR controller. In green mode, the operating current reduces to 800μA. This allows

power supplies to meet the most stringent power conservation requirements. When the discharge time of the internal capacitor is longer than $t_{GREEN-OFF}$ (around 5.8μs) for more than nine cycles, the SR circuit is enabled and resumes the normal operation, as shown in Figure 10.

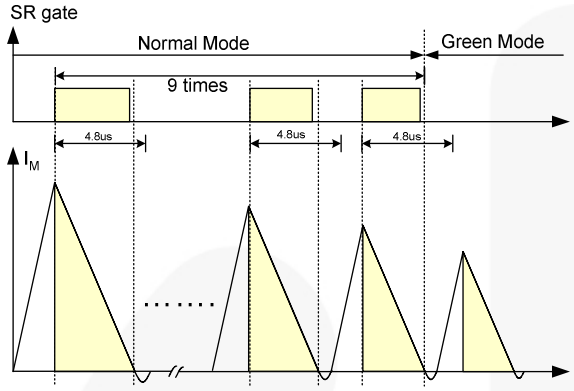


Figure 9. Entering Green Mode

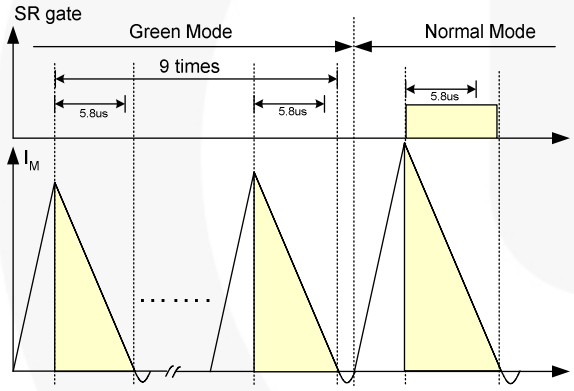


Figure 10. Resuming Normal Operation

Under-Voltage Lockout (UVLO)

The power ON and OFF V_{DD} threshold voltages of the FSR510 are fixed at 4.8V and 4.5V, respectively. With an ultra-low V_{DD} operating range, the FSR510 can be applied to various output voltage applications.

V_{DD} Pin Over-Voltage Protection

Over-voltage conditions are usually caused by open feedback loop. V_{DD} over-voltage protection has been built-in to prevent damage on SR MOSFET. When the voltage on V_{DD} pin exceeds 25.5V, the SR controller stops switching the SR MOSFET.

Output Short Protection

When the output of power supply is shorted, the input power is limited by pulse-by-pulse current limit and the output drops to almost zero. FSR510 has output short protection which is triggered when RES pin voltage is below 0.5V longer than 50μs. When output short protection triggers, it stops switching operation.

Typical Application Circuit (QR flyback Converter with SR)

Application	Fairchild Devices	Input Voltage Range	Output
Notebook Adaptor	FSR510 FAN6300	180~265V_{AC}	19V/4.74A (90W)

Features

- High efficiency (>92% at full load)
- Low standby (Pin<0.3W at no load condition)

Key Design Notes

- The voltage scale-down ratio between RES and LPC is determined as 5.7.
- The transformer turns ration is 6.8.

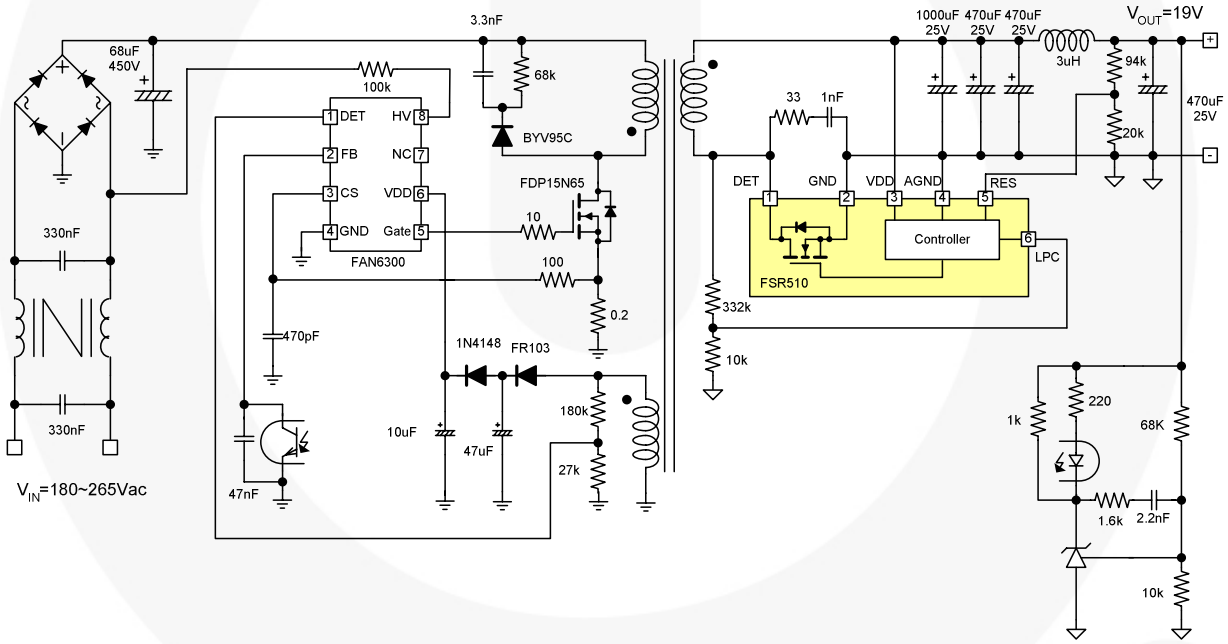


Figure 11. Application circuit

Physical Dimensions

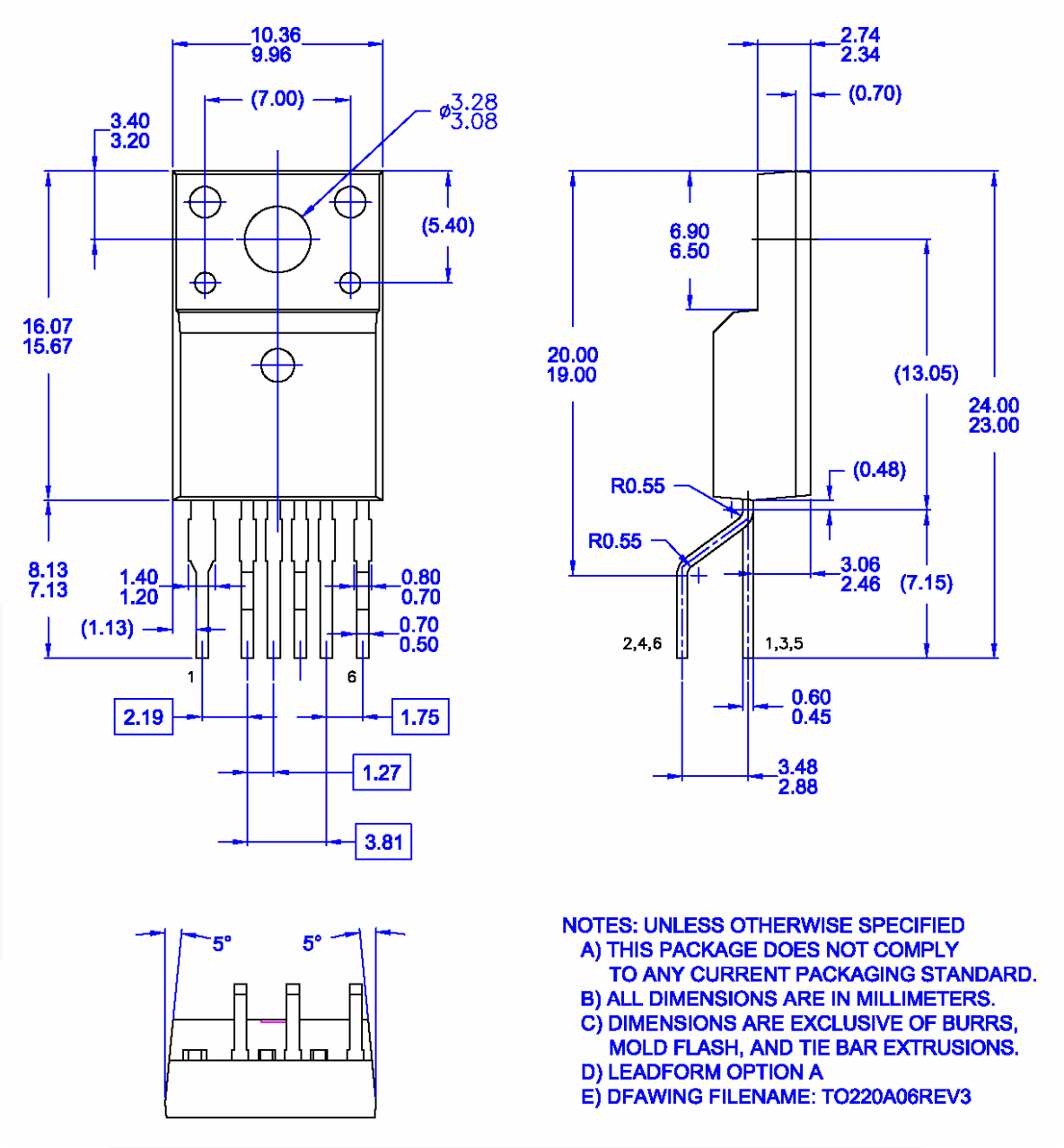


Figure 12. TO-220-6L

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SupreMOS™
SyncFET™
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TinyBoost™
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Definition of Terms

Datasheet Identification	Product Status	Definition
Advance Information	Formative / In Design	Datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	Datasheet contains preliminary data; supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.
No Identification Needed	Full Production	Datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve the design.
Obsolete	Not In Production	Datasheet contains specifications on a product that is discontinued by Fairchild Semiconductor. The datasheet is for reference information only.

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