How to achieve higher power density design by using ThinPAK 8x8

- New leadless SMD package for CoolMOS™

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- Introduction
- Package Specification
- Thermal Concept
- Application Test Conditions
- Impact on Efficiency and EMI
- Switching behaviour
- Portfolio and Target Applications
- Standardization
- Summary
Package overview
High voltage Mosfet ($V_{br}>400V$)

- DPak
- D²Pak
- I²Pak
- TO220FP
- TO220
- TO247

ThinkPAK 8x8
ThinPAK 8x8 - Introduction

What is it?
- A new leadless SMD package for HV MOSFETs
- It is very small
  - Footprint of only 64mm$^2$ (vs. 150mm$^2$ for the D2PAK)
  - Low profile with only 1mm height (vs. 4.4mm for the D2PAK)
- It has benchmark low parasitic inductances

Why is it needed?
- Fast switching HV silicon performance is increasingly limited by the parasitics of through-hole and conventional SMD packages

What benefits is the ThinPAK 8x8 package bringing?
- Provides improved performance and switching behavior (ease-of-use, EMI, reliability)
- Enables end-products with higher power density
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Package specification

- SMD package - leadless
- Height: 1 mm package height
- Footprint smaller than D2PAK (8 x 8 mm²)
- Rdson -> similar to D²PAK / TO220
- Creepage distance: 2.7 mm
- Low Parasitics (package inductivity, package resistance)
- Double sided cooling (optional)
- Soldering: wave and reflow
- Green mold compound
ThinPAK 8x8 versus D²PAK

10 x 15 x 4.4 mm³
8 x 8 x 1 mm³

60 % footprint reduction - 80% height reduction - 90% Volume reduction
Package parasitics of ThinPAK 8x8

<table>
<thead>
<tr>
<th></th>
<th>DC</th>
<th>100 MHz</th>
<th>200 MHz</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Gate</strong></td>
<td>R (mΩ)</td>
<td>64.2</td>
<td>97.9</td>
</tr>
<tr>
<td></td>
<td>L (nH)</td>
<td>4.99</td>
<td>4.26</td>
</tr>
<tr>
<td><strong>Source</strong></td>
<td>R (mΩ)</td>
<td>6</td>
<td>10.3</td>
</tr>
<tr>
<td></td>
<td>L (nH)</td>
<td>1.83</td>
<td>1.58</td>
</tr>
</tbody>
</table>

Lowest parasitic inductance available for HV-MOS

6~12nH
6nH
3.8nH
Gate driving circuit opportunity

- Separate source connection for driver
  - Negligible influence of the di/dt of the switched current
  - Driver is able to provide a constant turn-on / turn-off voltage

- Optimum performance can be achieved with
  - Pulse transformer (primary side – main converter stage)
  - Gate driving IC with separate power and signal GND
Gate driving circuit opportunity

- Pulse transformer
- Driver with separated ground

Minimizing influence of the source inductance possible
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Thermal Resistance: Comparison D²PAK vs. ThinPAK 8x8

- $R_{th}$ Junction to Ambient

![Graph showing thermal resistance vs. air velocity]

- $R_{th}$- Datasheet values

<table>
<thead>
<tr>
<th>Product</th>
<th>IPB60R199CP – D²PAK</th>
<th>IPL60R199CP – ThinPAK 8x8</th>
</tr>
</thead>
<tbody>
<tr>
<td>$R_{th-JC}$</td>
<td>0.9 K/W</td>
<td>0.9 K/W</td>
</tr>
<tr>
<td>$R_{th-JA}$</td>
<td>40 K/W</td>
<td>42 K/W</td>
</tr>
</tbody>
</table>

Device on 40mmx 40mm x 1.5mm one layer epoxy PCB FR4 with 6cm² copper area (thickness 70um) for Drain connection. PCB is vertical without air stream cooling.
Thermal measurement $R_{thja}$
Big heatspreader + different heatsink sizes

Up to 7W power handling capability in typical applications
($T_{ambient}=50^\circ C$, $T_{max}=120^\circ C$)
Thermal system

\[ R_{thjc} \approx 0.5 \text{ K/W depending on chip size} \]

\[ R_{th\_PCB} > 50 \text{ K/W} \]

\[ R_{th\_interface} \approx 1.8 \text{ K/W} \]

\[ R_{th\_j\_to\_heatsink} > 52 \text{ K/W (without heatsink)} \]

\[ R_{th\_j\_to\_heatsink} \approx 3.5 \text{ K/W (without heatsink)} \]

Use thermal vias to greatly reduce the thermal board resistance
Thermal PCB available solutions

- **2 layer PCB**
  - Thermal vias for thermal coupling to heatsink

- **Multi layer PCB**
  - Shifted thermal vias with heat spreading layer and EMI-shielding

- **PCB with Cu-inlay**
  - Cu-Inlay for high thermal conductivity
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## Application Test Conditions

<table>
<thead>
<tr>
<th>Application</th>
<th>CCM PFC</th>
</tr>
</thead>
<tbody>
<tr>
<td>Max Output Power (W)</td>
<td>300W</td>
</tr>
<tr>
<td>PFC Controller</td>
<td>ICE2PCS01G</td>
</tr>
<tr>
<td>PFC Diode</td>
<td>5A SiC</td>
</tr>
<tr>
<td>Heatsink Temperature</td>
<td>60°C</td>
</tr>
<tr>
<td>PCB</td>
<td>PFC Adapter Board_2</td>
</tr>
</tbody>
</table>
Application Test Condition

- ThinPAK 8x8 adapter PCB for PFC stage

- Gate driver IC
- Variable Rg
- MOSFET 199mOhm CP
- SiC Diode 2nd Gen 5A
- Ceramic Cap 500V 10n
- Ceramic Cap 500V 100n
- Connector array to PFC-Board
ThinPAK 8x8 vs. D²PAK
Application Test Condition
Improved commutation loop compared to TO220

Commutation loop

Big loop
2x TO220 + main PCB

Smallest loop
2x ThinPAK 8x8
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Efficiency comparison D$^2$PAK vs. ThinPAK 8x8
600V 199mOhm CP; 130kHz; 15 Ohm Rg; CCM; 60°C

**Efficiency High Line**

- Efficiency comparison D$^2$PAK vs. Thinpack_SS
- Efficiency difference High Line
- No major difference
- Similar efficiency

**Efficiency Low Line**

- Efficiency comparison D$^2$PAK vs. Thinpack_SS
- Efficiency difference Low Line
- No major difference
- Similar efficiency
EMI Measurement 200W; 15 Ohm Rg, 130kHz

D²PAK (TO263)

similar behaviour
Turn on waveform comparison
TO220 vs ThinPAK 8x8

- Lower ringing at the gate
- Smooth switching waveform
- Excellent EMI
Turn on: Waveform - Comparison

TO263 (D²PAK) vs ThinPAK 8x8

Highly reduced ringing at gate when using ThinPAK 8x8
Turn off: Waveform – Comparison

TO263 (D²PAK) vs ThinPAK 8x8

Highly reduced ringing at gate when using ThinPAK 8x8

VGs, VBulk, IChoke, VDS
Waveforms – 50ms AC line drop out

Up to -12V on $V_{GS}$
TO263 (DPAK)

Up to -1,3V on $V_{GS}$
ThinPAK 8x8

$V_{GS}$
$V_{Bulk}$
$I_{Choke}$
$V_{DS}$
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Initial Portfolio: 600V CoolMOS CP

<table>
<thead>
<tr>
<th>Part Number</th>
<th>Maximum Ratings</th>
<th>$R_{DS(ON)}$ (mOhm)</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>$V_{DSS}$ (V)</td>
<td>$I_D$ (A)</td>
</tr>
<tr>
<td>IPL60R199CP</td>
<td>600</td>
<td>16</td>
</tr>
<tr>
<td>IPL60R299CP</td>
<td>600</td>
<td>11</td>
</tr>
<tr>
<td>IPL60R385CP</td>
<td>600</td>
<td>9</td>
</tr>
</tbody>
</table>

Further portfolio extensions are in development for market introduction in H2 2010
Target applications and topologies

- Target applications:
  - Server (Computing, Telecom)
    - CCM PFC, ITTF
  - High power density applications (e.g.: UPS)
  - Ultra slim adapter
    - Quasi-resonant Fly-back
  - Lamp ballast HID applications
    - DCM PFC

- Daughter board use is a „new“ way to increase power density in compactness driven designs and target applications
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Standardization is key in today’s market

- Infineon & ST
  - Package footprint is supported by two major global power semiconductor suppliers

ThinPAK 8x8 = PowerFLAT™ 8x8 HV
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Summary of Advantages

- Leadless SMD approach enables highest power density designs
  - Small footprint (64 mm² vs. 150 mm² for D²PAK)
  - Low profile package (1.0 mm vs. 4.4 mm for D²PAK)

- Highly improved commutation loop (MOSFET, Diode, Cap)
  - Lowest stray inductances leads to lower $V_{DS}$ overshoots

- Small Drain area
  - Smaller capacitive coupling of the Drain to the heat sink compared to TO220

- Lowest $L_{source}$ (2 nH vs. 6 nH for D²PAK)
  - Separate driver source connection
  - Cleaner Waveforms, Easy to use for fast switching MOSFETs
  - Less tendency for dynamic re-turn-on or re-turn-off
  - Much easier for paralleling in high current applications
Innovative semiconductor solutions for energy efficiency, communications and security.