FAIRCHILD SEMICONDUCTOR®

September 2009

FAN6982
CCM Power Factor Correction Controller

Features

- Continuous conduction mode.
- Innovative *Switching-Charge*® multiplier-divider.
- Average-current-mode for input-current shaping.
- TriFault Detect™ prevent abnormal operation for feedback loop.
- Power on sequence control.
- Soft-start capability.
- Brownout protection.
- Cycle-by cycle Peak current limiting.
- Light load efficiency improvement.
- Fulfills class D requirements of IEC 1000-3-2.
- Programmable frequency 50kHz ~ 75 kHz.
- Wide range universal AC input voltage.
- Max duty cycle 97%.
- VDD under voltage lockout.

Applications

- Desktop PC Power Supply
- Internet Server Power Supply
- LCD TV, Monitor Power Supply
- DC Motor Power Supply
- Monitor Power Supply

Description

The FAN6982 is a 14-pin, continue conduction mode PFC controller IC intended for controlling PFC pre-regulators. The FAN6982 includes circuits for the implementation of leading edge, average current, “boost” type power factor correction and results in a power supply that fully complies with IEC1000-3-2 specification. TriFault Detect™ function help to reduce external components and provides fully protection for feedback loop such as open, short and over voltage. An over voltage comparator shuts down the PFC stage in the event of a sudden load decreasing. The RDY signal can be used for Power on sequence control. The EN function can choose to enable or disable the range function. FAN6982 also includes PFC soft start, peak current limiting and input voltage brownout protection.

Ordering Information

Part Number	Operating Temperature Range	Eco Status	Package	Packing Method
FAN6982MY	-40°C to +105°C	Green	14-pin Small Out-Line Package (SOP)	Tape & Reel

For Fairchild’s definition of Eco Status, please visit: http://www.fairchildsemi.com/company/green/rohs_green.html.

Application Diagram

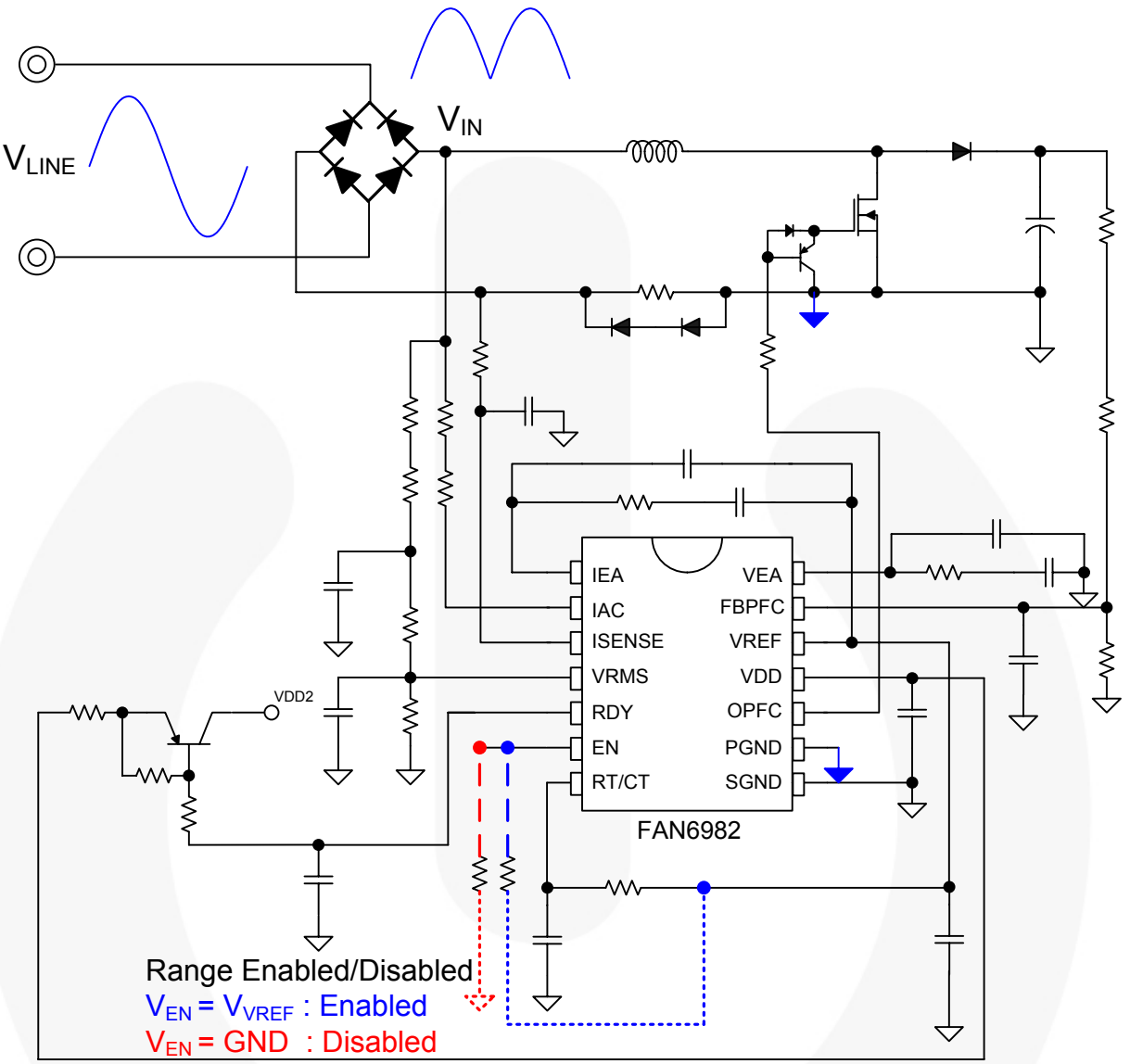


Figure 1. Typical Application

Block Diagram

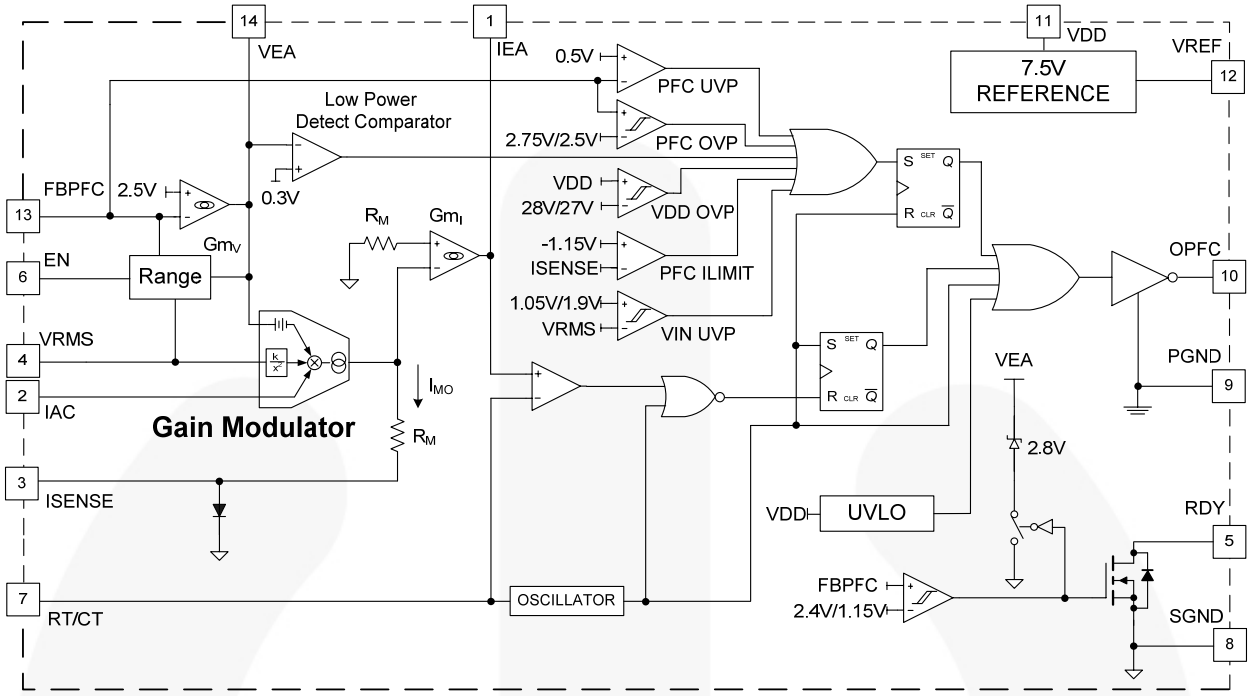
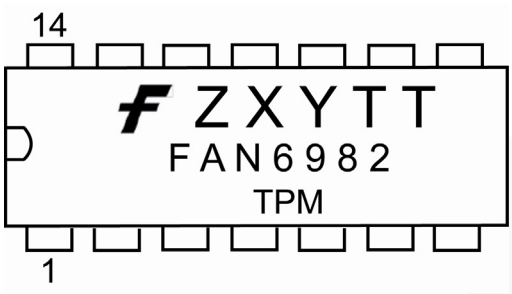


Figure 2. Function Block Diagram

Marking Information



F – Fairchild logo
Z – Plant code
X – 1 digit year code
Y – 1 digit week code
TT – 2 digits die run code
T – Package type (M: SOP)
P – Y: Green package
M – Manufacture flow code

Figure 3. Top Mark

Pin Configuration

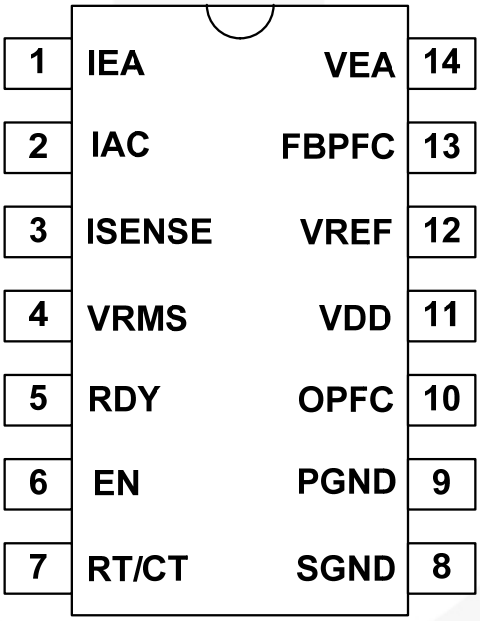


Figure 4. Pin Configuration

Pin Definitions

Pin #	Name	Description
1	IEA	**Output of Current Amplifier.** This is the output of the PFC current amplifier. The signal from this pin will be compared with saw-tooth and hence determine the pulse width for PFC gate drive.
2	IAC	**Input AC Current.** For normal operation, this input is used to provide current reference for the multiplier. The suggested maximum IAC is 100uA.
3	ISENSE	**Current Sense.** The non-inverting input of the PFC current amplifier and also the output of multiplier and PFC ILIMIT comparator.
4	VRMS	**Line-Voltage Detection.** Line voltage detection. The pin is used for PFC multiplier
5	RDY	**Ready Signal.** This pin controls the power on sequence. Once the FAN6982 is turned on and the FBPFC voltage exceeds in 2.4V the RDY pin will pull low impedance. The FBPFC voltage lower than 1.15V the RDY pin will pull high impedance.
6	EN	**Enable Range Function.** The Range function is enabled, when EN is connected to VREF; The Range function is disabled, when EN is connected to GND.
7	RT/CT	**Oscillator RC Timing Connection.** Oscillator timing node; timing set by RT and CT.
8	SGND	**Signal Ground.**
9	PGND	**Power Ground.**
10	OPFC	**Gate Drive.** The totem pole output drive for PFC MOSFET. This pin is internally clamped under 15V to protect the MOSFET.
11	VDD	**Supply.** The power supply pin. The threshold voltages for start-up and turn-off are 11V and 9.3V, respectively. The operating current is lower than 10mA.
12	VREF	**Reference Voltage.** Buffered output for the internal 7.5V reference.
13	FBPFC	**Voltage Feedback Input.** The feedback input for PFC voltage loop. The inverting input of PFC error amp. This pin is connected to the PFC output through a divider network.
14	VEA	**Output of Voltage Amplifier.** The error-amp output for PFC voltage feedback loop. A compensation network is connected between this pin and ground.

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter	Min.	Max.	Unit
V_{DD}	DC Supply Voltage		30	V
V_H	OPFC, RDY, EN, VREF	-0.3	30	V
V_L	IAC, VRMS, RT/CT, FBPFC, VEA	-0.3	7	V
V_{IEA}	IEA	0	V_{VREF}+0.3	V
V_N	ISENSE	-5	0.7	V
I_{AC}	Input AC Current		1	mA
I_{REF}	VREF Output Current		5	mA
$I_{PFC-OUT}$	Peak PFC OUT Current, Source or Sink		0.5	A
P_D	Power Dissipation T_A < 50°C		800	mW
$R_{\Theta j-a}$	Thermal Resistance (Junction to Air)		104.10	°C/W
$R_{\Theta j-c}$	Thermal Resistance (Junction to Case)		40.61	°C/W
T_J	Operating Junction Temperature	-40	125	°C
T_{STG}	Storage Temperature Range	-55	150	°C
T_L	Lead Temperature(Soldering)		260	°C
ESD	ESD Capability, HBM Model		4.5	kV
	ESD Capability, CDM Model		1000	V

Notes:
1. All voltage values, except differential voltage, are given with respect to GND pin.
2. Stresses beyond those listed under “absolute maximum ratings “may cause permanent damage to the device.

Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to Absolute Maximum Ratings.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
T_A	Operating Ambient Temperature		-40		+105	°C

Electrical Characteristics

V_{DD}=15V, T_A= 25°C, T_A = T_J, R_T = 27kΩ, C_T = 1000pF unless noted operating specs.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
VDD Section						
V_{DD-OP}	Continuously Operating Voltage				22	V
$I_{DD\ ST}$	Start-Up Current	V_{DD}=V_{TH-ON}-0.1V; OPFC open		30	80	uA
I_{DD-OP}	Operating Current	V_{DD}=13V; OPFC open	2	2.3	3	mA
V_{TH-ON}	Turn-on Threshold Voltage		10	11	12	V
$\triangle V_{TH}$	Hysteresis		1.35		1.9	V
V_{DD-OVP}	VDD OVP		27	28	29	V
$\triangle V_{DD-OVP}$	VDD OVP Hysteresis			1		V
Oscillator						
F_{OSC}	PFC Frequency	R_T=27kΩ, C_T=1000pF	60	64	67	kHz
F_{DV}(3)	Voltage Stability	11V ≦ V_{DD} ≦ 22V			2	%
F_{DT}(3)	Temperature Stability	-40°C ~ +105°C			2	%
F_{TV}	Total Variation	Line, Temp	58		70	kHz
F_{RV}	Ramp Voltage	Valley to Peak		2.8		V
$I_{OSC-DIS}$	Discharge Current	V_{RAMP}=0V, $V_{RT/CT}$=2.5V	6.5		15	mA
F_{RANGE}	Frequency Range		50		75	kHz
$t_{PFC-DEAD}$	PFC Dead Time	R_T=27kΩ, C_T=1000pF	400	600	800	nS
VREF						
V_{VREF}	Reference voltage	I_{REF}=0mA, C_{REF}=0.1uF	7.4	7.5	7.6	V
$\triangle V_{VREF1}$	Load regulation of reference voltage	C_{REF}=0.1uF, I_{REF}=0mA to 3.5mA V_{VDD}=14V, Rise/Fall Time > 20us		30	50	mV
$\triangle V_{VREF2}$	Line regulation of reference voltage	C_{REF}=0.1uF, V_{VDD}=11V to 22V			25	mV
$\triangle V_{VREF-DT}$(3)	Temperature Stability	-40°C ~ +105°C		0.4	0.5	%
$\triangle V_{VREF-TV}$(3)	Total Variation	Line, Load, Temp	7.35		7.65	V
$\triangle V_{VREF-LS}$(3)	Long term Stability	T_J = 125°C, 0 ~ 1000HRs	5		25	mV
$I_{REF-MAX}$.	Max. Current	V_{VREF} > 7.35V	5			mA
Brown Out						
$V_{RMS-UVL}$	VRMS Threshold Low	When V_{RMS}=1.05V @75Vrms	1.00	1.05	1.10	V
$V_{RMS-UVH}$	VRMS Threshold High	When V_{RMS}=1.9V @85*1.414	1.85	1.9	1.95	V
$\triangle V_{RMS-UVP}$	Hysteresis		750	850	950	mV
t_{UVP}	Under voltage protection de-bounce time		340	410	480	ms
RDY Section						
$V_{FBPFC-RD}$	FBPFC Voltage level to Pull low impedance with RDY pin.		2.3	2.4	2.5	V
$\triangle V_{FBPFC-RD}$	Hysteresis		1.15	1.25	1.35	V
$I_{RDY-LEK}$	The leakage current of RDY while it is high impedance	V_{FBPFC}<2.4V			500	nA
V_{RDY-L}	RDY Low Voltage	I_{SINK}=2mA			0.5	V

Electrical Characteristics

V_{DD}=15V, T_A= 25°C, $T_A = T_J$, R_T = 27kΩ, C_T = 1000pF unless noted operating specs.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
Voltage Error Amplifier						
V_{REF}	Reference Voltage		2.45	2.5	2.55	V
A_V (3)	Open-loop Gain	at T_A = 25°C	35	42		dB
Gm_V	Transconductance	$V_{NONINV}=V_{INV}$, V_{VEA}=3.75V at T=25°C	50	70	90	umho
$I_{FBPFC-L}$.	Maximum Source Current	V_{FBPFC}=2V, V_{VEA}=1.5V	40	50		uA
$I_{FBPFC-H}$.	Maximum Sink Current	V_{FBPFC}=3V, V_{VEA}=6V		-50	-40	uA
I_{BS}	Input Bias Current		-1		1	uA
V_{VEA-H}	Output High Voltage on V_{VEA}		5.8	6		V
V_{VEA-L}	Output Low Voltage on V_{VEA}			0.1	0.4	V
Current Error Amplifier						
V_{ISENSE}	Input Voltage Range		-1.5		0.7	V
A_I (3)	Open loop Gain	at T_A = 25°C	40	50		dB
Gm_I	Transconductance	$V_{NONINV}=V_{INV}$, V_{IEA} = 3.75V	75	88	100	umho
V_{OFFSET}	Input offset voltage	V_{VEA}=0V, IAC Open	-10		10	mV
V_{IEA-H}	Output High Voltage		6.8	7.4	8.0	V
V_{IEA-L}	Output Low Voltage			0.1	0.4	V
I_L	Source Current	V_{ISENSE}= -0.6V, V_{IEA}=1.5V	35	50		uA
I_H	Sink Current	V_{ISENSE}= +0.6V, V_{IEA}=4.0V		-50	-35	uA
PFC OVP Comparator						
$V_{FBPFC-OVP}$	Over voltage protection		2.7	2.75	2.8	V
$\triangle V_{FBPFC-OVP}$	PFC OVP Hysteresis		200	250	300	mV
Low-Power Detect Comparator						
$V_{VEA-OFF}$	VEA Voltage OFF OPFC		0.2	0.3	0.4	V
PFC Soft Start						
V_{VEA_CLAMP}	PFC Soft Start	V_{FBPFC} < 2.4V	2.2	2.8	3.3	V
EN Section						
V_{EN-H}	High Voltage level of V_{EN}	$V_{EN}=V_{VREF}$	7.4	7.5	7.6	V
V_{EN-L}	Low Voltage level of V_{EN}	V_{EN}=GND		0		V
Range						
V_{VRMS-L}	RMS AC Voltage Low	When V_{VRMS} =1.95V @132Vrms	1.9	1.95	2	V
V_{VRMS-H}	RMS AC Voltage High	When V_{VRMS} =2.45V @150Vrms	2.4	2.45	2.5	V
V_{VEA-L}	VEA Low	When V_{VEA}= 1.95V @ 30% Loading	1.9	1.95	2	V
V_{VEA-H}	VEA High	When V_{VEA}= 2.45V @ 40% Loading	2.4	2.45	2.5	V
I_{TC}	Source Current from FBPFC		18	20	22	uA

Electrical Characteristics

V_{DD}=15V, T_A= 25°C, T_A = T_J, R_T = 27kΩ, C_T = 1000pF unless noted operating specs.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
Gain Modulator						
I_{AC}	Input for AC Current	Multiplier linear range	0		100	uA
GAIN[3][4]	GAIN Modulator	I_{IAC} = 17.67uA, V_{VRMS} = 1.080V V_{FBPFC} = 2.25V, at T_A = 25°C	7.500	9.000	10.50	
		I_{IAC} = 20uA, V_{VRMS} = 1.224V V_{FBPFC} = 2.25V, at T_A = 25°C	6.367	7.004	7.704	
		I_{IAC} = 25.69uA, V_{VRMS} = 1.585V V_{FBPFC} = 2.25V, at T_A = 25°C	3.801	4.182	4.600	
		I_{IAC} = 51.62uA, V_{VRMS} = 3.169V V_{FBPFC} = 2.25V, at T_A = 25°C	0.950	1.045	1.149	
		I_{IAC} = 62.23uA, V_{VRMS} = 3.803V V_{FBPFC} = 2.25V, at T_A = 25°C	0.660	0.726	0.798	
BW	Bandwidth	I_{IAC} = 40uA		2		KHz
$V_{O(GM)}$	Output Voltage=5.7kΩ × (I_{SENSE}-I_{OFFSET})	I_{AC}=20μA, V_{RMS}=1.224V V_{FBPFC}=2.25V, at T_A = 25°C	0.710	0.798	0.885	V
PFC ILIMIT Comparator						
$V_{PFC-ILIMIT}$	Peak Current Limit Threshold Voltage Cycle-by-Cycle Limit		-1.25	-1.15	-1.05	V
$\triangle V_{pk}$	PFC ILIMIT-Gain Modulator Output	I_{IAC} = 17.67uA, V_{VRMS} = 1.08V V_{FBPFC} = 2.25V, at T_A = 25°C	200			mV
PFC Output Driver						
$V_{GATE-CLAMP}$	Gate Output Clamping Voltage	V_{DD}=22V	13	15	17	V
V_{GATE-L}	Gate Low Voltage	V_{DD}=15V; I_O = 100mA			1.5	V
V_{GATE-H}	Gate High Voltage	V_{DD}=13V; I_O = 100mA	8			V
t_R	Gate Rising Time	V_{DD}=15V; C_L=4.7nF; O/P= 2V to 9V	40	70	120	nS
t_F	Gate Falling Time	V_{DD}=15V; C_L=4.7nF; O/P= 9V to 2V	40	60	110	nS
$D_{PFC-MAX}$	Maximum Duty Cycle	V_{IEA}<1.2V	94	97		%
$D_{PFC-MIN}$	Minimum Duty Cycle	V_{IEA}>4.5V			0	%
Tri-Fault Detect						
t_{FBPFC_OPEN}	Time to FBPFC Open	V_{FBPFC} = $V_{FBPFC-OVP}$ to FBPFC OPEN, 470pF from FBPFC to GND.		2	4	mS
$V_{PFC-UVP}$	PFC Feedback Under Voltage Protection		0.4	0.5	0.6	V

Notes:

3. This parameter, although guaranteed by design, is not 100% production tested.
4. This Gain is the maximum gain of modulation with a given VRMS voltage when VEA is saturated to high.

Typical Performance Characteristics

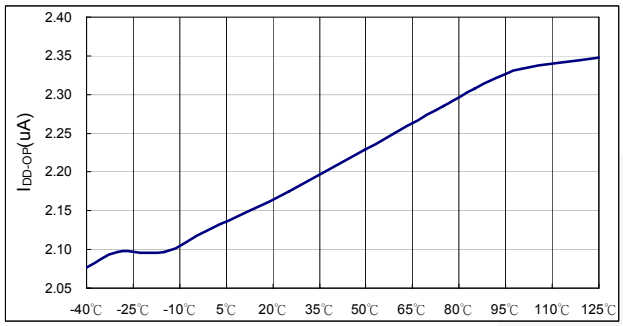


Figure 5. I_{DD-OP} vs. Temperature

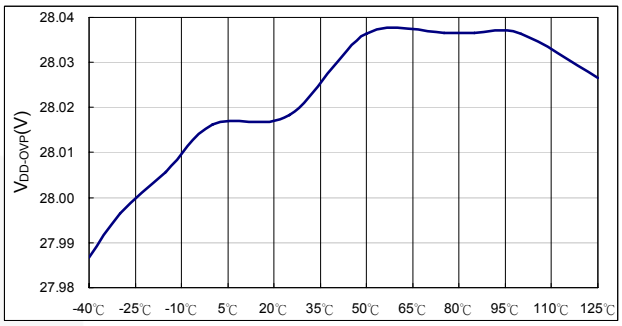


Figure 6. V_{DD-OVP} vs. Temperature

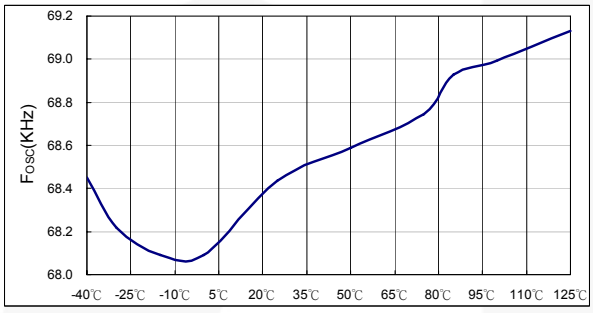


Figure 7. F_{OSC} vs. Temperature

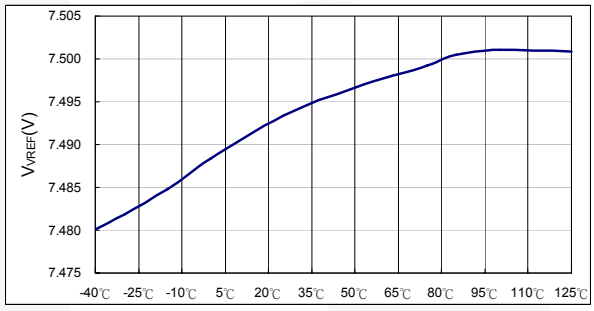


Figure 8. V_{VREF} vs. Temperature

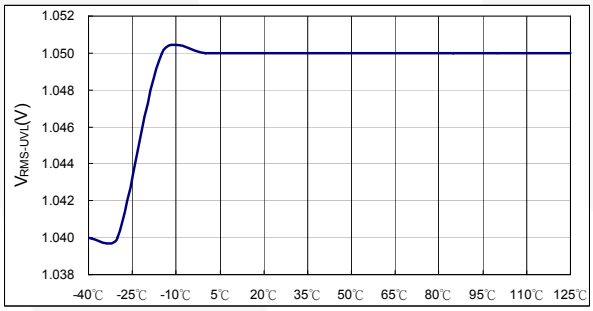


Figure 9. $V_{RMS-UVL}$ vs. Temperature

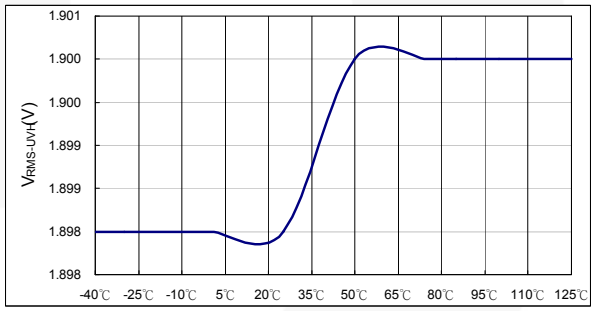


Figure 10. $V_{RMS-UVH}$ vs. Temperature

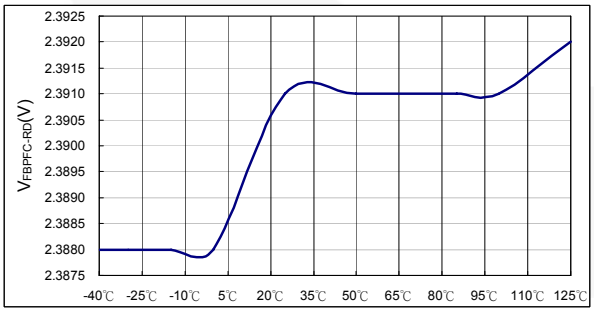


Figure 11. $V_{FBPFC-RD}$ vs. Temperature

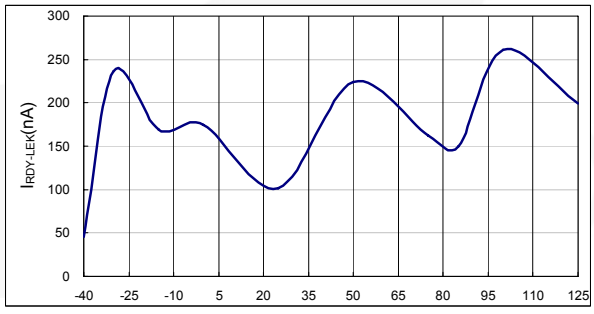


Figure 12. $I_{RDY-LEK}$ vs. Temperature

Typical Performance Characteristics

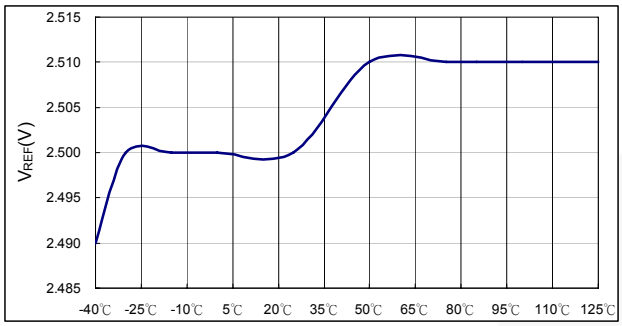


Figure 13. V_{REF} vs. Temperature

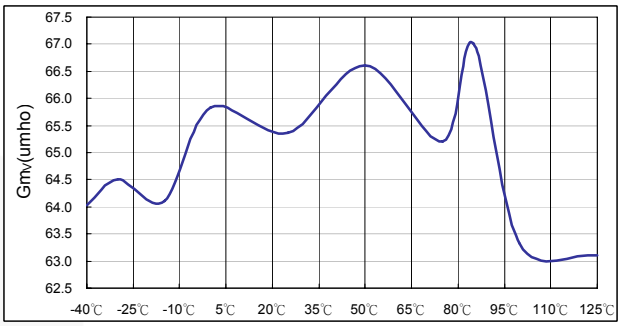


Figure 14. Gm_V vs. Temperature

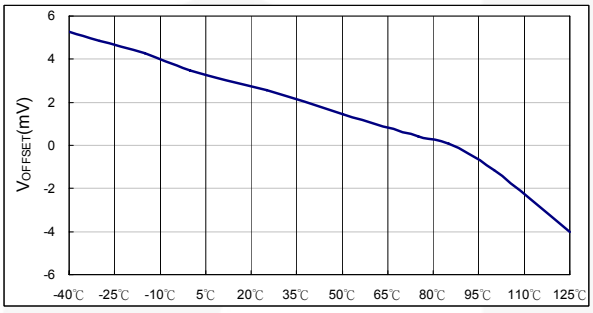


Figure 15. V_{OFFSET} vs. Temperature

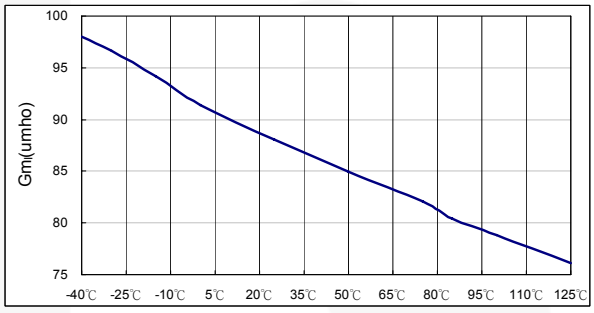


Figure 16. Gm_I vs. Temperature

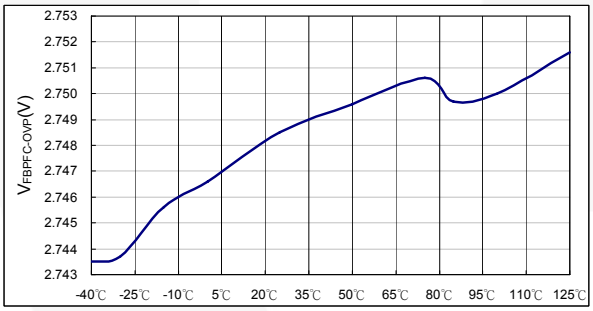


Figure 17. $V_{FBPFC-OVP}$ vs. Temperature

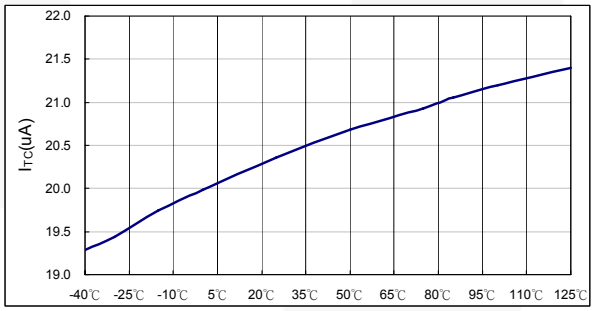


Figure 18. I_{TC} vs. Temperature

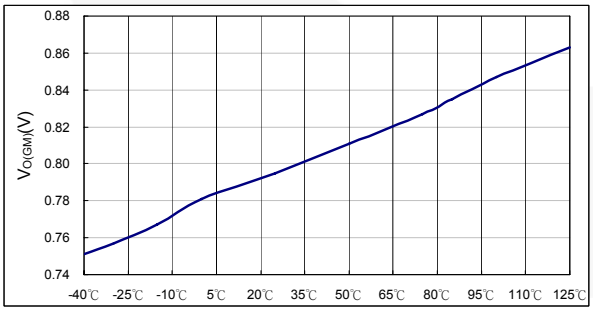


Figure 19. $V_{O(GM)}$ vs. Temperature

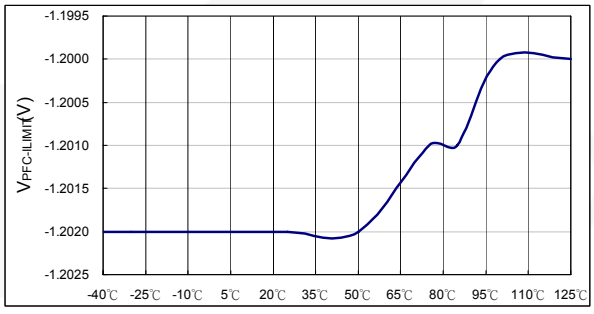


Figure 20. $V_{PFC-ILIMIT}$ vs. Temperature

Typical Performance Characteristics

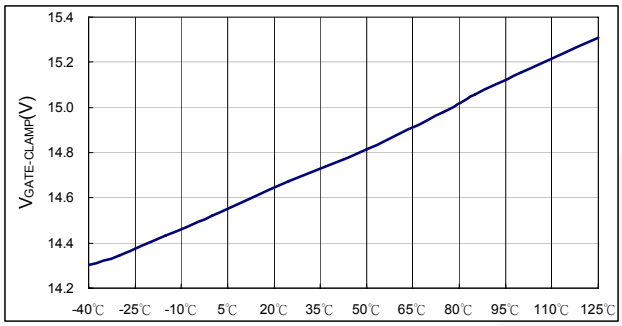


Figure 21. $V_{GATE-CLAMP}$ vs. Temperature

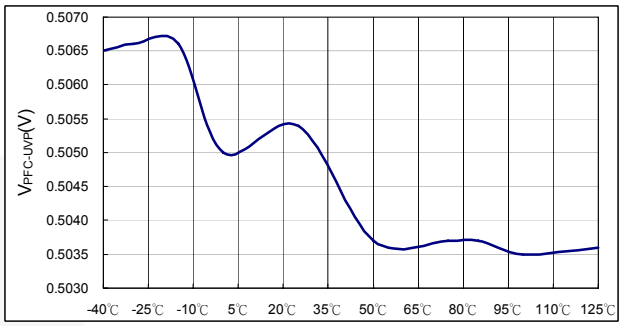


Figure 22. $V_{PFC-UVP}$ vs. Temperature

Functional Description

Oscillator

The internal oscillator frequency of FAN6982 is determined by the timing resistor and capacitor on RT/CT pin. The frequency of the internal oscillator is given by

$$f_{OSC} = \frac{1}{0.56 \cdot R_T \cdot C_T + 360 C_T} \quad (1)$$

The dead time for the PFC gate drive signal is determined by

$$t_{DEAD} = 360 C_T \quad (2)$$

The dead time should be smaller than 2% of switching period to minimize line current distortion around line zero crossing.

Gain Modulator

Gain modulator is the key block for PFC stage since it provides the reference to the current control error amplifier for the input current shaping as shown in Figure 23. The output current of gain modulator is a function of V_{EA}, I_{AC} and V_{RMS}. The gain of the gain modulator is given in the datasheet as a ratio between I_{MO} and I_{AC} with a given V_{RMS} when V_{EA} is saturated to high. The gain is inversely proportional to V_{RMS}^2 as shown in Figure 24 to implement line feed-forward. This automatically adjusts the reference of current control error amplifier according to the line voltage such that the input power of PFC converter is not changed with line voltage as shown in Figure 25.

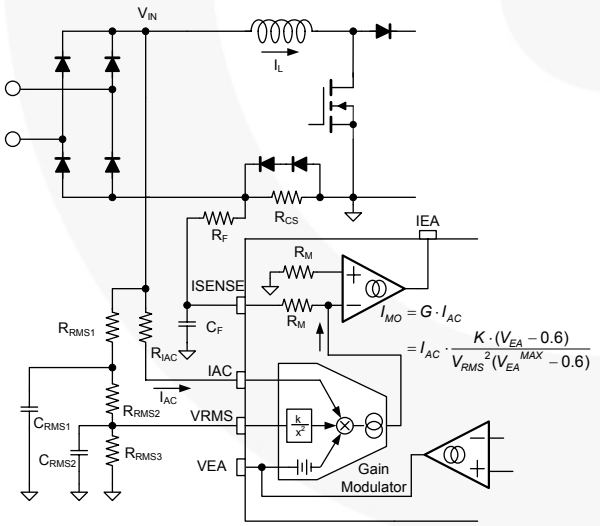


Figure 23. Gain Modulator Block

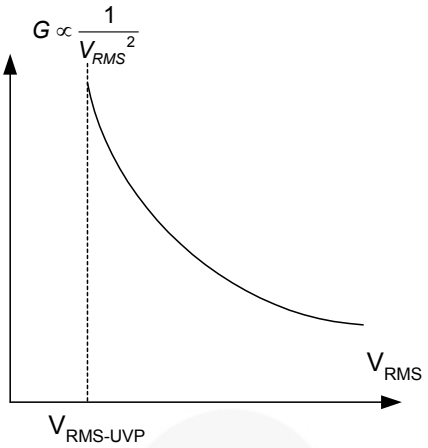


Figure 24. Modulation Gain Characteristics

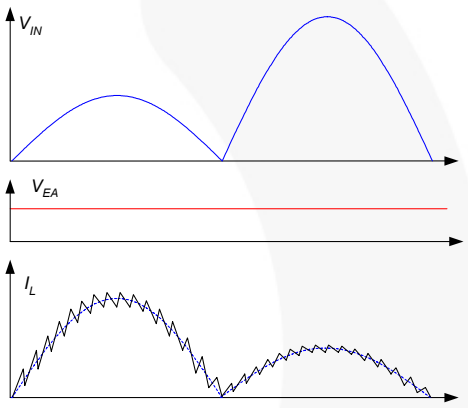


Figure 25. Line Feed-forward operation

To sense RMS value of the line voltage, averaging circuit with two poles is typically employed as shown in Figure 23. It should be noticed that the input voltage of PFC is clamped at the peak of the line voltage once PFC stops switching since the junction capacitance of bridge diode is not discharged as shown in Figure 26.

Therefore, the voltage divider for VRMS should be designed considering the brown-out protection trip point and minimum operation line voltage.

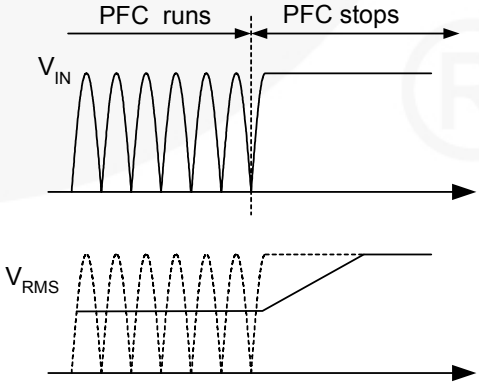


Figure 26. V_{RMS} according to the PFC operation

The rectified sinusoidal signal is obtained by the current flowing into the IAC pin. The resistor R_{IAC} should be large enough to prevent saturation of the gain modulator as

$$\frac{\sqrt{2}V_{LINE.BO}}{R_{IAC}} \cdot G^{MAX} < 159\mu A \quad (3)$$

Where $V_{LINE.BO}$ is the line voltage that trips brown-out protection, G^{MAX} is the maximum modulator gain when V_{RMS} is 1.08V, which can be found in the datasheet and 159uA is the maximum output current of the gain modulator.

Current control of Boost stage

The FAN6982 employs two control loops for power factor correction as shown in Figure 27: a current control loop and a voltage control loop. The current control loop shapes inductor current as shown in Figure 28 based on the reference signal obtained at IAC pin as

$$I_L \cdot R_{CS1} = I_{MO} \cdot R_M = I_{AC} \cdot G \cdot R_M \quad (4)$$

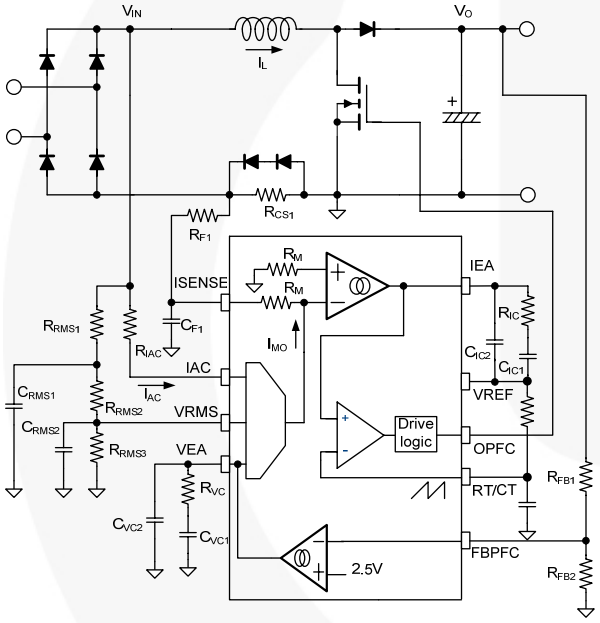


Figure 27. Gain Modulation Block

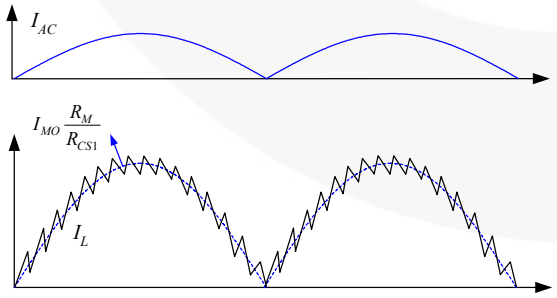


Figure 28. Inductor current shaping

The current control feedback loop also has a pulse-by-pulse current limit comparator that forces the PFC switch to turn off if the ISENSE pin voltage drops below -1.15V until the next switching cycle.

Voltage Control of Boost stage

The voltage control loop regulates PFC output voltage using internal error amplifier such that the FBPFC voltage is same as internal reference of 2.5V.

To improve system efficiency at low AC line voltage and light load condition, FAN6982 provides two-level PFC output voltage. As shown in Figure 29, FAN6982 monitors VEA and VRMS voltages to adjust the PFC output voltage. When VEA and VRMS are lower than thresholds, internal current source of 20uA is enabled which flows through R_{FB2} increasing the voltage of FBPFC pin. This causes the PFC output voltage to reduce when 20uA is enabled as

$$V_{OPFC2} = \frac{R_{FB1} + R_{FB2}}{R_{FB2}} \times (2.5 - 20\mu A \times R_{FB2}) \quad (5)$$

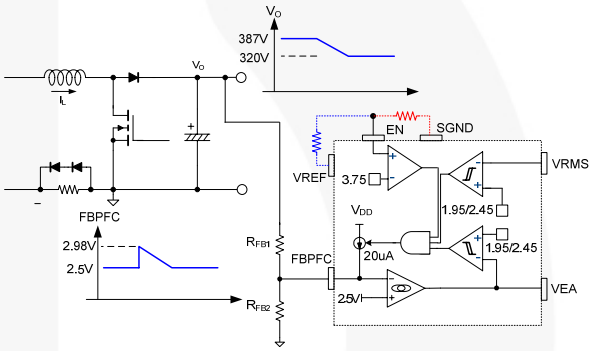


Figure 29. Block of two level PFC output

Brownout Protection

FAN6982 has a built-in internal brownout protection comparator monitoring voltage of VRMS pin. Once VRMS pin voltage is lower than 1.05V, the PFC stage is shutdown to protect the system from over current. FAN6982 starts up the boost stage once VRMS voltage increases above 1.9V.

TriFault Detect™

To improve power supply reliability, reduce system component count, and simplify compliance to UL 1950 safety standards, the FAN6982 includes TriFault Detect. This feature monitors FBPFC for certain PFC fault conditions.

In the case of a feedback path failure, the output of the PFC could go out of safe operating limits. With such a failure, FBPFC will go outside of its normal operating area. Should FBPFC go too low, too high, or open, TriFault Detect senses the error and terminates the PFC output drive.

TriFault detect is an entirely internal circuit. It requires no external components to serve its protective function.

PFC Soft Start Function

The FAN6982 has PFC Soft Start function as shown in Figure 30. In PFC soft start function, when bulk voltage under the 96% of setting voltage, V_{EA} will clamps to 2.8V, the output current of multiplier will cut half, the rectifier line current will be limited by current loop, the PFC output rise time will increase.

When bulk voltage over the 96%, the clamping function will be disabled, then the bulk voltage can be regulated by voltage error amplifier.

There have two advantages with PFC soft start: one is the MOSFET experiences current will reduce, that can obtain more de-rating with MOSFET current level.

The other is reduce the PFC OVP at bulk voltage reach the setting voltage, because the charge current becomes small, the bulk voltage can not exceed to setting voltage easily.

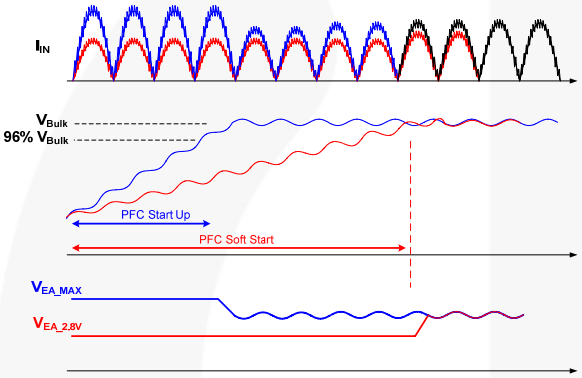


Figure 30. PFC Soft Start

RDY Function

The FAN6982 has RDY function as shown in Figure 31. The RDY function is controlled by voltage of FBPFC, if the voltage of FBPFC is over than 96% of 2.5V, the RDY PIN will be connected to SGND, if the FBPFC is under the 46% of 2.5V and the RDY will appear “open drain situation”. Usually the capacitor is parallel with the RDY pin to prevent the layout noise.

We can use the PNP transistor to control the AHB LLC or Dual-forward controller on the same side or use the “op-to” to control the LLC controller on the other side.

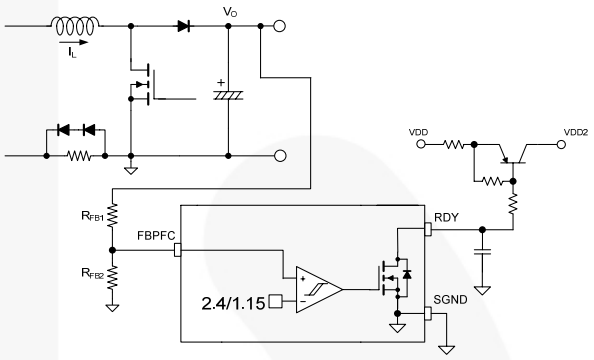


Figure 31. RDY Application Circuit

Physical Dimensions (Continued)

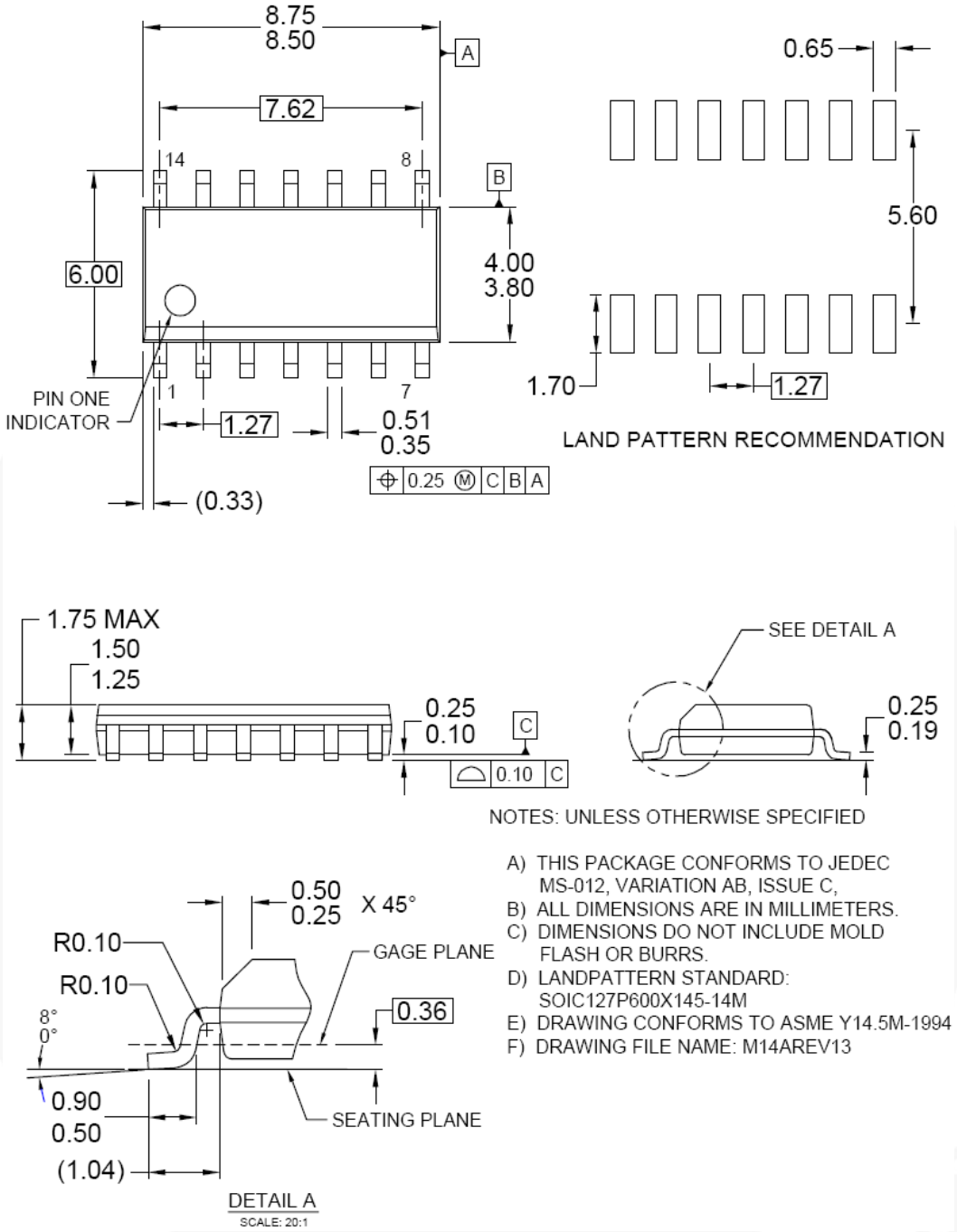


Figure 32. 14-Pin Small Outline Package (SOIC)

Package drawings are provided as a service to customers considering Fairchild components. Drawings may change in any manner without notice. Please note the revision and/or date on the drawing and contact a Fairchild Semiconductor representative to verify or obtain the most recent revision. Package specifications do not expand the terms of Fairchild's worldwide terms and conditions, specifically the warranty therein, which covers Fairchild products.

Always visit Fairchild Semiconductor's online packaging area for the most recent package drawings:
http://www.fairchildsemi.com/packaging/

FAIRCHILD SEMICONDUCTOR®

TRADEMARKS

The following includes registered and unregistered trademarks and service marks, owned by Fairchild Semiconductor and/or its global subsidiaries, and is not intended to be an exhaustive list of all such trademarks.

AccuPower™
Auto-SPM™
Build it Now™
CorePLUS™
CorePOWER™
CROSSVOLT™
CTL™
Current Transfer Logic™
EcoSPARK®
EfficientMax™
EZSWITCH™*
EZ™*
F®
Fairchild®
Fairchild Semiconductor®
FACT Quiet Series™
FACT®
FAST®
FastvCore™
FETBench™
FlashWriter®*
FPS™
F-PFS™
FRFET®
Global Power Resource℠
Green FPS™
Green FPS™ e-Series™
Gmax™
GTO™
IntelliMAX™
ISOPLANAR™
MegaBuck™
MICROCOUPLER™
MicroFET™
MicroPak™
MillerDrive™
MotionMax™
Motion-SPM™
OPTOLOGIC®
OPTOPLANAR®
®
PDP SPM™
Power-SPM™
PowerTrench®
PowerXS™
Programmable Active Droop™
QFET®
QS™
Quiet Series™
RapidConfigure™
™
Saving our world, 1mW/W/kW at a time™
SignalWise™
SmartMax™
SMART START™
SPM®
STEALTH™
SuperFET™
SuperSOT™-3
SuperSOT™-6
SuperSOT™-8
SupreMOS™
SyncFET™
Sync-Lock™
SYSTEM ®* GENERAL
The Power Franchise®
the power franchise
TinyBoost™
TinyBuck™
TinyCalc™
TinyLogic®
TINYOPTO™
TinyPower™
TinyPWM™
TinyWire™
TriFault Detect™
TRUECURRENT™*
µSerDes™
SerDes
UHC®
Ultra FRFET™
UniFET™
VCX™
VisualMax™
XS™

* Trademarks of System General Corporation, used under license by Fairchild Semiconductor.

DISCLAIMER

FAIRCHILD SEMICONDUCTOR RESERVES THE RIGHT TO MAKE CHANGES WITHOUT FURTHER NOTICE TO ANY PRODUCTS HEREIN TO IMPROVE RELIABILITY, FUNCTION, OR DESIGN. FAIRCHILD DOES NOT ASSUME ANY LIABILITY ARISING OUT OF THE APPLICATION OR USE OF ANY PRODUCT OR CIRCUIT DESCRIBED HEREIN; NEITHER DOES IT CONVEY ANY LICENSE UNDER ITS PATENT RIGHTS, NOR THE RIGHTS OF OTHERS. THESE SPECIFICATIONS DO NOT EXPAND THE TERMS OF FAIRCHILD'S WORLDWIDE TERMS AND CONDITIONS, SPECIFICALLY THE WARRANTY THEREIN, WHICH COVERS THESE PRODUCTS.

LIFE SUPPORT POLICY

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF FAIRCHILD SEMICONDUCTOR CORPORATION.

As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury of the user.
2. A critical component in any component of a life support, device, or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

ANTI-COUNTERFEITING POLICY

Fairchild Semiconductor Corporation's Anti-Counterfeiting Policy. Fairchild's Anti-Counterfeiting Policy is also stated on our external website, www.fairchildsemi.com, under Sales Support.

Counterfeiting of semiconductor parts is a growing problem in the industry. All manufacturers of semiconductor products are experiencing counterfeiting of their parts. Customers who inadvertently purchase counterfeit parts experience many problems such as loss of brand reputation, substandard performance, failed applications, and increased cost of production and manufacturing delays. Fairchild is taking strong measures to protect ourselves and our customers from the proliferation of counterfeit parts. Fairchild strongly encourages customers to purchase Fairchild parts either directly from Fairchild or from Authorized Fairchild Distributors who are listed by country on our web page cited above. Products customers buy either from Fairchild directly or from Authorized Fairchild Distributors are genuine parts, have full traceability, meet Fairchild's quality standards for handling and storage and provide access to Fairchild's full range of up-to-date technical and product information. Fairchild and our Authorized Distributors will stand behind all warranties and will appropriately address any warranty issues that may arise. Fairchild will not provide any warranty coverage or other assistance for parts bought from Unauthorized Sources. Fairchild is committed to combat this global problem and encourage our customers to do their part in stopping this practice by buying direct or from authorized distributors.

PRODUCT STATUS DEFINITIONS

Definition of Terms

Datasheet Identification	Product Status	Definition
Advance Information	Formative / In Design	Datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	Datasheet contains preliminary data; supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.
No Identification Needed	Full Production	Datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve the design.
Obsolete	Not In Production	Datasheet contains specifications on a product that is discontinued by Fairchild Semiconductor. The datasheet is for reference information only.

Rev. I42