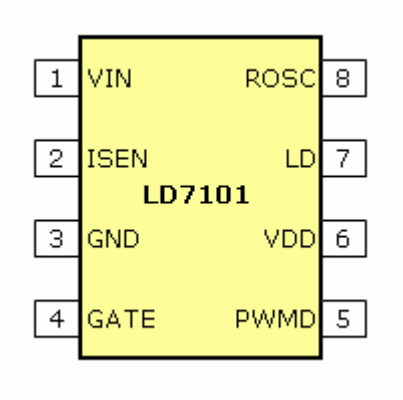
Features

- Wide input voltage range : 8V to 450V
- Efficiency : >90%
- Regulated current drives LED from 1 to 100 of LEDs in series or parallel combinations
- Linear or PWM brightness control
- Resistor programmable oscillator frequency
- SOIC-8 RoHS compliant package

Applications

- TFT flat panel backlighting
- AC/DC LED lamp
- LED traffic light
- T5, T8 LED line bar
- MR-16 lamp
- Signage or decorative LED lamp

Package Pin Out



General Description

The LD7101 is a low cost and high-efficiency off-line LED driver. Built-in high voltage regulator enables the LD7101 operating from 8V to 450Vdc with very few external components. The LD7101 maintains a constant current, rather than constant voltage, for LED to provide a constant brightness.

The LD7101 drives an external power MOSFET at a fixed frequency up to 300KHz from GATE pin. The frequency can be adjusted by an external resistor connected to the ROSC pin.

Dimming the LED string is controlled by adjusting the duty cycle of the PWMD pin which accepts an external PWM signal with a duty ratio from 0% ~100% and a frequency up to a few kilo Hz; or, it can be applied a linear voltage from 0 to 250mV to the LD pin.

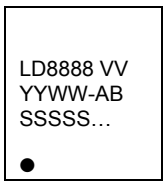
Ordering Information

		Packing Options	
Part No.	Package	Tube (TU)	Tape & Reel (TR)
LD7101	SOP-8(S1)	LD7101S1-TU	LD7101S1-TR

- Package material default is “Green” package.

Product Marking

For SOP-8 (S1)



- Line 1: “LD” is a fixed character
  8888: product name
  VV: Voltage
- Line 2: YYWW: year and week no.
  A: package material code
  B: the brevity code of assembly house
- Line 3: SSSSS…: lot no.

Absolute Maximum Ratings

Parameter	Maximum	Unit
V_{IN} to GND	-0.5 to +450	V
ISEN, GATE, PWMD, LD, ROSC to GND	-0.3 to VDD+0.3	V
V_{DD} to GND	+15	V
Operating Junction Temperature	-40 to +125	°C
Storage Temperature	-65 to +150	°C

The values beyond the boundaries of absolute maximum rating may cause the damage to the device. Functional operation in this context is not implied. Continuous use of the device at the absolute rating level might influence device reliability. All voltages have their reference to device ground.

Electrical Characteristics

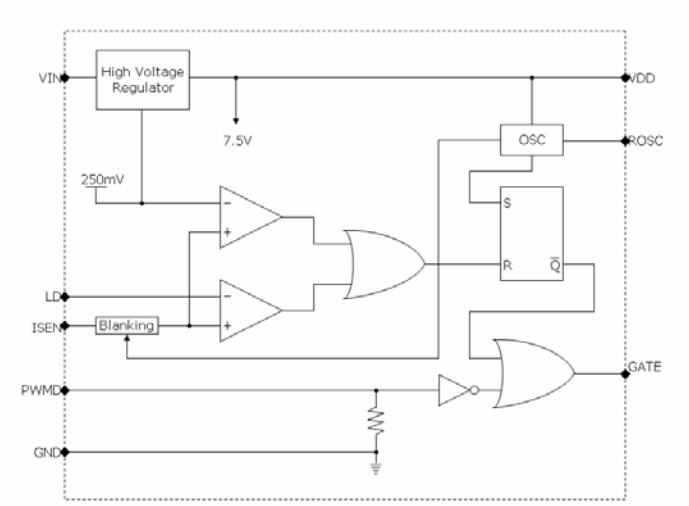
VIN=24V, T_A=25°C unless specified, otherwise minimum and maximum values are guaranteed by production testing requirements.

Parameter	Symbol	Condition	Min	Typ.	Max	Unit
Input						
Input DC Voltage Range	V_{INDC}	DC input voltage	8	–	450	V
Chip Shut-Down current	I_{INSD}	PWMD to GND, VIN = 8~450V	–	0.5	1.0	mA
Regulator						
Internal Voltage Regulator	V_{DD}	V_{IN} = 8~450V, 500pF at GATE, Rosc = 220KΩ	7.25	7.5	7.75	V
V_{DD} line resulation	$V_{DD, line}$	V_{IN} = 8~450V, 500pF at GATE, Rosc = 220KΩ	0	–	1.0	V
V_{DD} load regulation	$V_{DD, load}$	$I_{DD(ext)}$ = 0~1mA, 500pF at GATE, Rosc = 220KΩ	–100	–	100	mV
V_{DD} under voltage lockout threshold	UVLO	V_{DD} rising	6.2	6.5	7.2	mV
V_{DD} under voltage lockout hysteresis	ΔUVLO	V_{DD} = 8~450V, $I_{DD(ext)}$ = 1mA	–	500	–	mV
PWMD (Digital Dimming)						
PWMD input low voltage	$V_{PWMD(lo)}$	V_{IN} = 8 ~ 450V	–	–	0.8	V
PWMD input high voltage	$V_{PWMD(hi)}$	V_{IN} = 8 ~ 450V	2.0	–	–	V
PWMD pull-down resistance	R_{PWMD}	V_{PWMD} = 5V	50	100	150	KΩ
LD (Linear Dimming)						
Linear dimming input voltage	V_{LD}	V_{IN} = 12V	0	–	250	mV
Current Sense Comparator						
Current sense threshold voltage	$V_{ISEN(hi)}$		225	250	275	mV
Offset voltage for LD comparator	V_{OFFSET}		-20	–	20	mV
Current Sense Blanking Interval	T_{BLANK}	V_{ISEN} = 0.5V, V_{LD} = V_{DD}	–	200	300	nS
Delay from ISEN trip to GATE lo	T_{DELAY}	V_{IN} = 12V, V_{LD} = 0.15V, V_{ISEN} = 0~ 0.22V after T_{BLANK}	–	110	–	nS
GATE						
GATE source current	Isource	V_{GATE} = 7.5V, V_{DD} = 7.5V	165	–	–	mA
GATE sink current	Isink	V_{GATE} = 0V, V_{DD} = 7.5V	165	–	–	mA
GATE output rise time	T_{RISE}	C_{GATE} = 500pF, V_{IN} = 8V	–	24	50	nS
GATE output fall time	T_{FALL}	C_{GATE} = 500pF, V_{IN} = 8V	–	12	50	nS
Oscillator						
Oscillator frequency	f_{OSC1}	ROSC=1MΩ, f_{OSC1}= 25/(1000(KΩ)+22)MHz	20	24	30	KHz
Oscillator frequency	f_{OSC2}	ROSC=220KΩ,f_{OSC2}= 25/(220(KΩ)+22)MHz	80	101	120	KHz

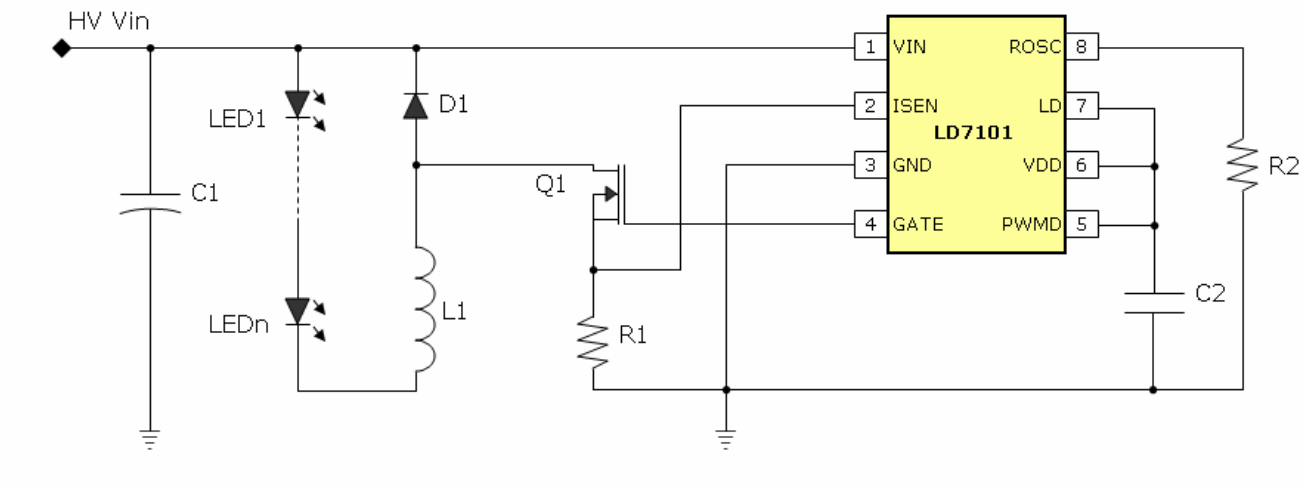
Pin Description

Pin #	Name	Description
1	VIN	Input voltage 8V to 450Vdc for linear regulator
2	ISEN	Inductor peak current sense input - current sense threshold is set at 250mV
3	GND	Power ground
4	GATE	Control signal for external n-channel power MOSFET
5	PWMD	PWM dimming control input - when this pin is set to GND, GATE is tuned off; set to high, GATE is works normally. There is an internal resistor, 100K ohms, pull this pin down to GND.
6	VDD	Regulated voltage 7.5V output from V_{IN}. An external low ESR bypass capacitor >1.0uF/10V is required to connect to the ground.
7	LD	Linear dimming control input
8	ROSC	Frequency is controlled by an external resistor via this pin.

Block Diagram



Typical Application circuit



Package Outline