1.5MHz, 600mA Synchronous Step-Down Regulator

General Description

The XN4406 is a high efficiency monolithic synchronous buck regulator in which constant switching frequency and current mode architecture are introduced. With 2.5V to 5.5V input voltage range, it is an ideal choice for single-terminal Li-Ion battery applications. 100% duty cycle provides low dropout operation and extends battery lifetime in portable systems. The output voltage can be regulated as low as 0.6v and the device can makes the XN4406 support up to 600mA load current. The switching frequency is internally set at 1.5MHz, allowing the usage of small surface mount inductors and capacitors. The internal synchronous switch increases efficiency and eliminates the need for an external Schottky diode. The XN4406 is available in a small profile SOT package with 5 leads.

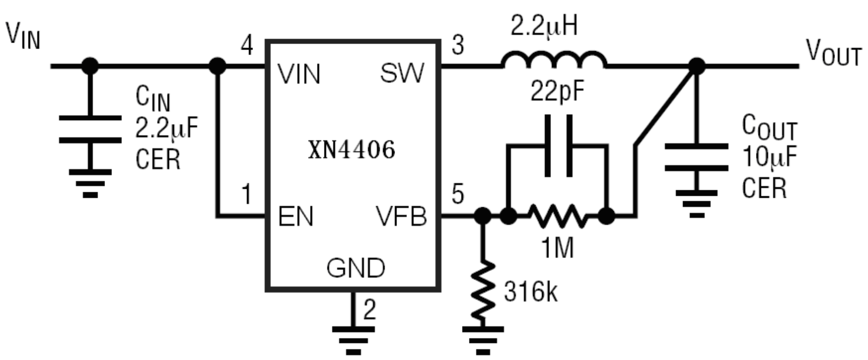
Features

- 1.5MHz constant switching frequency
- 600mA load current available
- 250µA typical quiescent current
- 2.5V to 5.5V input voltage range
- Adjustable output voltage as low as 0.6V
- Low dropout operation at 100% duty cycle
- No Schottky diode required
- Short circuit and thermal protection
- Over voltage protection
- ＜1µA shutdown current
- Available in SOT23-5 package
- High efficiency is up to 95%

Applications

- Cellular and smart phones
- Portable media players/ MP3 players
- Digital still and video cameras
- Portable instruments
- WLAN PC Cards

Typical Application Circuit



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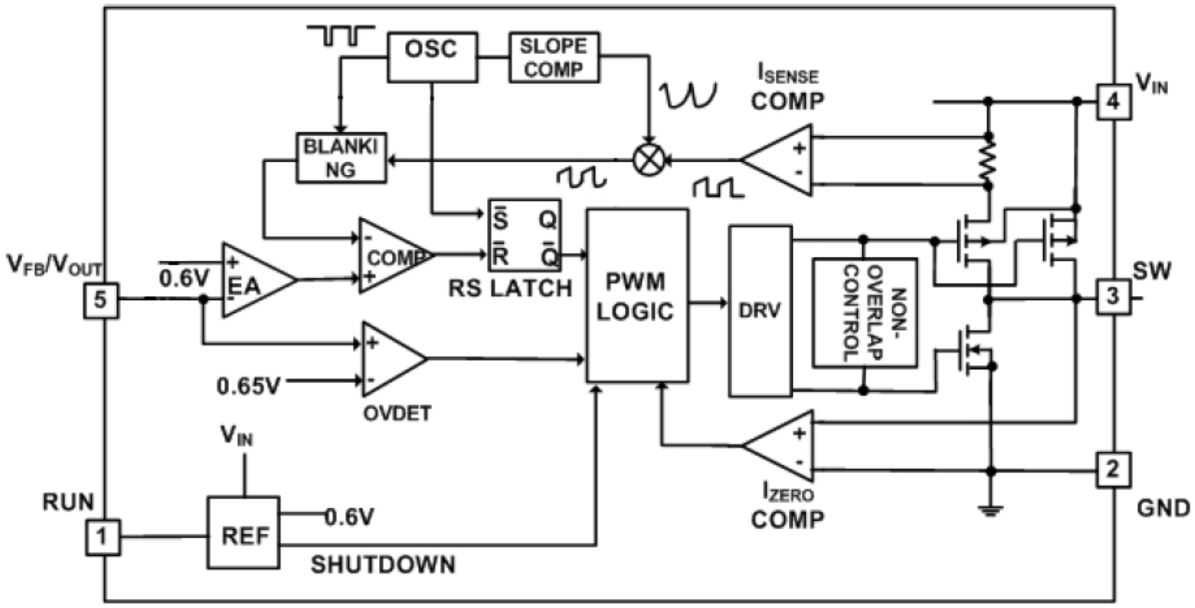
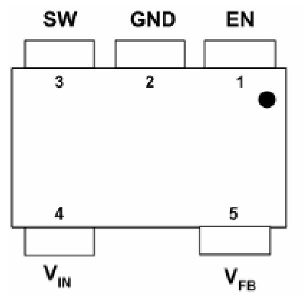
DS.XN4406V1.0

Block Diagram



Pin Definition

Part Number	Pin Configurations
XN4406 **SOT23-5**	

Pin Function Description

Pin #	Name	Function
1	EN	Chip Enable pin. Forcing this pin above 1.5V enables the part. Forcing this pin below 0.3V shuts down the device. Do not leave EN floating.
2	GND	Common ground
3	SW	Switch Node Connection to Inductor. This pin connects to the drains of the internal main and synchronous power MOSFET switches.
4	VIN	Supply voltage pin
5	VFB	Feedback pin

Absolute Maximum Ratings

- Input Supply Voltage ---0.3V to 6V
- EN, VFB Voltages ---0.3V to V_{IN}
- P-Channel Switch Source Current (DC) ---800mA
- N-Channel Switch Sink Current (DC) ---800mA
- Peak SW Sink and Source Current --1.4A
- Operating Temperature Range --40°C to 85°C
- Junction Temperature -- 125°C
- Storage Temperature ---65°C to 150°C
- Lead Temp (Soldering, 10sec) -- 260°C
- ESD Rating (HBM) ---2kV

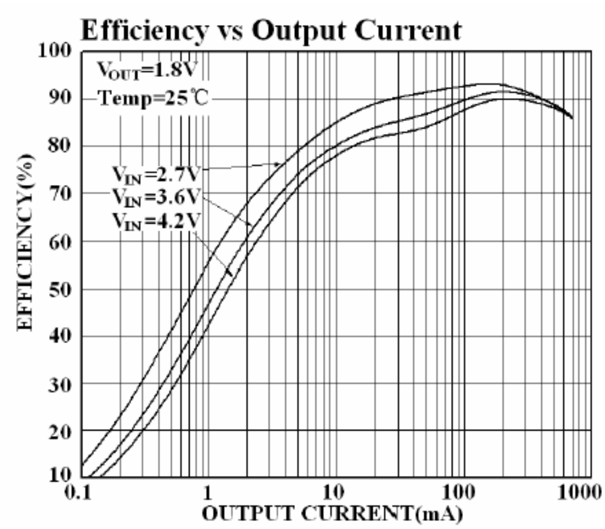
Electrical Characteristics

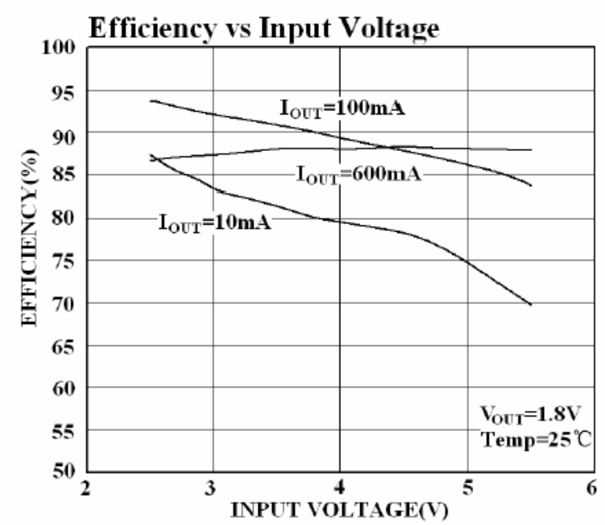
Unless otherwise specified, T_A=25°C, V_{IN}=V_{EN}=3.6V.

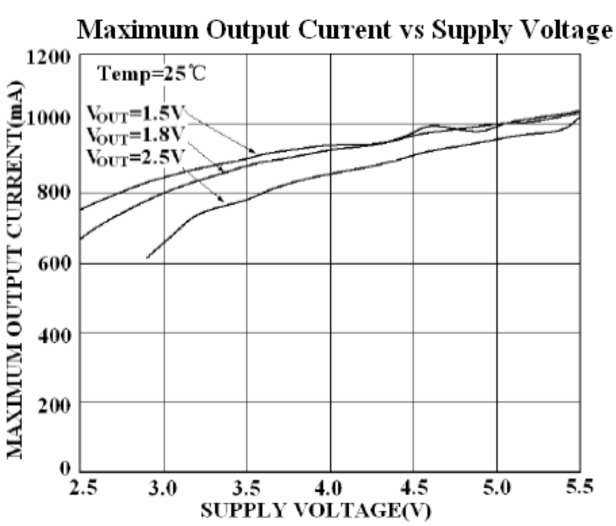
Symbol	Parameter	Conditions	Min	Typ	Max	units
V_{IN}	Iutput Voltage		2.5		5.5	V
I_{VFB}	Feedback Current			50		nA
I_Q	Quiescent Current	V_{FB}=0.5V		250	400	uA
I_{SHDN}	Quiescent Current In Shutdown Mode	V_{EN}=0V, V_{IN}= 4.5V			1	uA
I_{PK}	Peak Inductor Current	V_{IN}=3V, V_{FB}= 0.5V		1.2		A
V_{FB}	Regulated Feedback t Voltage		0.588	0.6	0.612	V
ΔV_{OVL}	Δ Output Over voltage Lockout	$\Delta V_{OVL}=V_{OVL}-V_{FB}$	20	50	80	mV
ΔV_{OUT}	Output Voltage Line Regulation	V_{IN}=2.5V to 5.5V, I_{LOAD}=0		0.2	0.4	%/V
ΔV_{FB}	Reference Voltage Line Regulation	V_{IN}=2.5V to 5.5V, I_{LOAD}=0		0.2	0.4	%/V
$V_{LOADREG}$	Output Voltage Load Regulation	I_{LOAD}=0mA to 600mA		0.5		%
f_{OSC}	Oscillator Frequency	V_{FB}=0.6V	1.2	1.5	1.8	MHz
		V_{FB}=0V		210		kHz
R_{PFET}	$R_{DS(ON)}$ of P-Channel	I_{SW}=100mA		0.26	0.4	Ω

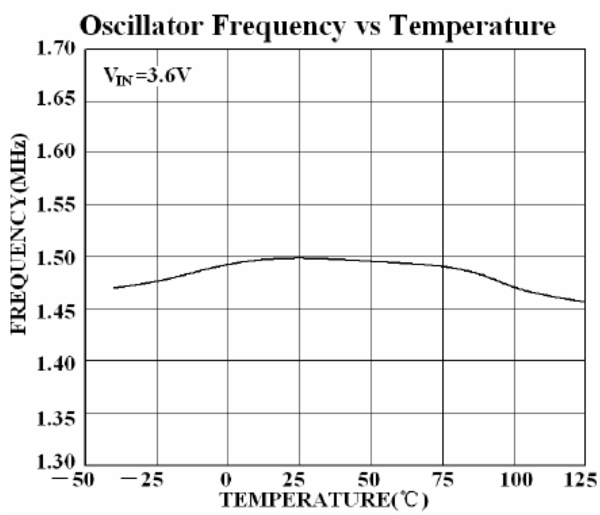
	FET					
R_{NFET}	$R_{DS(ON)}$ of N-Channel FET	I_{SW}=-100mA		0.26	0.4	Ω
I_{LSW}	SW Leakage Current	V_{EN}=0V, V_{SW}=0V or 5V, V_{IN}=5V			±1	uA
V_{EN}	EN Threshold		0.3	1	1.5	V
I_{EN}	EN Leakage Current				1	uA

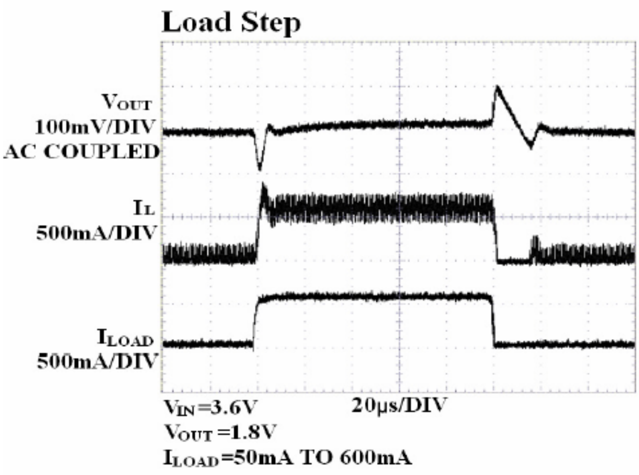
Typical Operating Characteristics

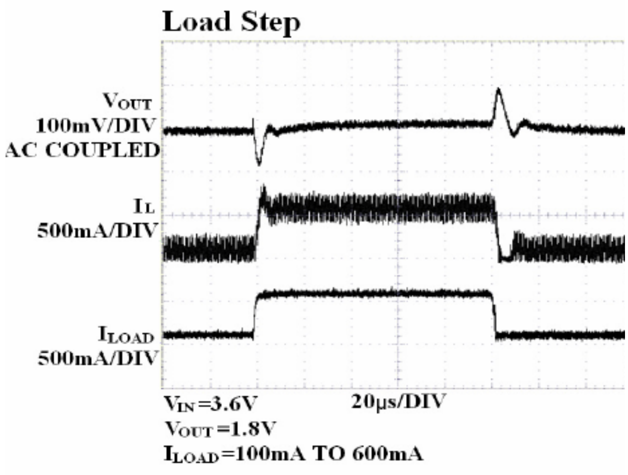









Load Step
VOUT
100mV/DIV
AC COUPLED
IL
500mA/DIV
ILOAD
500mA/DIV
VIN=3.6V
20μs/DIV
VOUT=1.8V
ILOAD=50mA TO 600mA


Load Step
VOUT
100mV/DIV
AC COUPLED
IL
500mA/DIV
ILOAD
500mA/DIV
VIN=3.6V
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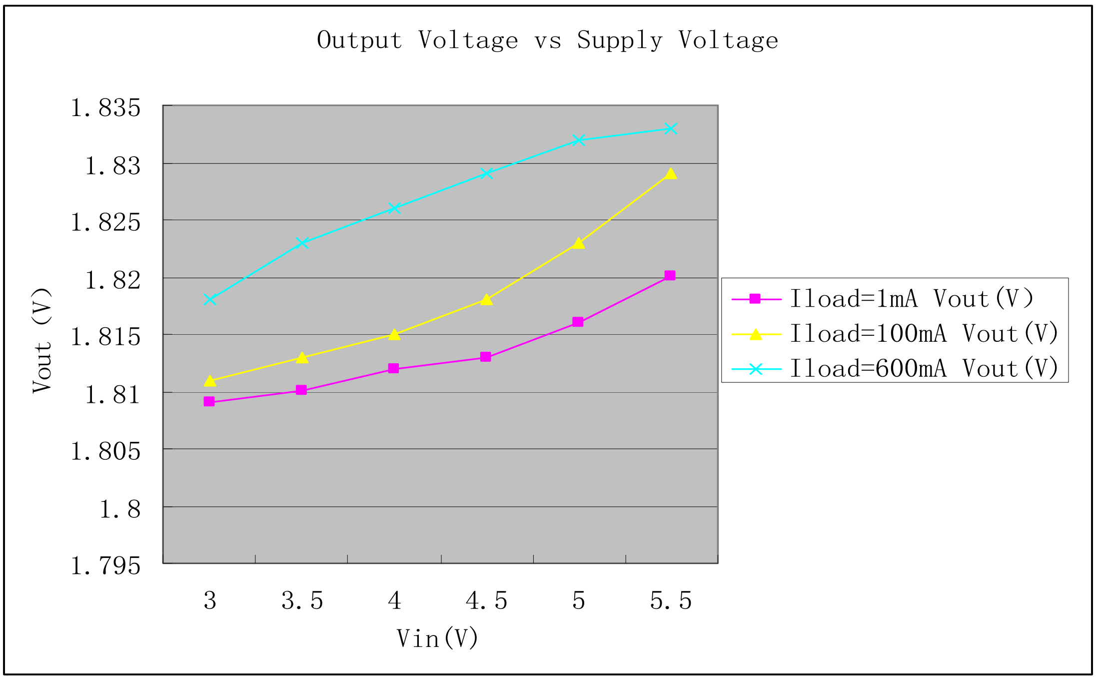
VOUT=1.8V
ILOAD=100mA TO 600mA


Output Voltage vs Supply Voltage
1.835
1.83
1.825
1.82
1.815
1.81
1.805
1.8
1.795
Vout (V)
3
3.5
4
4.5
5
5.5
Vin(V)
Iload=1mA Vout(V)
Iload=100mA Vout(V)
Iload=600mA Vout(V)

Function Description

Main Control Loop

The XN4406 uses a slop-compensated constant frequency, current mode PWM architecture. Both the main (P-Channel MOSFET) and synchronous (N-channel MOSFET) switches are internally integrated. During normal operation, the XN4406 modulates the output voltage by switching at a constant frequency and then modulating the power transferred to the load each cycle using PWM comparator. There are totally three weighted differential signals, the output feedback voltage coming from the external resistance divider, the current sampling of main switch, and the slope-compensated ramp. It modulates output power by adjusting the peak inductor current during the first half of each cycle. An N-channel, synchronous switch turns on during the second half of each cycle (off time). When the inductor current starts to reverse or the PWM reaches the end of the oscillation period, the synchronous switch turns off. This can prevent excess current flowing backward through the inductor, flowing forward through the output capacitor to GND, or through the main and synchronous switch to GND.

Inductor Selection

The output inductor is selected to limit the ripple current to some predetermined value, typically 20%~40% of the full load current at the maximum input voltage. Large inductors generally have lower ripple currents. Bigger V_{IN} or V_{OUT} give rise to larger ripple current as shown in the formula below. A reasonable starting point for ripple current setting is ΔI_L=240mA (40% of 600mA).

$$\Delta I_L=(1-V_{OUT}/V_{IN})V_{OUT}/(f)(L)$$

The DC current rating of the inductor should not be smaller than the sum of the maximum load current and the ripple current divided by two to prevent core saturation. Thus, a 720mA (600mA+120mA) rated inductor should be big enough for most applications. Inductors with lower DC-resistance are chosen to get better efficiency.

C_{IN} and C_{OUT} Selection

In continuous current-mode, the source current of the top MOSFET is a square wave of duty cycle determined by V_{OUT}/V_{IN}. The input capacitor is introduced to provide a low impedance loop for the edges of current pulse drawn by XN4406. The input capacitor should be equipped with small ESR and meet the maximum RMS current requirements. Additionally, the input capacitance, which is typically 4.4uF, is determined by load, impedance characteristics of the input/output voltage. The equation for the maximum RMS current in the input capacitor is. The output capacitor C_{OUT} can greatly affect the loop stability. Moreover, the ESR value, which is a basic parameter of C_{OUT}, should also be considered. Physically speaking, larger capacitors are generally equipped with smaller ESRS. Once the ESR requirement for C_{OUT} has been met, the RMS current rating generally far exceeds the I_{RIPPLE} (P-P) requirements. The output ripple ΔV_{OUT} is determined by:

$$\Delta V_{OUT}=\Delta I_L(ESR+1/8fC_{OUT})$$

The X5R or X7R dielectric formulations are generally chosen for the input and output ceramic capacitors. These dielectrics have the best temperature and voltage characteristics among all the ceramics for a given value and size.

Thermal Considerations

A thermal analysis should be done to keep XN4406 away the maximum junction temperature. The temperature rise is given by:

$$T_R=(P_D)(\theta_{JA})$$

Where $P_D=I_{LOAD}^2 \times R_{DS(ON)}$ is the power dissipated by the regulator ; θ_{JA} is the thermal resistance from the junction of the die to the ambient temperature. The junction temperature, T_J, is given by:

$$T_J=T_A+T_R$$

T_A is the ambient temperature. T_J should be below the maximum junction temperature of 125°C.

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PC Board Layout Checklist

The following guidelines should be complied to ensure proper operation during PCB layout.

1. The input capacitor C_{IN}, which provides the AC current to the internal power MOSFET, should be connected to V_{IN} as closely as possible.
2. The power traces, which consists of the GND trace, the SW trace and the VIN trace, should be kept short, direct and wide.
3. The V_{FB} pin should be connected directly to the feedback resistors. The resistive divider R1/R2 must be connected between the C_{OUT} and ground.
4. Keep the switching node (SW) away from the sensitive V_{FB} node.