DYNAMIC ANALYSIS AND CONTROL DESIGN OF LCC RESONANT CONVERTER

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Abstract: *Dynamics of LCC resonant converters are investigated by using a newly developed small-signal model which is accurate up to the switching frequency. It is shown that the beat frequency dynamics are not only related to the operating region but also heavily dependent on the output filter design. This paper concentrates on frequency control of LCC resonant converters. Compensator designs are discussed taking into consideration of the strong impact of beat frequency dynamics. The frequency domain analyses are verified using accurate large-signal simulations.*

I. INTRODUCTION

Soft-switching features of resonant converters make them desirable for high frequency, high power applications. Among many converter topologies, the LCC resonant converter is quite popular [1-3]. An LCC resonant converter is very similar to a parallel resonant converter (PRC), except that a series capacitor is added to the resonant tank, as shown in Fig.1. For given design specifications, a properly designed LCC resonant converter has less current stress than a PRC does, because LCC resonant converter combines the advantages of series resonant converters (SRCs) and PRCs. Therefore, LCC resonant converters are also called series-parallel resonant converters (SPRCs).

By using the extended describing function technique [4, 5], the continuous-time small-signal model of the LCC resonant converter was derived in a closed form, and the equivalent circuit model was also synthesized [6]. The model can be used as a tool to investigate the dynamics of the converters and to clarify the issues involved with the control design.

In this paper, the frequency control of LCC resonant converters is studied. It is known that the system dynamics, which include low frequency output filter dynamics and beat frequency dynamics [7], are dependent on switching frequency and load resistance. As a significant result of this paper, it is shown that the beat frequency is determined not only by the operating point, but also by the output filter design. If the output filter is well designed, the beat frequency dynamics will only occur at high frequency (above one fourth of the switching frequency), rather than at low frequency as implied in [7], when the switching frequency is close to the resonant frequency. The compensation could only be designed optimally with the considerations of the beat frequency dynamics which usually limit the control bandwidth.

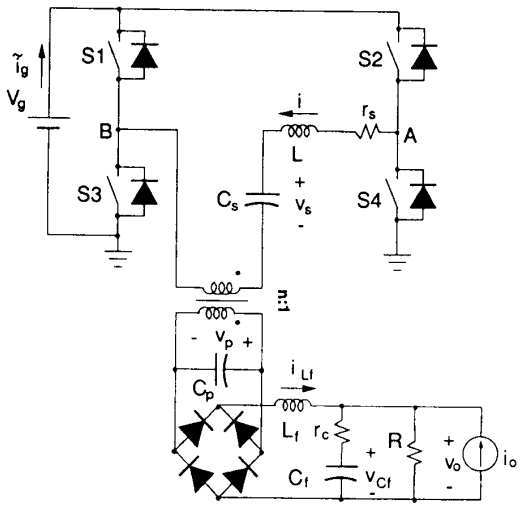

Fig. 1 The circuit diagram of an LCC resonant converter.

For given specifications of a high-frequency application, the operating region selection is considered based on the optimal design of power stage. The worst case dynamics are then identified, and the discussion of compensator design follows.

Section II of this paper discusses the dynamic features of LCC resonant converters. In section III, complete design procedures are illustrated by an example, and large-signal verification is provided. Section IV concludes the paper.

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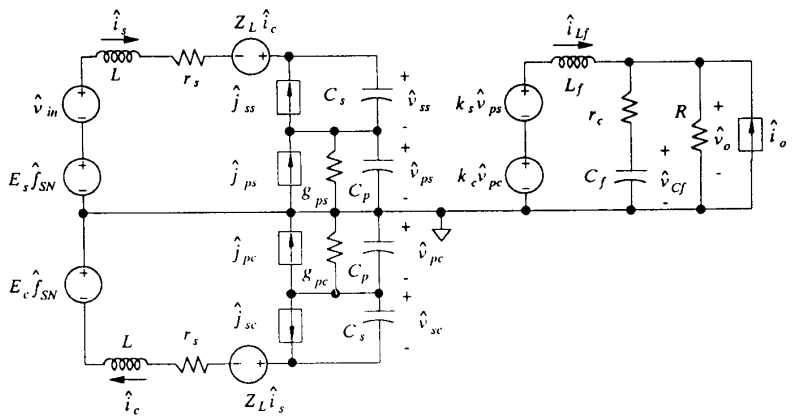

Fig. 3 Small-signal circuit model of LCC resonant converters [6].

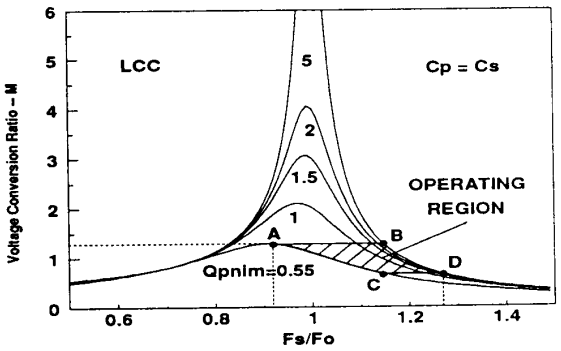

Fig. 2 Voltage conversion ratio of LCC resonant converters.

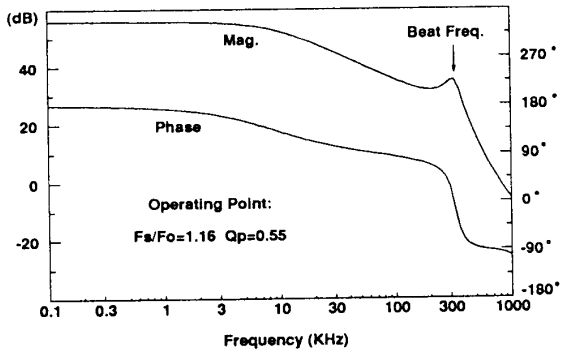

Fig. 4 Typical control-to-output transfer function of LCC resonant converters.

II. DYNAMICS OF LCC RESONANT CONVERTERS

The voltage conversion ratios of LCC resonant converters are shown in Fig. 2 [2, 6]. In this paper, frequency control of LCC resonant converters is discussed, hence the switching frequency is the control variable. In Fig. 2, the switching frequency is normalized to the natural resonant frequency of the converter, which is defined as:

$$F_o = \frac{1}{2\pi\sqrt{LC_e}}, \tag{1}$$

where the equivalent resonant capacitance, C_e, is defined by:

$$C_e = \frac{C_s C_p}{n^2 C_s + C_p} \quad . \tag{2}$$

The transformer turns ratio is denoted by n. The characteristic impedance of the resonant tank is given by:

$$Z_o = \sqrt{\frac{L}{C_e}} \quad . \tag{3}$$

Using the small-signal circuit model shown in Fig. 3, the typical control-to-output transfer function can be obtained by PSPICE simulation, and it is shown in Fig. 4. This transfer function has the form of

$$\frac{\hat{v}_o}{\hat{f}_{SN}} = G(s) \tag{4}$$

$$= \frac{G_o(1 + s/\omega_{esr})}{(1 + s/\omega_{p1})(1 + s/\omega_{p2})(1 + s/\omega_b Q_b + s^2/\omega_b^2)}$$

The low frequency gain, G_o, is a product of the line voltage and the slope of the dc conversion ratio curve at the given operating point:

$$G_o = \left(\frac{\partial V_o}{\partial F_{SN}}\right) = V_g\left(\frac{\partial M}{\partial F_{SN}}\right) \quad . \tag{5}$$

The zero is caused by parasitic resistance (esr) of output capacitor, to give

$$\omega_{esr} = \frac{1}{r_c C_f} \quad . \tag{6}$$

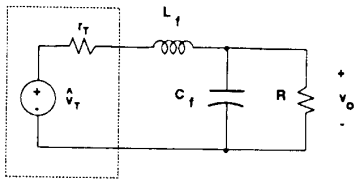

Fig. 5 The low frequency equivalent circuit of the resonant tank determines the damping of the output filter.

The output filter poles, $\{\omega_{p1}, \omega_{p2}\}$, are usually heavily damped by both the load resistance and the output resistance of the resonant tank, as shown in Fig. 5, where the resonant tank part of the small-signal model is simplified by its low frequency Thevenin's equivalence.

Usually, the damping factor is dominated by the equivalent tank resistance, r_T:

$$Q_f \approx \frac{Z_f}{r_T} \quad , \tag{7}$$

where

$$Z_f = \sqrt{\frac{L_f}{C_f}} \tag{8}$$

is the characteristic impedance of the output filter.

The interaction between the switching frequency and the resonant frequency results in the beat frequency dynamics. This unique feature of resonant converters was first studied by Vorperian [7]. The beat frequency dynamics are specified by $\{\omega_b, Q_b\}$. This double pole causes an additional 180° phase lag, which must be carefully considered in the control loop design.

Since the system dynamics are complex function of the design parameters and the operation conditions, it is very difficult to provide explicit expressions of system poles analytically without sacrificing accuracy. Instead of making simplified assumptions, the closed form small-signal model derived in [6] will be used to generate system pole loci under different designs and operation conditions.

A. Varying Switching Frequency (F_S/F_o)

The dc conversion ratio curves are redrawn in Fig. 6. If the operating point moves from A to B while the load remains unchanged ($Q_p = 1$), the system poles will move as shown in Fig. 7(a). We can see the damping of the output filter poles first decreases, then increases, and finally decreases again. We know that the damping is related with the load sensitivity of the resonant tank, or the output resistance, r_T, of the tank. The damping variation can be explained by the fact that r_T first decreases, then

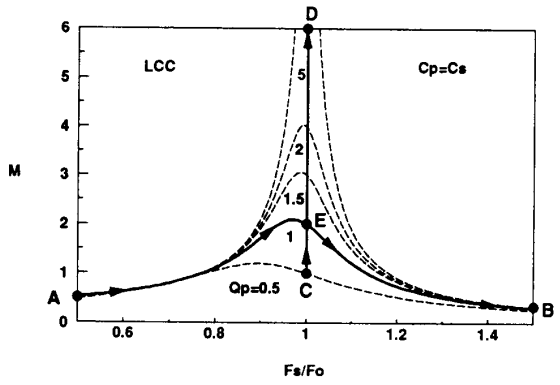

Fig. 6 Varying operating conditions will change the system root loci.

increases, and finally decreases again as the operating point moves from A to B on the curve $Q_p = 1$.

The beat frequency poles first move towards the origin of the complex plane as the switching frequency approaches the resonant frequency, then run away in high frequency direction as the switching frequency moves to point B. It is important to know that the beat frequency is not simply the difference between the switching frequency and the resonant frequency., *i.e.*

$$\omega_b \neq | \omega_s - \omega_o | \quad , \tag{9}$$

because when the switching frequency is swept from below the resonant frequency to above it, the beat frequency does not go to zero or even close to zero. The lowest beat frequency occurs when the switching frequency is right on the peak of the dc conversion ratio curve. The quality factor, Q_b, has higher values above the resonant frequency than below it.

To sum up, the operating points can be selected near the resonant peak to minimize the reactive power and improve efficiency, without fearing that the beat frequency reduces to very low frequency such that it affects the control loop design and limits the band width.

B. Varying Load (Q_p)

As the operating point moves from point C to D, as shown in Fig. 6, the root loci associated with this change are shown in Fig. 7(b). We can see that as Q_p increases, the damping of the output filter poles and of the beat frequency poles is reduced, while the beat frequency essentially remains constant.

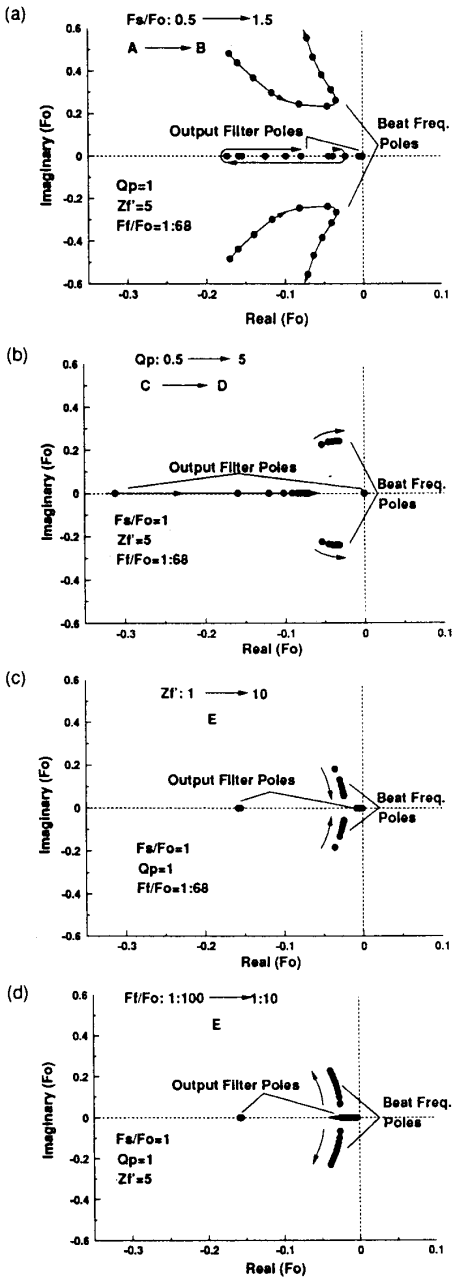

Fig. 7 Root loci under different conditions and design.
(a) Changing switching frequency;
(b) Changing load;
(c) Changing output filter characteristic impedance;
(d) Changing output filter corner frequency.

C. Varying Output Filter Design (Z_f, F_f)

If the operating point is fixed at point E in Fig. 6, and the characteristic impedance of the output filter, Z_f, increases while the corner frequency of the output filter

$$F_f = \frac{1}{2\pi\sqrt{L_f C_f}} \tag{10}$$

remains constant, the root loci will look like in Fig. 7(c). It is clear that the beat frequency decreases as Z_f increases. If Z_f is fixed and the corner frequency of the output filter, F_f, increases, the beat frequency will increase, as shown in Fig. 7(d).

This is a very interesting fact that has not been reported before: the beat frequency dynamics can be affected by the output filter design. By reducing the characteristic impedance, Z_f, or increasing the corner frequency, F_f, the beat frequency can be pushed to higher frequency. Usually, the corner frequency, F_f, is determined by the output ripple specification; it cannot be too high. Often we want the converter to operate in a continuous inductor current mode at light load, which means that the output filter inductance can not be too small, so as the value of Z_f. This issue will be further addressed in the next section, where we will see that in a practical design, the beat frequency will not reduce to a dangerously low value to affect the loop gain and stability.

In this section, the relations between system dynamics and operating conditions as well as output filter design are discussed. The knowledge of these relations will help us to design the control loop.

III. A DESIGN EXAMPLE

For a high frequency LCC resonant converter, the following specifications are given:

input voltage: $V_g = 200V---400V$;

output voltage: $V_o = 50V$;

output power: $P_o = 500W$;

switching frequency: $F_S = 1MHz---1.38MHz$.

The selection of the operating region, aimed at optimizing the power stage design, is discussed first. The compensator design is then discussed, and the analysis results are verified by large-signal simulations.

A. Power Stage Design

For this high frequency application, MOSFETs should be used, and zero voltage switching (ZVS) of these switches is desirable. Therefore, the operating region should be higher than the resonant frequency. An optimal

design of power stage should minimize the reactive power and current stress for the given switching frequency range.

To reduce the reactive power, an operating point should, ideally, be right on the peak of the conversion ratio curve (Fig. 2), so that the inductor current and tank voltage (v_{AB}) are in phase, and all of the power transferred to the tank is delivered to the load. Since only a little amount of reactive power is needed to achieve ZVS, the operating point should be slightly at the right side of the resonant peak. It can be shown that by choosing a lower Q_p value, it reduces current stress, resonant inductor size and transformer turns ratio. But the switching frequency range will increase, which is not desirable for the optimizing of magnetic components. The detailed design trade-offs are beyond the scope of this paper. But we can conclude that for a given switching frequency rang, the lower Q_p is the better design.

For the given specifications at beginning of this section, the operating region is chosen, as shown in Fig. 2, according to the principles mentioned above. Then, it is easy to come up with the power stage design:

$$n = 5 \quad Z_o = 227.2\Omega \quad F_o = 1.09MHz$$

$$L = 33.2\mu H \quad C_s = 1.28nF \quad C_p = 32.1nF$$

It can be shown that under the following light load condition, the output choke current will be in discontinuous mode (DCM):

$$R > 26L_f F_{Smin}. \tag{18}$$

If we define the light load as 10% of the full load, and we want the choke current to be in continuous conduction mode from the light load to the full load, then

$$L_f = \frac{10R_{\min}}{26F_{Smin}} = 1.92\mu H. \tag{19}$$

If the output voltage ripple is less than 0.1%, the corner frequency of the output filter can be found by

$$F_f \approx 2F_{Smin}\sqrt{\frac{2}{\pi}\left(\frac{\delta v_o}{V_o}\right)} = 50KHz. \tag{20}$$

The output capacitance is then determined to give

$$C_f = \frac{1}{L_f(2\pi F_f)^2} = 5.28\mu F. \tag{21}$$

B. The Worse Case Dynamics

Assume that the parasitic resistance of the output capacitor (esr) has the value

$$r_C = 50m\Omega, \tag{22}$$

the control-to-output transfer functions at the four corners of the operating region (points A, B, C, D, Fig. 2) can be obtained as shown in Fig. 8. The values of $\{\omega_{p1}, \omega_{p2}, \omega_b, Q_b, G_o\}$ are shown in Table 1.

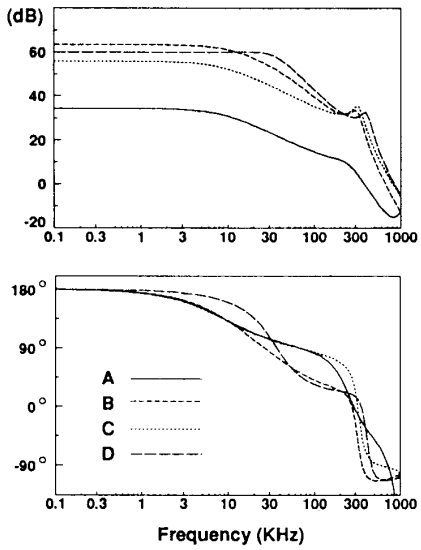

Fig. 8 The control-to-output transfer functions at four corners of the operating region. The worst case dynamics occur at operating point D.

Table 1. Parameters of Control-to-Output Transfer Function

	$f_{p1}(KHz)$	$f_{p2}(KHz)$	$f_b(KHz)$	Q_b	$G_o(dB)$
A	9.15	227	258	1.18	34.2
B	12.2	53.3	316	4.14	63.5
C	8.88	313	327	4.23	55.9
D	35.8	35.8	407	4.28	60.0

For this practical design, the lowest beat frequency occurs at point A (low-line, full-load) which is almost on the peak of the dc curve (Fig. 2), but the beat frequency is as high as 258KHz. Such a high beat frequency will not adversely affect the control loop design and the dynamics.

The loop gain method [8] is used in designing the control loop. The loop gain, denoted as $T(s)$ in Fig. 9, is given by

$$T(s) = G(s)H(s), \tag{23}$$

where $H(s)$ is the compensator transfer function including the gain of voltage controlled oscillator (VCO). The compensator should be designed such that it can provide a wide control bandwidth while maintaining adequate phase margins for the loop gain in the entire operation region.

Since the beat frequency dynamics causes an additional 180° phase lag, it is very hard to design the control loop

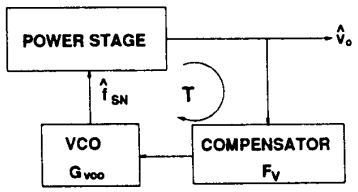

Fig. 9 Block diagram of the feedback control loop.

with cross-over frequency higher than the beat frequency, unless the beat frequency poles can be effectively cancelled by the compensation network. This cancellation cannot be easily implemented because the beat frequency poles are moving poles according to the given operating conditions.

Based on the above considerations, the loop gain cross-over frequency should be lower than the beat frequency. From Fig. 8, we can see that the transfer function of the operating point D (high-line, light-load) has the highest gain and the largest phase lag. Therefore, the high-line, light-load case is used as the worst case for the compensation design.

C. Compensation Design

Two commonly used compensators are considered, as shown in Fig. 10; they are two-pole one zero compensator (type I) and three-pole two-zero compensator (type II), respectively.

The type I compensator has transfer function

$$H(s)=\frac{K_M(1+s/\omega_{zc1})}{s(1+s/\omega_{pc1})}. \tag{24}$$

The positions of the pole, ω_{pc1}, and of the zero, ω_{zc1}, and the integration gain, K_M, need to be designed. The compensator pole is usually selected to cancel the esr zero of the control-to-output transfer function $G(s)$ as shown in (4). By adjusting the position of the compensator zero and the integration gain, we can maximize the control bandwidth and maintain the phase margin about 45°. Cancelling the first pole of $G(s)$ by the compensator zero

$$\omega_{zc1}=\omega_{p1}, \tag{25}$$

so that the loop gain, $T(s)$, will keep (-1) slope (-20dB/dec) up to the second pole of $G(s)$, then change to (-2) slope. The integration gain can then be adjusted to make the loop gain cross-over frequency at the second pole of $G(s)$:

$$\omega_c=\omega_{p2}. \tag{26}$$

In this way, the control bandwidth is maximized, and the phase margin is about 45°. These design considerations are illustrated by asymptotic lines, as shown in Fig. 11.

With type I compensator, the cross-over frequency is limited by ω_{p2}. If the type II compensator is used, which has the transfer function

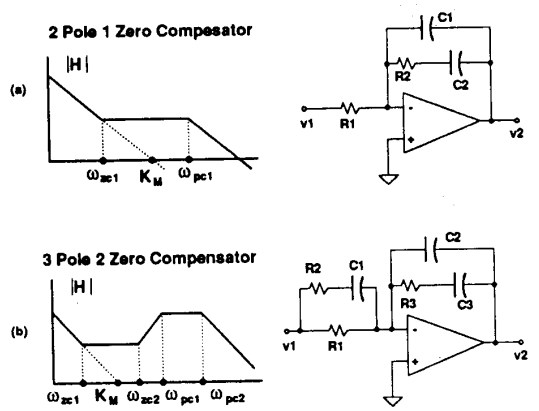

Fig. 10 Two commonly used compensators.
(a) Type I: two-pole one-zero compensator;
(b) Type II: three-pole two-zero compensator.

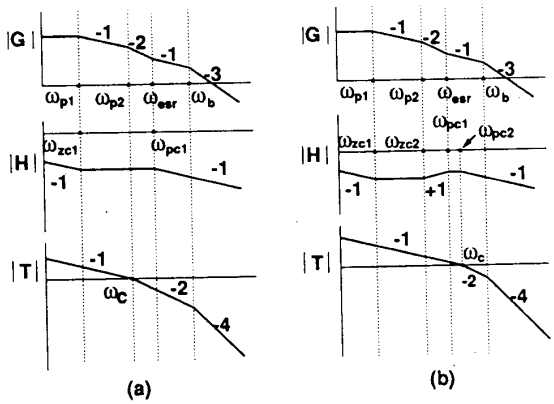

Fig. 11 The asymptotic representation of the loop gains.
(a) Using type I compensator;
(b) Using type II compensator.

$$H(s)=\frac{K_M(1+s/\omega_{zc1})(1+s/\omega_{zc2})}{s(1+s/\omega_{pc1})(1+s/\omega_{pc2})}, \tag{27}$$

there is one more zero available to cancel the second pole of $G(s)$ at ω_{p2}, hence the (-1) slope can be stretched to a higher frequency. Still, the first compensator pole is to cancel the esr zero, and the second compensator pole can be put below the beat frequency to reduce the detrimental effects of the beat frequency peaking. The loop gain cross-over frequency is now at ω_{pc2} where the slope changes from (-1) to (-2), and the phase margin is about 40°, as shown in Fig. 11.

Based on the above discussion, it is obvious that type II compensator is superior to type I compensator. The loop gain of operating point D (worst case, high-line, light-load) is obtained with type II compensator, as shown in Fig. 12.

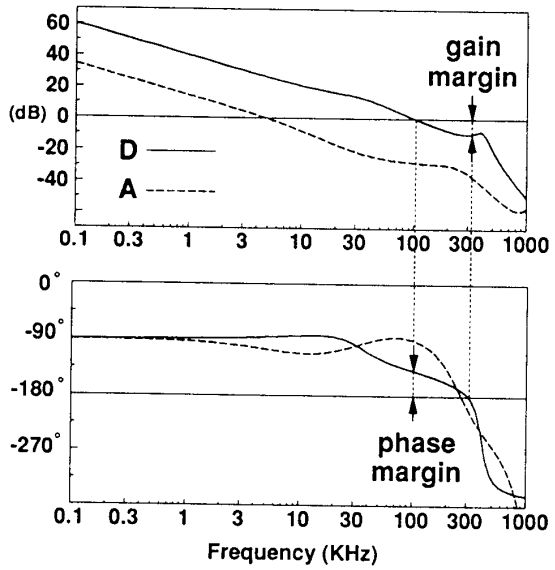

Fig. 12 The loop gains of high-line light-load case (D) and low-line full-load case (A).

We can see from the figure both the phase margin and the gain margin are adequate. Therefore, the converter will be stable for the entire operating region.

There is an intrinsic shortcoming of LCC resonant converters operating in the frequency control as illustrated in Fig. 12: the control bandwidth drops significantly for low-line, full-load operations (point A). This phenomenon can be explained by the fact that the low-frequency gain, G_o, of the control-to-output transfer function, which is determined by line voltage and slope of dc curve, is much lower at low-line full-load case (near operating point A in Fig. 2) than it is under other operating conditions (Fig. 8). In this design example, the gain is about 25 dB lower than that of the worst case (Table I). This gain variation range can be reduced if the operating region is selected away from the resonant peak, but that selection will cause more reactive power flowing in and out of the resonant tank, which is not beneficial for the efficiency. This trade off issue is typical also for other resonant converters.

It is desirable to adopt some adaptive control schemes to schedule the compensator gain by sensing the line voltage and load current. One of the possible schemes is to use current mode control because the gain of control-to-inductor current transfer function varies in a similar pattern to that of control-to-output transfer function as operating point changes. Therefore, closing the current loop will cancel the gain variation of the outer voltage loop. The details of these control methods are beyond the scope of this paper.

D. Large Signal Simulation

The closed-loop output impedances at operating points

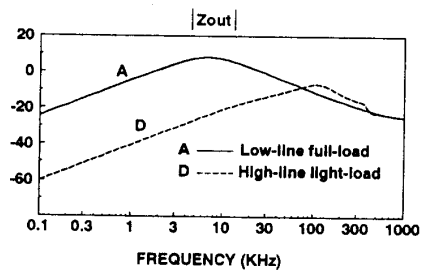

Fig. 13 The closed-loop output impedances.

A & D are shown in Fig. 13. The following cases are set up to verify the frequency domain analyses by accurate large-signal simulations.

1: step load from 125W ($Q_p = 2.2$) to 50W ($Q_p = 5.5$) at high line;

2: the same step load as in Case 1, but with the compensator gain increased such that the loop gain has 0° phase margin at operating point D;

3: step load from 425W ($Q_p = 0.647$) to 500W ($Q_p = 0.55$) at low line;

The corresponding simulation results are shown in Fig. 14. For 15% step load current around operating point D, the voltage overshoot is about 1% and the settling time is about 20 micro seconds (Fig. 14 (a)). In Fig. 14 (b), we can see that the output voltage is oscillatory as the phase margin drops to zero; the system becomes unstable. Figure 14 (c) shows the response for the same 15% step load around operating point A, the voltage undershoot is about 2.4% and the settling time is 60 micro seconds. The step load response at the point A is worse than that at the point D because the output impedance, Z_o, has higher peak value near the operating point A than near point D.

These accurate large-signal simulations support the conclusions of the small-signal analyses.

IV. CONCLUSIONS

The dynamic features of LCC resonant converters with frequency control are investigated by employing a newly developed small-signal model. The control-to-output transfer function is fourth order with two low frequency poles contributed by the output filter and two high frequency poles caused by the interaction of the switching frequency and the natural resonant frequency, often referred to as the beat frequency dynamics. It is shown that the beat frequency is affected not only by the operating point (switching frequency and load) but also by the output filter design. For a well designed power stage, the

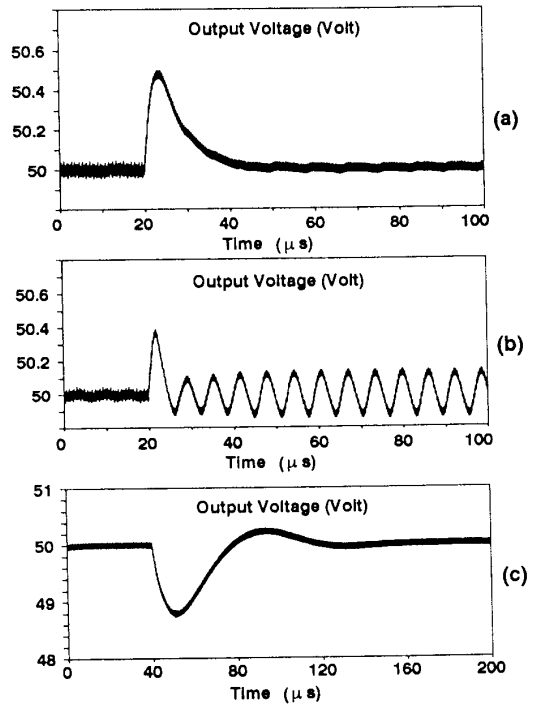

Fig. 14 **The large signal-simulations of step load responses.**
(a) Output voltage under step load from 125W to 50W ($Q_p = 2.2 \rightarrow 5.5$**);**
(b) Output voltage becomes oscillatory when phase margin of the loop gain drops to zero.
(c) Output voltage under step load from 425W to 500W ($Q_p = 0.647 \rightarrow 0.55$**);**

beat frequency is higher than one forth of the resonant frequency and will not cause significant degradation to control loop design.

Generally, the operating region should be selected close to resonant peak to minimize the reactive power and with as low as possible Q_p to minimize the current stress. The cross-over frequency should be lower than the beat frequency to avoid abrupt phase dropping and resonant peaking. The three-pole two-zero compensator is suggested. The worst-case dynamics occur under the high-line light-load condition.

The performance of the feedback control will degenerate when converter is operated under low-line full-load condition, because the control gain drops significantly. Adaptive control schemes are suggested for a better performance. Although the dynamics and control are studied only for LCC resonant converters, the problems and conclusions are typical for other resonant converters as well.

Finally, the frequency domain analyses are verified by accurate large-signal simulations.

REFERENCES

[1] A. K. S. Bhat, and S. B. Dewan, "Analysis and design of a high-frequency resonant converter using LCC-type commutation," IEEE Trans. Power Electron., Vol. 2, no. 4, pp. 291-301, 1987.

[2] R. L. Steigerwald, "A comparison of half-bridge resonant converter topologies," IEEE Trans. Power Electron., Vol. 3, no. 2, pp. 174-182, 1988.

[3] I. Bataresh, R. Liu, C. Q. Lee, and A. K. Upadhyay, "150 Watts and 140 KHz multi-output LCC-type parallel resonant converter," Proc. APEC, pp. 221-230, 1989.

[4] S. Sanders, J. Noworolski, X. Liu, and G. Verghese, "Generalized averaging method for power conversion circuits," in IEEE Power Specialists' Conf. Rec., pp. 273-290, 1989.

[5] E. X. Yang, F. C. Lee, and M. M. Jovanovic, "Small-signal modeling of power electronic circuits using extended describing function concept," Proc. VPEC Seminar, pp. 167-178, 1991.

[6] E. X. Yang, F. C. Lee, and M. M. Jovanovic, "Small-signal modeling of LCC resonant converter," in IEEE Power Specialists' Conf. Rec., 1992.

[7] Vatche Vorperian, "Approximate small-signal analysis of the series and parallel resonant converters," IEEE Trans. Power Electron., Vol. 4, no. 1, pp. 15-24, 1989.

[8] R.B. Ridley, B.H. Cho, and F.C. Lee, "Analysis and interpretation of loop gains of multi-loop-controlled switching regulator," IEEE Trans. Power Electron., pp. 489-497, 1988.