■ INTRODUCTION:

The CE3320 is a 2A Li-Ion battery charger intended for 5V wall adapters. It utilizes a 1.5MHz synchronous buck converter topology to reduce power dissipation during charging. Low power dissipation, an internal MOSFET and sense resistor allow a physically small charger that can be embedded in a wide range of handheld applications. The CE3320 includes complete charge termination circuitry, automatic recharge and a ±1% float voltage. Input short-circuit protection is included, so no blocking diode is required.

Battery charge current, charge timeout and end-of-charge indication parameters are set with external components. Additional features include shorted cell detection, temperature qualified charging and overvoltage protection.

■ APPLICATIONS：

- Battery Back-Up Systems
- Tablets and Portable Mobile Internet Devices
- Netbook, Smartbook
- Portable Media Players
- IPod, iTunes, iPhone, iPad Docking
- Bluetooth speaker & 2.4G Wireless speaker
- Smart Phones
- Portable Data Capture Terminals
- Personal Medical Products
- Portable Instruments
- 3G/4G Wireless Routers

■ FEATURES:

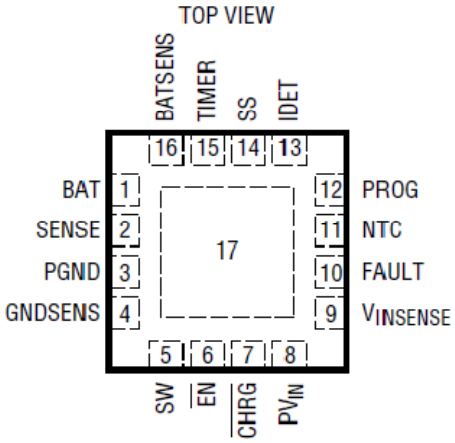
- 1.5MHz PWM/Linear Charger
- Low Power Dissipation
- 2A Maximum Charge Current
- No External MOSFETs, Sense Resistor or Blocking Diode Required
- Battery Preconditioning/Constant Current/Constant Voltage Charge Mode
- Precharge Conditioning for Reviving Deeply Discharged Cells and Minimizing Heat Dissipation During Initial Stage of Charge
- Programmable Charge Current Detection/Termination
- ±10%Charge Current Accuracy
- Preset Float Voltage with ±1% Accuracy
- Remote Sensing at Battery Terminals
- IDET Blanking
- Programmable Charge Termination Timer
- Automatic Recharge
- Charge Current Monitor Output for Gas Gauging
- Charge Status Indication
- Thermistor Input for Temperature Qualified Charging
- Shorted Cell Detection
- Battery Fault Indication
- Input Short-Circuit Protection, No Blocking Diode Required
- Compatible with Current Limited Wall Adapters
- Undervoltage Lockout and Automatic Shutdown
- Soft-start To Prevent High Start-up Current
- Overtemperature Shutdown
- Uses Small,Low Profile External Components

■ ORDER INFORMATION(1)

Operating free air temperature range	Battery Float Voltage	Package	Device No.
-40~+85℃	4.10V	QFN4X4-16	CE3320A410QD16
-40~+85℃	4.15V	QFN4X4-16	CE3320A415QD16
-40~+85℃	4.20V	QFN4X4-16	CE3320A420QD16
-40~+85℃	4.35V	QFN4X4-16	CE3320A435QD16

(1)Contact Chipower to check availability of other battery float voltage versions.

■ PIN CONFIGURATION:



PIN FUNCTIONS

PIN		TYPE(1)	DESCRIPTION
NO.	NAME		
1	BAT	I/O	**Battery Charger Output Terminal**. Connect to the positive terminal of the battery. Additionally, bypass BAT to PGND with a 10μF ceramic chip capacitor to keep the ripple voltage small.
2	SENSE	I	**Internal Sense Resistor**. Connect to external inductor.
3	PGND	P	**Power Ground**.
4	GNDSENS	I	**Ground Sense**. Connect this pin to the negative battery terminal. GNDSENS provides a Kelvin connection for PGND and must be connected to PGND schematically.
5	SW	O	**Switch Node Connection**. This pin connects to the drains of the internal main and synchronous power MOSFET switches. Connect to external inductor. Keep these PCB trace lengths as short and wide as possible to reduce EMI and voltage overshoot.

(1)I = input; O = output; P = power

PIN FUNCTIONS (continued)

PIN		TYPE(1)	DESCRIPTION
NO.	NAME		
6	$\overline{EN}$	I	**Chip Enable Input Pin**. Pulling the $\overline{EN}$ pin high places the CE3320 into a low power state where the BAT drain current drops to less than 3μA and the supply current is reduced to less than 50μA. For normal free running operation, pull the $\overline{EN}$ pin low.
7	$\overline{CHRG}$	I	**Open-Drain Charge Status Output**. When the battery is being charged, $\overline{CHRG}$ is pulled low by an internal N-channel MOSFET. When the charge current drops below the IDET threshold (set by the R_{IDET} programming resistor) for more than 5 milliseconds, the N-channel MOSFET turns off and a 30μA weak current source is connected from $\overline{CHRG}$ to ground. (This signal is latched and is reset by initiating a new charge cycle.) When the timer runs out or the input supply is removed, the current source will be disconnected and the $\overline{CHRG}$ pin is forced to a high impedance state. A temperature fault causes this pin to blink.
8	PV_{IN}	I	**Positive Supply Voltage Input**. This pin connects to the power devices inside the chip. V_{IN} ranges from 4V to 5.5V for normal operation. Operation down to the undervoltage lockout threshold is allowed with current limited wall adapters. Decouple with a 10μF or larger surface mounted ceramic capacitor.
9	V_{INSENS}	I	**Positive Supply Sense Input**. This pin connects to the inputs of all input comparators (UVL, V_{IN} to V_{BAT}). It also supplies power to the controller portion of this chip. When the BATSENS pin rises to within 30mV of $V_{INSENSE}$, the CE3320 enters sleep mode, dropping I_{IN} to 50μA. Tie this pin directly to the terminal of the PV_{IN} decoupling capacitor.
10	FAULT	I	**Battery Fault**. This pin is a logic high if a shorted battery is detected or if a temperature fault is detected. A temperature fault occurs with the temperature monitor circuit enabled and the thermistor temperature is either below 0°C or above 50°C (typical).

(1) I = input; O = output; P = power

PIN FUNCTIONS (continued)

11	NTC	I	**Input to the NTC (Negative Temperature Coefficient) Thermistor Temperature Monitoring Circuit**. Under normal operation, tie a thermistor from the NTC pin to the GNDSENS pin and a resistor of equal value from NTC to V_{IN}. When the voltage on this pin is above $0.74V_{IN}$ (Cold, 0°C) or below $0.29V_{IN}$ (Hot, 50°C), charging is disabled and the $\overline{CHRG}$ pin blinks. When the voltage on NTC comes back between $0.74V_{IN}$ and $0.29V_{IN}$, the timer continues where it left off and charging resumes. There is approximately 3°C of temperature hysteresis associated with each of the input comparators. If the NTC function is not used, connects the NTC pin to GNDSENS. This will disable all of the NTC functions. NTC should never be pulled above V_{IN}.
12	PROG	O	**Charge Current Program**. The R_{PROG} resistor connects from this pin to GNDSENS, setting the current: $$R_{PROG} = \frac{1.110K}{I_{BAT}(AMPS)}$$ where I_{BAT} is the high rate battery charging current.
13	IDET	O	**Charge Rate Detection Threshold**. Connecting a resistor, R_{IDET} to GNDSENS programs the charge rate detection threshold. If R_{IDET} = R_{PROG}, $\overline{CHRG}$ provides an $I_{BAT}/10$ indication. For other thresholds see the Applications Information section.
14	SS	O	**Soft-Start/Compensation**. Provides soft-start function and compensation for the float voltage control loop and compensation for the charge current control loop. Tie a soft-start/compensation capacitor between this pin and GNDSENS.
15	TIMER	O	**Timer Capacitor**. The timer period is set by placing a capacitor, C_{TIMER}, to GNDSENS. Set C_{TIMER} to: C_{TIMER} = Time (Hrs) • 0.0733(μF) where time is the desired charging time. Connect this pin to IDET to disable the timer. Connect this pin to GNDSENS to end battery charging when I_{BAT} drops below the IDET charge rate threshold.
16	BATSENS	I	**Battery Sense Input**. An internal resistor divider sets the final float voltage at this pin. The resistor divider is disconnected in sleep mode or when $\overline{EN}$ = H to reduce the battery drain current. Connect this pin to the positive battery terminal.
17	Exposed Pad(bottom)	P	**Ground**. This pin must be soldered to the PCB ground (PGND) for electrical contact and rated thermal performance. There is an internal electrical connection between the exposed pad and the PGND pin of the device. Do not use the Exposed Pad as the primary ground input for the device. PGND pin must be connected to ground at all times.

(1)I = input; O = output; P = power

■ ABSOLUTE MAXIMUM RATINGS

(unless otherwise specified, T_{opr}=25°C)(1)

PARAMETER		SYMBOL	RATINGS	UNITS
Input Voltage(2)	t<1ms，DC<1%	PV_{IN},$V_{INSENSE}$	V_{SS}-0.3~V_{SS}+7	V
	Steady State		V_{SS}-0.3~V_{SS}+6	
SW, SENSE, BAT, BATSENS, SS, FAULT, $\overline{CHRG}$, $\overline{EN}$, NTC, PROG, IDET, TIMER Voltage(2)			V_{SS}-0.3~V_{SS}+6	V
Output sink current		$I_{\overline{CHRG}}$	10	mA
Power Dissipation	QFN4x4-16	P_D	2.5	mW
Operating free air temperature range(3		T_{opr}	-40~85	°C
Operating Junction Temperature(4)		T_j	-40~125	°C
Storage Temperature Range		T_{stg}	-65~+125	°C
Soldering Temperature & Time		T_{solder}	260℃, 10s	
ESD rating(5)		Human Body Model - (HBM)	2	kV
		Machine Model- (MM)	200	V

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods my affect device reliability.

(2) All voltages are with respect to network ground terminal.

(3)The CE3320 is guaranteed to meet performance specifications from 0°C to 85°C. Specifications over the –40°C to 85°C operating temperature range are assured by design, characterization and correlation with statistical process controls.

(4)This IC includes overtemperature protection that is intended to protect the device during momentary overload. Junction temperature will exceed 125°C when overtemperature protection is active. Continuous operation above the specified maximum operating junction temperature may impair device reliability.

(5)ESD testing is performed according to the respective JESD22 JEDEC standard.

The human body model is a 100 pF capacitor discharged through a 1.5kΩ resistor into each pin. The machine model is a 200pF capacitor discharged directly into each pin.

■ RECOMMENDED OPERATING CONDITIONS

PARAMETER(1)	MIN	NOM	MAX	UNITS
Supply voltage at PV_{IN} and $V_{INSENSE}$	4.0		5.5	V
Charge current, I_{BAT}			2	A
Operating free air temperature range, T_{opr}	0		85	°C
Operating junction temperature range, T_j	0		125	°C

(1) The inherent switching noise voltage spikes should not exceed the absolute maximum rating on the SW pin. A tight layout minimizes switching noise.

■ ELECTRICAL CHARACTERISTICS

V_{IN}=5V, $V_{\overline{EN}}$=0V, R_{PROG}=549Ω, R_{IDET}=549Ω, T_{opr}=25℃, unless otherwise specified

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
POWER SUPPLIES						
Supply Voltage	V_{IN}	**(Note1)**	4		5.5	V
Supply Current	I_{IN}	PV_{IN} Connected to $V_{INSENSE}$, PROG and IDET Pins Open, Charger On			2	mA
		Shutdown, $\overline{EN}$= V_{IN}			50	μA
ENABLE						
$\overline{EN}$ Low-level Voltage	$V_{\overline{ENL}}$	V_{EN} Falling, Device ON			0.3	V
$\overline{EN}$ High-level Voltage	$V_{\overline{ENH}}$	V_{EN} Rising, Device Off	1.5		V_{IN}	V
$\overline{EN}$ Input Bias Current	$I_{(\overline{EN})}$	$\overline{EN}$=GNDSENS or $\overline{EN}$=V_{IN}		±0.01	±1	μA
BATTERY CHARGER						
Trickle Charge Threshold	V_{TRIKL}	V_{BAT} Rising	3.05	3.1	3.20	V
		V_{BAT} Falling	2.85	3.0	3.05	V
Trickle Charge Current	I_{TRIKL}	V_{BAT} = 2V	35	50	65	mA
Deglitch Time For Trickle Charge To Current Mode Charge Transition	$t_{DGL(TRIKL)}$			5		mS
Current Mode Charge Current	I_{BAT}	R_{PROG} = 549Ω, V_{BAT} =3.5V	1.8	2	2.2	A
		R_{PROG} = 1.10k, V_{BAT} =3.5V	0.9	1	1.1	A
		Shutdown, $\overline{EN}$= V_{IN}			±5	μA
PROG Pin Voltage	V_{PROG}	R_{PROG} = 549Ω,Current Mode		1.213		V
V_{BAT} Regulated Float Voltage	V_{FLOAT}	Measured from BATSENS to GNDSENS	4.158	4.2	4.242	V
IDET Pin Voltage	V_{IDET}	R_{IDET} = 549Ω		1.213		V
IDET Threshold	I_{IDET}	R_{IDET} = 549Ω	150	200	250	mA
Deglitch Time For IDET	$t_{DGL(IDET)}$	Both rising and falling, 2-mV over-drive, t_{RISE}, t_{FALL}= 100 ns		5		mS
Recharge Battery Threshold Voltage, V_{FLOAT} – V_{RECHRG}	V_{RECHRG}	V_{BAT} Falling	50	100	135	mV
Deglitch Time For Recharge	$t_{DGL(RECHRG)}$	V_{BAT} Falling Below V_{RECHRG},	4			mS
Recharge Time	t_{RECHRG}	Percent of Total Charge Time		50		%

■ ELECTRICAL CHARACTERISTICS(continued)

V_{IN}=5V, $V_{\overline{EN}}$=0V, R_{PROG}=549Ω, R_{IDET}=549Ω, T_{opr}=25℃, unless otherwise specified

STATUS OUTPUT						
$\overline{CHRG}$ Pin Weak Pull-Down Current	$I_{WPD-\overline{CHRG}}$	$V_{\overline{CHRG}}$=1V	15	30	50	μA
$\overline{CHRG}$ Pin Low-level Output Voltage	$V_{OL-\overline{CHRG}}$	$I_{\overline{CHRG}}$=5mA(sink current)		0.2	0.4	V
$\overline{CHRG}$ Pin Leakage Current	$I_{\overline{CHRG}-LEAK}$	When output FET is off, $V_{\overline{CHRG}}$=5V			1	μA
$\overline{CHRG}$ Pin Pulse Frequency	$f_{\overline{CHRG}-FLASH}$	Battery Temperature Fault, C_{TIMER}=0.1μF		1.5		Hz
$\overline{CHRG}$ Pin Pulse Width	$t_{\overline{CHRG}-PULSE}$	Battery Temperature Fault, C_{TIMER}=0.1μF		333		mS
FAULT Pin Low-level Output Voltage	$V_{OL-FAULT}$	1mA Load			0.4	V
FAULT Pin High-level Output Voltage	$V_{OH-FAULT}$	1mA Load	4.6			V
PROTECTION						
V_{IN} Undervoltage Lockout Voltage	V_{UVL}	V_{IN} Rising, Measured from $V_{INSENSE}$ to GNDSENS	2.7		2.82	V
V_{IN} Undervoltage Lockout Hysteresis	ΔV_{UVL}	Measured from $V_{INSENSE}$ to GNDSENS		100		mV
Soft-Start Ramp Current	I_{SS}	V_{BAT}< V_{FLOAT} – 100mV, V_{BAT} Across BATSENS and GNDSENS Pins	6	12.8	16	μA
Sleep-mode Entry Threshold, $V_{INSENSE}$ – $V_{BATSENS}$	V_{SLP}	$V_{INSENSE}$ Falling(Turn-Off) $V_{BATSENSE}$= 4V	15	30	60	mV
Sleep-mode Exit Hysteresis, $V_{INSENSE}$ – $V_{BATSENS}$	$V_{(SLP\_EXIT)}$	$V_{INSENSE}$ Rising (Turn-On), $V_{BATSENSE}$= 4V	200	250	300	mV
Deglitch time for $V_{INSENSE}$ rising above V_{SLP} + $V_{(SLP\_EXIT)}$		Rising voltage, 2-mV over drive, t_{RISE}=100 nS		5		mS
Battery OVP Threshold Voltage	$V_{(BOVP)}$	$V_{BATSENSE}$ threshold over V_{FLOAT} to turn off charger during charge	1.02x V_{FLOAT}	1.05x V_{FLOAT}	1.08x V_{FLOAT}	V
VB_{OVP} Hysteresis	$V_{(BOVP-HYS)}$	Lower limit for $V_{BATSENSE}$ falling from above $V_{(BOVP)}$		1		% of V_{FLOAT}
Battery Short Circuit Threshold Voltage	$V_{(BATSHRT)}$	$V_{BATSENSE}$ rising, 100 mV hysteresis		1.8		V
Battery Short Circuit Current	$I_{(BATSHRT)}$		35	50	65	mA

■ ELECTRICAL CHARACTERISTICS(continued)

V_{IN}=5V, $V_{\overline{EN}}$=0V, R_{PROG}=549Ω, R_{IDET}=549Ω, T_{opr}=25℃, unless otherwise specified

Safety Timer Accuracy	t_{TIMER}	C_{TIMER} = 0.1μF		±10		%
Low-Battery Trickle Charge Time	t_{TRIKL}	Percent of Total Charge Time, V_{BAT}< 3.1V, Measured Using BATSENS and GNDSENS Pins		25		%
Cycle by Cycle Current Limit	I_{CL}			3.5		A
Thermal Shutdown	T_{TSD}			160		°C
Thermal Shutdown Hysteresis	T_{HYS}			10		°C
OSCILLATOR						
Oscillator Frequency	f_{osc}		1.3	1.5	1.7	MHz
Max Duty Cycle	D				100	%
POWER SWITCH						
P-CH MOSFET On Resistance	R_{PFET}	Measured from PV_{IN} to SW		125		mΩ
N-CH MOSFET On Resistance	R_{NFET}	Measured from SW to PGND		120		mΩ
P- CHMOSFET Leakage Current	I_{LKG}	$V_{\overline{EN}}=V_{IN}$=5V, V_{SW}=0V		±0.01	±1	μA
N- CHMOSFET Leakage Current		$V_{\overline{EN}}=V_{IN}=V_{SW}$=5V		±0.01	±1	μA
Reverse Leakage Current (Measured from SW to V_{IN})	$I_{REV-LEAK}$	$\overline{EN}$=H or L, V_{IN}=0V, V_{SW}=5V			1	μA
BATTERY-PACK NTC MONITOR						
NTC Pin Hot Temperature Fault Threshold	V_{HOT}	From NTC to GNDSENS Pin Falling Threshold		0.29 $V_{INSENSE}$		%
		From NTC to GNDSENS Pin Rising Threshold		0.30 $V_{INSENSE}$		%
NTC Pin Cold Temperature Fault Threshold	V_{COLD}	From NTC to GNDSENS Pin Rising Threshold		0.74 $V_{INSENSE}$		%
		From NTC to GNDSENS Pin Falling Threshold		0.72 $V_{INSENSE}$		%
NTC Disable Threshold	$V_{(NTCDIS)}$	From NTC to GNDSENS Pin Falling Threshold	0.015 $V_{INSENSE}$	0.020 $V_{INSENSE}$	0.025 $V_{INSENSE}$	%
NTC Disable Hysteresis	$\Delta V_{(NTCDIS-HYS)}$	From NTC to GNDSENS Pin		0.010 $V_{INSENSE}$		%
Deglitch time for NTC change				5		mS

Note1: Operation with current limited wall adapters is allowed down to the undervoltage lockout threshold.

■ TYPICAL APPLICATION CIRCUITS

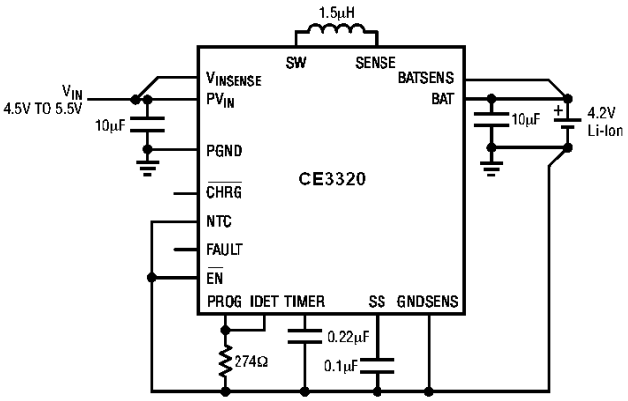


Figure1 Typical Application Circuit

■ BLOCK DIAGRAM

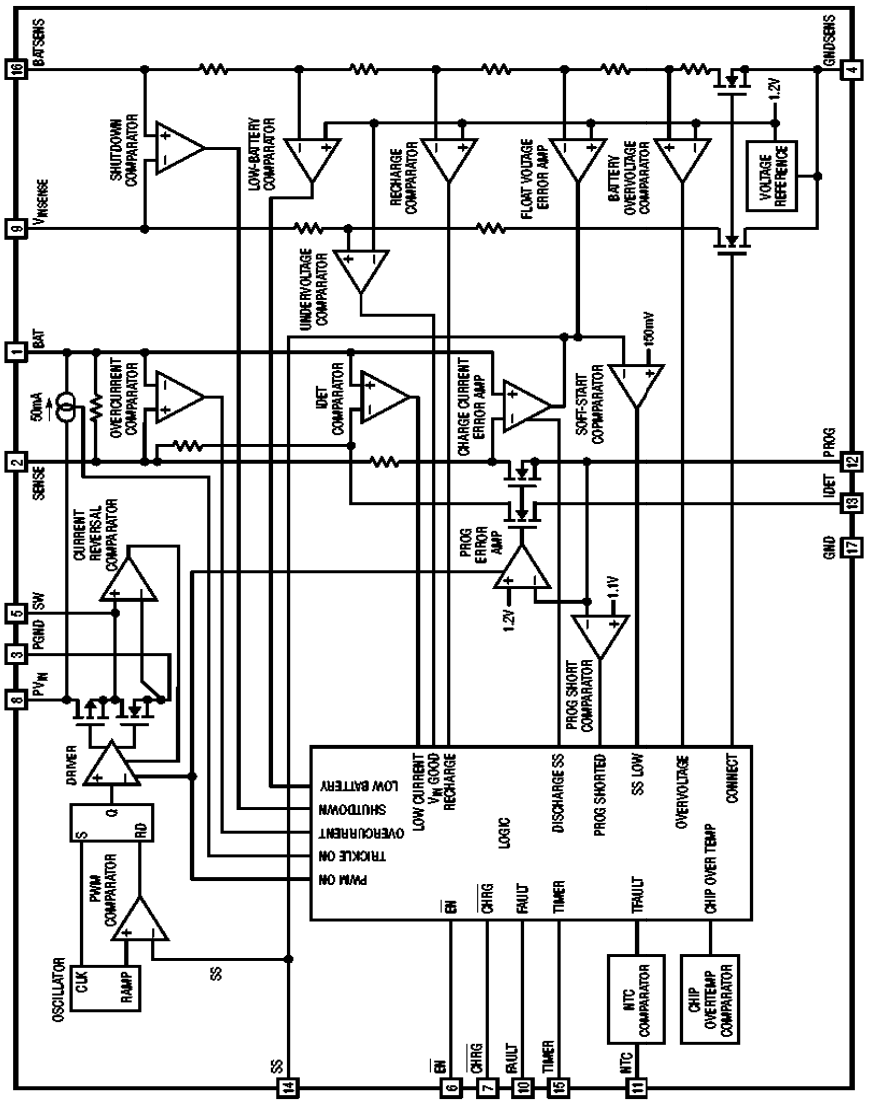


Figure 2 Functional Block Diagram

■ OPERATION

The CE3320 is a constant current, constant voltage Li-Ion battery charger based on a synchronous buck architecture. Low power dissipation makes continuous high rate (2A) battery charging practical. The battery DC charge current is programmed by a resistor R_{PROG} (or a DAC output current) at the PROG pin. The final battery float voltage is internally set to 4.2V.

Charging begins when the V_{IN} voltage rises above the UVLO level (approximately 2.75V), V_{IN} is 250mV greater than the battery voltage and $\overline{EN}$ is low. At the beginning of the charge cycle, if the battery voltage is less than the trickle charge threshold, 3V, the charger goes into trickle charge mode and delivers approximately 50mA to the battery using a linear charger. If the battery voltage stays low for more than one quarter of the charge time, the battery is considered faulty, the charge cycle is terminated and the FAULT pin produces a logic high output.

When the battery voltage exceeds the trickle charge threshold, the low rate linear charger is turned off and the high rate PWM charger ramps up (based on the SS pin capacitance) reaching its full-scale constant current (set via the PROG pin). When the battery approaches the float voltage, the charge current will start to decrease. When the charge current drops below the charge rate detection threshold(set via the IDET pin) for more than 5ms, an internal comparator turns off the internal pull-down N-channel MOSFET at the $\overline{CHRG}$ pin, and connects a weak current source (30μA typical) to ground to indicate a near end-of-charge condition.

Total charge time is set by an external capacitor connected to the timer pin. After time out occurs, the charge cycle is terminated and the $\overline{CHRG}$ pin is forced to a high impedance state. To restart the charge cycle, remove and reapply the input voltage, or momentarily shut the charger down via the $\overline{EN}$ pin. Also, a new charge cycle will begin if the battery voltage drops below the recharge threshold voltage(100mV below the float voltage). A recharge cycle lasts only one-half of the normal charge time.

A negative temperature coefficient (NTC) thermistor located close to the battery pack can be used to monitor battery temperature and suspend charging when battery temperature is out of the 0°C to 50°C window. A temperature fault drives the FAULT pin high and makes the $\overline{CHRG}$ pin blink. When the input voltage (V_{IN}) is present, the charger can be shut down by pulling the $\overline{EN}$ pin up.

IDET Blanking

The IDET comparator provides an end-of-charge indication by sensing when battery charge current is less than the IDET threshold. To prevent a false end-of-charge indication from occurring during soft-start, this comparator is blanked until the battery voltage approaches the float voltage.

Charge Safety Timer

While monitoring the charge cycle, the CE3320 utilizes a charge safety timer to help identify damaged cells and to ensure that the cell is charged safely. Operation is as follows: upon initiating a charging cycle, the CE3320 charges the cell at a 50mA charge current until V_{BAT}> 3.1V(typ). If the cell voltage falls to the trickle threshold of 3.1V(typ) before the safety timer expires, the cell is assumed to be damaged and the charge cycle terminates. If the cell voltage exceeds 3.1V prior to the expiration of the timer, the charge cycle proceeds into fast charge. Two time out periods of 45 minutes for Trickle Charge mode and 3 hours for Constant Voltage mode.

Mode	Time
Trickle Charge (TC) Time Out	45 minutes
Constant Voltage (CV) Mode Time Out, I_{BAT}<I_{IDET}	3 hours

Table 1. Summary for a 0.22μF Ceramic Capacitor Used for the Timer Capacitor

The TIMER pin is driven by a constant current source and will provide a linear response to increases in the timer capacitor value. Thus, if the timer capacitor were to be doubled from the nominal 0.1μF value, the time-out periods would be doubled. If the programmable timer function is not needed, it can be disabled by terminating the TIMER pin to IDET pin.

The TIMER pin should not be left floating or unterminated, as this will cause errors in the internal timer control circuit. The constant current provided to charge the timer capacitor is very small, and this pin is susceptible to noise and changes in capacitance value. Therefore, the timer capacitor should be physically located on the printed circuit board layout as close as possible to the TIMER pin. Since the accuracy of the internal timer is dominated by the capacitance value, a 10% tolerance or better ceramic capacitor is recommended. Ceramic capacitor materials, such as X7R and X5R types, are a good choice for this application.

Automatic Battery Recharge

After the charge cycle is completed and if both the battery and the input power supply (wall adapter) are still connected, a new charge cycle will begin if the battery voltage drops below 4.1V due to self-discharge or external loading. This will keep the battery near maximum capacity at all times without manually restarting the charge cycle.

In some applications such as battery charging in GPRS cell phones, large load current transients may cause battery voltage to momentarily drop below the recharge threshold. To prevent these transients from initiating are charge cycle when it is not needed, the output of the recharge comparator is digitally qualified. Only if the battery voltage stays below the recharge threshold for at least 4ms will battery recharging occur. (GPRS qualification is available even if time out is disabled.)

Battery Charging Profile

Figure 3 illustrates the entire battery charging profile, which consists of three phases:

1. Preconditioning-Current Mode (Trickle) Charge - Linear Mode.
2. Constant-Current Mode(Fast) Charge - Switching Mode.
3. Constant-Voltage Mode (Taper) Charge - Switching Mode.

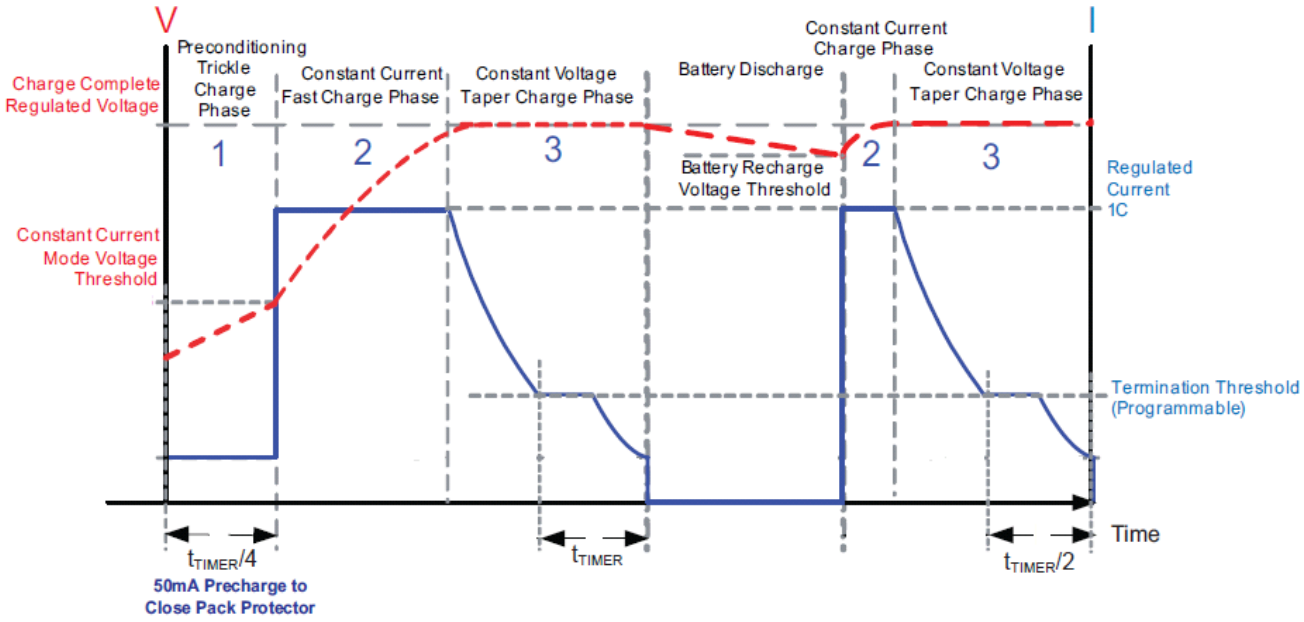


Figure 3: Charging Current and Battery Voltage vs Time

Undervoltage Lockout and Automatic Shutdown

Internal undervoltage lockout circuits monitor V_{IN} and keep the charger circuits shut down until V_{IN} rises above the undervoltage lockout threshold. The UVLO has a built-in hysteresis of 100mV. Furthermore, to protect against reverse current, the charger also shuts down if V_{IN} is less than V_{BAT}. If automatic shutdown is tripped, V_{IN} must increase to more than 250mV above V_{BAT} to allow charging.

Overvoltage, Chip Overtemperature and Short-Circuit Current Protection

The CE3320 includes overvoltage, chip overtemperature and several varieties of short-circuit protection.

A comparator turns off both chargers (high rate and trickle) if battery voltage exceeds the float voltage by approximately 5%. This may occur in situations where the battery is accidentally disconnected while battery charging is underway The CE3320 will resume normal charging operation after the over-voltage condition is removed. During an over-voltage event, the status indication LED will report a system fault.

A comparator continuously monitors on-chip temperature and will shut off the battery charger when chip temperature exceeds approximately 160°C. Battery charging will be enabled again when temperature drops to approximately150°C.

Short-circuit protection is provided in several different ways. First, a hard short on the battery terminals will cause the charge to enter trickle charge mode, limiting charge current to the trickle charge current (typically 50mA). Second, PWM charging is prevented if the high rate charge current is programmed far above the 2A maximum recommended charge current (via the PROG pin). Third, an overcurrent comparator monitors the peak inductor current.

■ TYPICAL PERFORMANCE CHARACTERISTICS

(T_{opr}=25℃, unless otherwise specified, Test Figure1 above)

Oscillator Frequency vs V_{IN}Oscillator

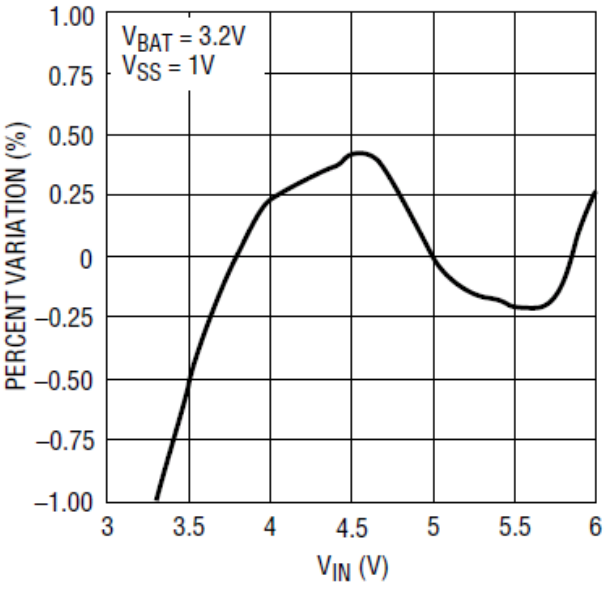


Figure 4

Frequency vs Temperature

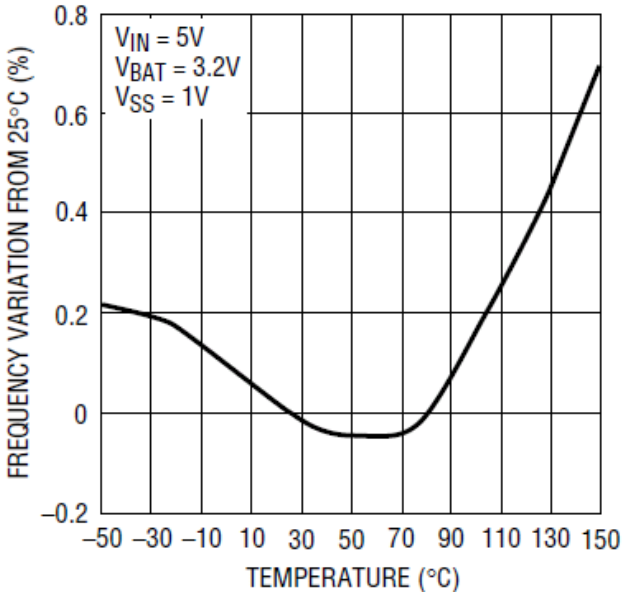


Figure5

Power Loss vs V_{BAT} Charging (PWM Mode)

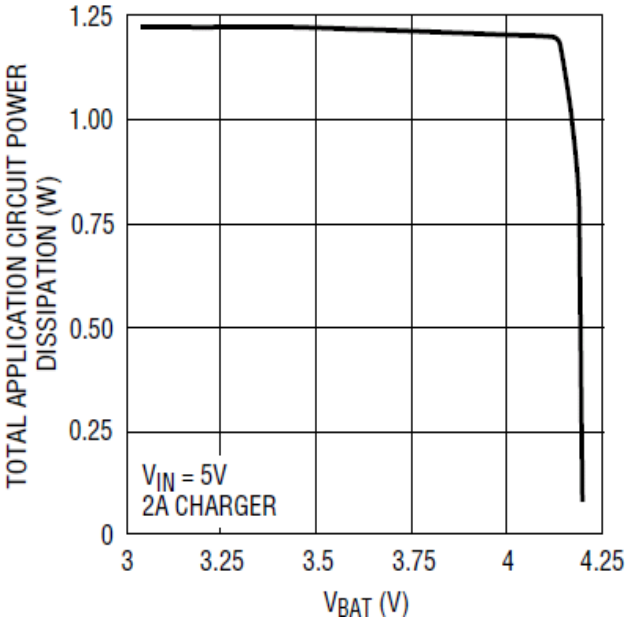


Figure 6

Dissipation of Figure 24 Circuit vs I_{BAT}

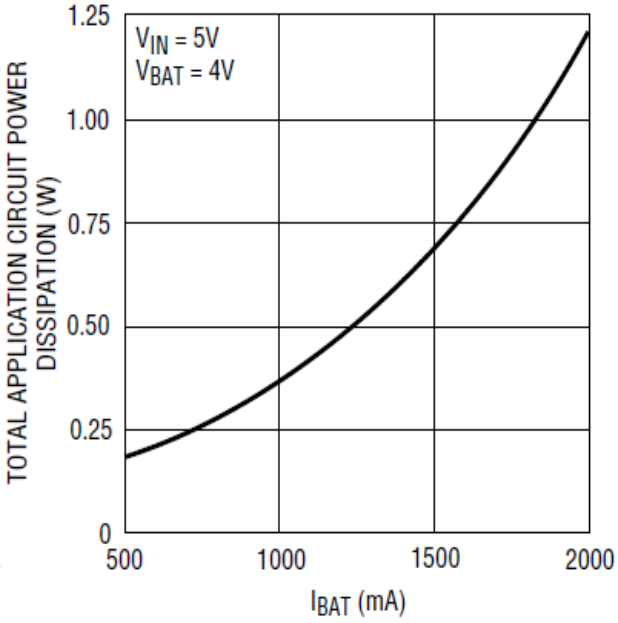


Figure7

Dissipation of Figure 24 Circuit vs V_{IN}

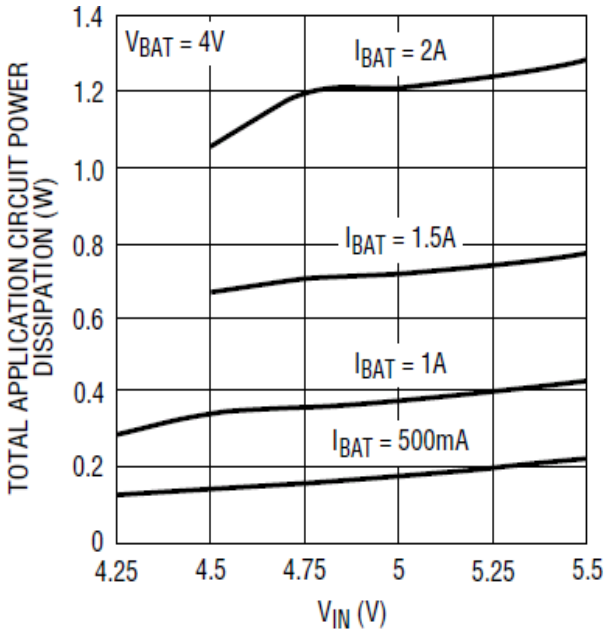


Figure 8

Trickle Charge Current vs V_{BAT}

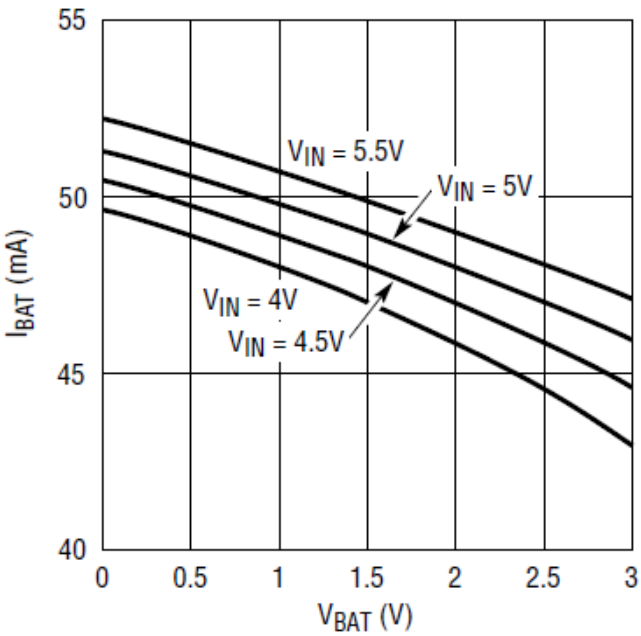


Figure9

PROG Pin Characteristic(V_{PROG}vs I_{PROG})

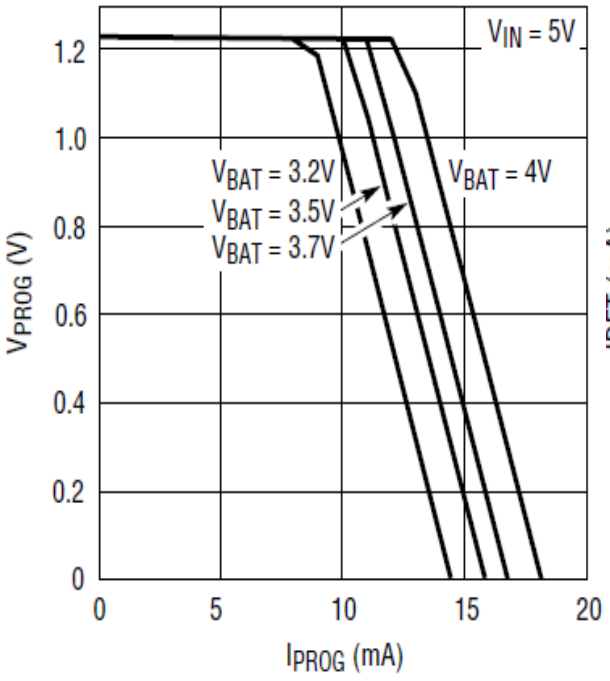


Figure 10

IDET Threshold vs R_{IDET} for R_{PROG} = 549Ω

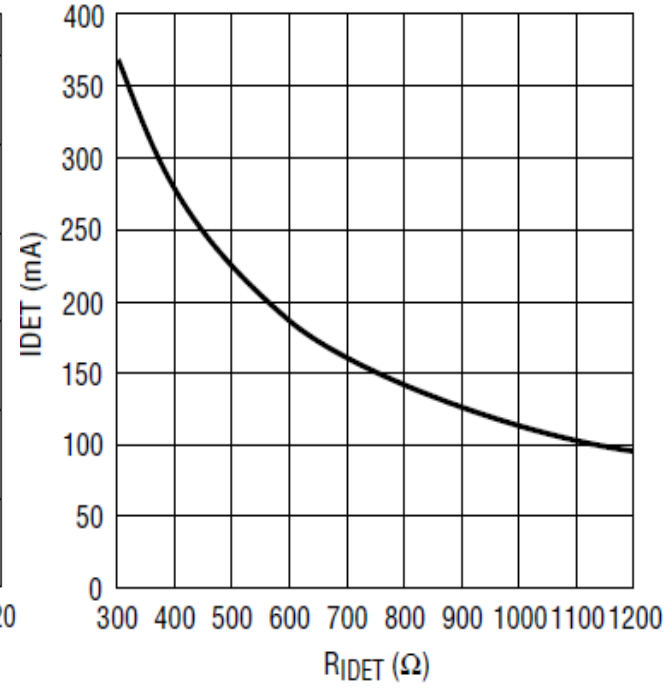


Figure 11

Output Charging Characteristic Showing Constant Current and Constant Voltage

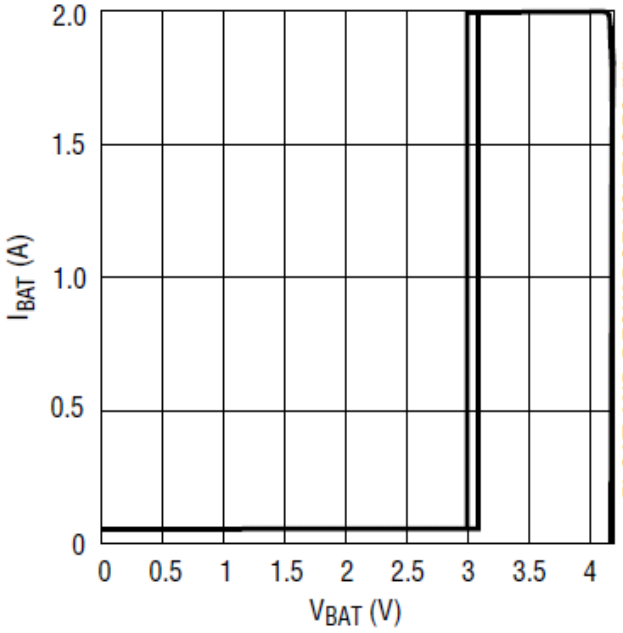


Figure 12

V_{FLOAT} and Recharge Battery OperationThreshold Voltage vs Temperature

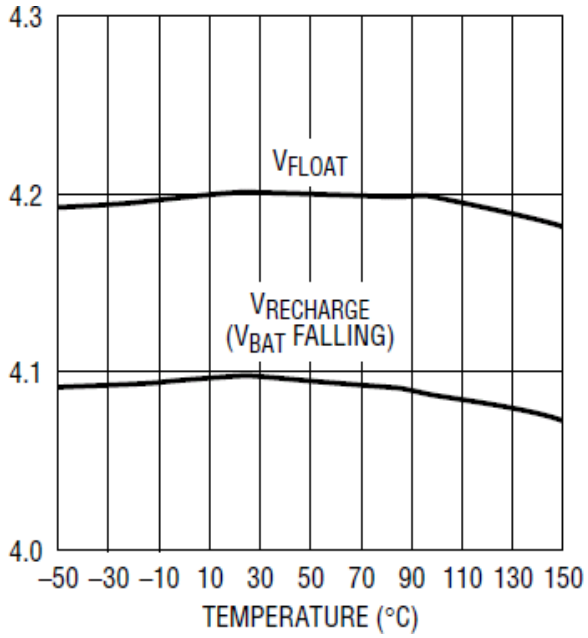


Figure 13

$\overline{\text{CHRG}}$ Pin Temperature Fault Behavior (Detail)

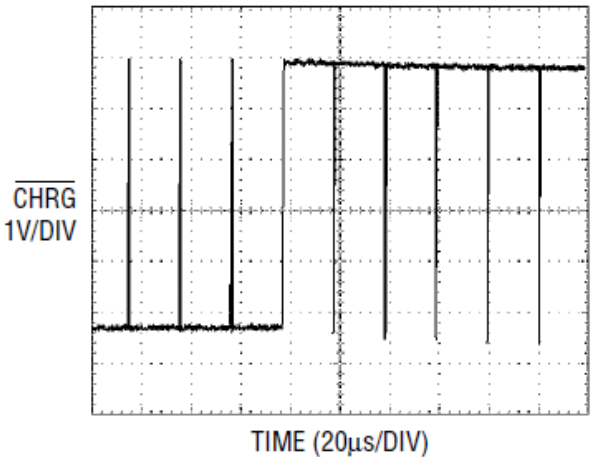


Figure 14

Soft-Start (PWM Mode)

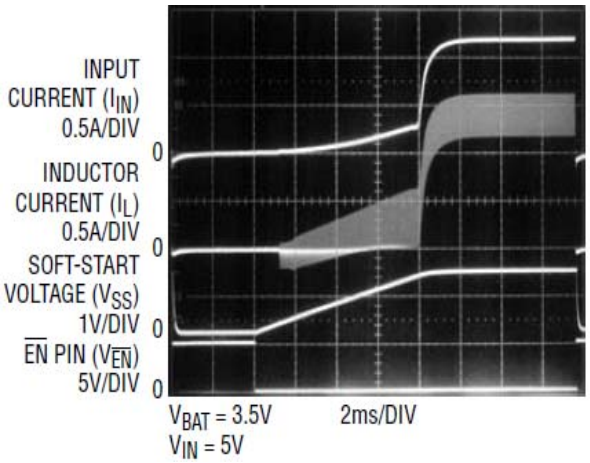


Figure 15

■ APPLICATION INFORMATION

Because of the high integration in the CE3320 IC, the application circuit based on this Synchronous Buck Li-Ion Charger IC is rather simple. Only low profile external components need to be selected for the targeted application specifications.

Soft-Start and Compensation Capacitor Selection

The CE3320 has a low current trickle charger and a PWM-based high current charger. Soft-start is used whenever the high rate charger is initially turned on, preventing high start-up current. Soft-start ramp rate is set by the internal 12.8µA pull-up current and an external capacitor. The control range on the SS pin is approximately 0.3V to1.6V. With a 0.1µF capacitor, the time to ramp up to maximum duty cycle is approximately 10ms.

The external capacitor on the SS pin also sets the compensation for the current control loop and the float voltage control loop. A minimum capacitance of 10nF is required.

Charge Current and IDET Programming

The CE3320 has two different charge modes. If the battery is severely depleted (battery voltage less than 2.9V) a 50mA trickle current is initially used. If the battery voltage is greater than the trickle charge threshold, high rate charging is used. This higher charge current is programmable and is approximately 915 times the current delivered by the PROG pin. This current is usually set with an external resistor from PROG to GNDSENS, but it may also be set with a current output DAC connected to the PROG pin. The voltage on the PROG pin is nominally 1.213V.

For 2A charge current:

$$R_{IDET} = \frac{915 \bullet 1.213V}{2A} \cong 554.9\Omega$$

The IDET threshold (a charge current threshold used to determine when the battery is nearly fully charged) is programmed in much the same way as the PROG pin, except that the IDET threshold is 91.5

times the current delivered by the IDET pin. This current is usually set with an external resistor from IDET to GNDSENS, but it may also be set with a current output DAC. The voltage on the IDET pin is nominally 1.213V.

For 200mA IDET current (corresponding to C/10 for a 2AHr battery):

$$R_{IDET} = \frac{91.5 \bullet 1.213V}{0.2A} \cong 554.9\Omega$$

1.10kΩ programs approximately 100mA and 274Ω approximately 400mA.

For applications where IDET is set to one tenth of the high rate charge current, and slightly poorer charger current and IDET threshold accuracy is acceptable, the PROG and IDET pins may be tied together and a single resistor, R1,can program both (Figure 16).

$$R1 = \frac{457.5 \bullet 1.213}{I_{CHARGE}}$$

and

$$IDET = \frac{I_{CHARGE}}{10}$$

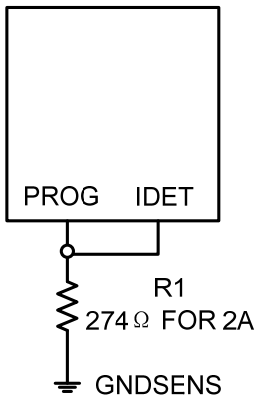


Figure 16. Programming Charge Current and IDET Threshold with a Single Resistor

The equations for calculating R1 (used in single resistor programming) differ from the equations for calculating R_{PROG} and R_{IDET} (2-resistor programming) and reflect the fact that the current from both the IDET and PROG pins must flow through a single resistor R1 when a single programming resistor is used.

Charge Termination

Battery charging may be terminated several different ways, depending on the connections made to the TIMER pin. For time-based termination, connect a capacitor between the TIMER pin and GNDSENS (C_{TIMER} = Time (Hrs) x 0.0733μF). Charging may be terminated when charge current drops below the IDET threshold by tying TIMER to GNDSENS. Finally, charge termination may be defeated by tying TIMER to IDET. In this case, an external device can terminate charging by pulling the $\overline{EN}$ pin high.

$\overline{CHRG}$ Status Output Pin

When a charge cycle starts, the $\overline{CHRG}$ pin is pulled to ground by an internal N-channel MOSFET which is capable of driving an LED. When the charge current drops below the end-of-charge (IDET) threshold for at least 4ms, and the battery voltage is close to the float voltage, the N-channel MOSFET turns off and

a weak 30μA current source to ground is connected to the CHRG pin. This weak pull down remains until the charge cycle ends. After charging ends, the pin will become high impedance. By using two different value resistors, a microprocessor can detect three states from this pin (charging, end-of-charge and charging stopped). See Figure 17.

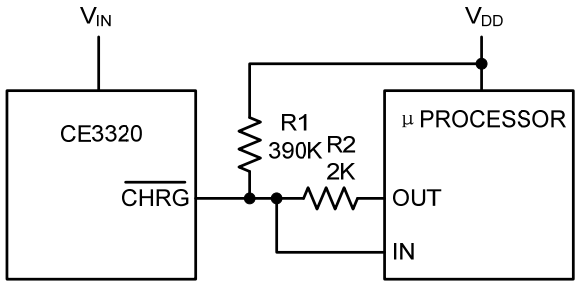


Figure 17. Microprocessor Interface

To detect the charge mode, force the digital output pin, OUT, high and measure the voltage on the $\overline{CHRG}$ pin. The N-channel MOSFET will pull the pin low even with a 2k pull-up resistor. Once the charge current drops below the end-of-charge threshold, the N-channel MOSFET is turned off and a 30μA current source is connected to the $\overline{CHRG}$ pin. The IN pin will then be pulled high by the 2k resistor connected to OUT. Now force the OUT pin into a high impedance state, the current source will pull the pin low through the 390k resistor. When charging stops, the $\overline{CHRG}$ pin changes to a high impedance state and the 390k resistor will then pull the pin high to indicate charging has stopped.

Battery Temperature Detection

When battery temperature is out of range (either too hot or too cold)， charging is temporarily halted and the FAULT pin is driven high. In addition, if the battery is still charging at a high rate (greater than the IDET current) when a temperature fault occurs, the $\overline{CHRG}$ pin NMOS turns on and off at approximately 50kHz, alternating between a high and low duty factor at an approximate rate of 1.5Hz (Figure 18).

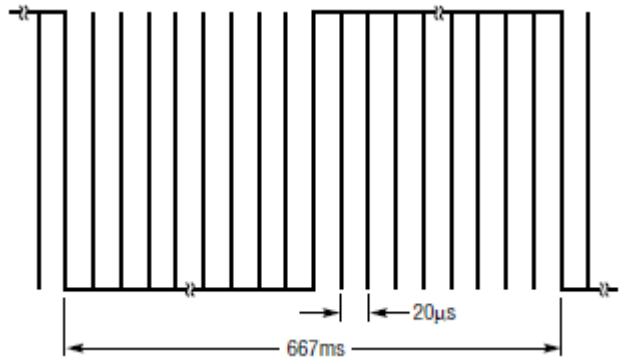


Figure 18. $\overline{CHRG}$ Temperature Fault Waveform

This provides a low rate visual indication (1.5Hz) when driving an LED from the $\overline{CHRG}$ pin while providing a fast temperature fault indication (20μseconds typical) to a microprocessor by tying the $\overline{CHRG}$ pin to an interrupt line. Serrations within this pulse are typically 500ns wide.

The battery temperature is measured by placing a negative temperature coefficient (NTC) thermistor close to the battery pack. To use this feature, connect the NTC thermistor, R_{NTC}, between the NTC pin and GNDSENS and the resistor, R_{NOM}, from the NTC pin to $V_{INSENSE}$. R_{NOM} should be a 1% resistor with a

value equal to the value of the chosen NTC thermistor at 25°C. The CE3320 goes into hold mode when the resistance, R_{HOT}, of the NTC thermistor drops to 0.41 times the value of R_{NOM}. For instance for R_{NTC} = 10k. (The value for a Vishay NTHS0603N02N1002J thermistor at 25°C) hold occurs at approximately 4.1k, which occurs at 50°C. The hold mode freezes the timer and stops the charge cycle until the thermistor indicates a return to a valid temperature. As the temperature drops, the resistance of the NTC thermistor rises. The CE3320 is designed to go into hold mode when the value of the NTC thermistor increases to 2.82 times the value of R_{NOM}. This resistance is R_{COLD}. For the Vishay 10k thermistor, this value is 28.2k, which corresponds toapproximately 0°C. The hot and cold comparators each have approximately 3°C of hysteresis to prevent oscillation about the trip point. Grounding the NTC pin disables the NTC function.

Thermistors

The CE3320 NTC trip points were designed to work with thermistors whose resistance temperature characteristics follow Vishay Dale's "R-T Curve 2." However, any thermistor whose ratio of R_{COLD} to R_{HOT} is about 7 will also work (Vishay Dale R-T Curve 2 shows a ratio of R_{COLD} to R_{HOT} of 2.815/0.4086 = 6.89).

Power conscious designs may want to use thermistors whose room temperature value is greater than 10k. Vishay Dale has a number of values of thermistor from 10k to 100k that follow the "R-T Curve 1." Using these as indicated in the NTC Thermistor section will give temperature trip points of approximately 3°C and 47°C, a delta of 44°C.This delta in temperature can be moved in either direction by changing the value of R_{NOM} with respect to R_{NTC}.

Increasing R_{NOM} will move the trip points to higher temperatures. To calculate R_{NOM} for a shift to lower temperature for example, use the following equation:

$$R_{NOM} = \frac{R_{COLD}}{2.815} \bullet R_{NTC} \text{ at } 25℃$$

where R_{COLD} is the resistance ratio of R_{NTC} at the desired cold temperature trip point. If you want to shift the trip points to higher temperatures, use the following equation:

$$R_{NOM} = \frac{R_{HOT}}{0.4086} \bullet R_{NTC} \text{ at } 25℃$$

where R_{HOT} is the resistance ratio of R_{NTC} at the desired hot temperature trip point.

Here is an example using a 100k R-T Curve 1 thermistor from Vishay Dale. The difference between trip points is 44°C, from before, and we want the cold trip point to be 0°C, which would put the hot trip point at 44°C. The R_{NOM} needed is calculated as follows:

$$R_{NOM} = \frac{R_{COLD}}{2.815} \bullet R_{NTC} \text{ at } 25℃$$

$$= \frac{3.266}{2.815} \bullet 100K = 116K$$

The nearest 1% value for R_{NOM} is 115k. This is the value used to bias the NTC thermistor to get cold and hot trip points of approximately 0°C and 44°C respectively. To extend the delta between the cold and hot trip points a resistor, R1, can be added in series with R_{NTC} (see Figure 19).

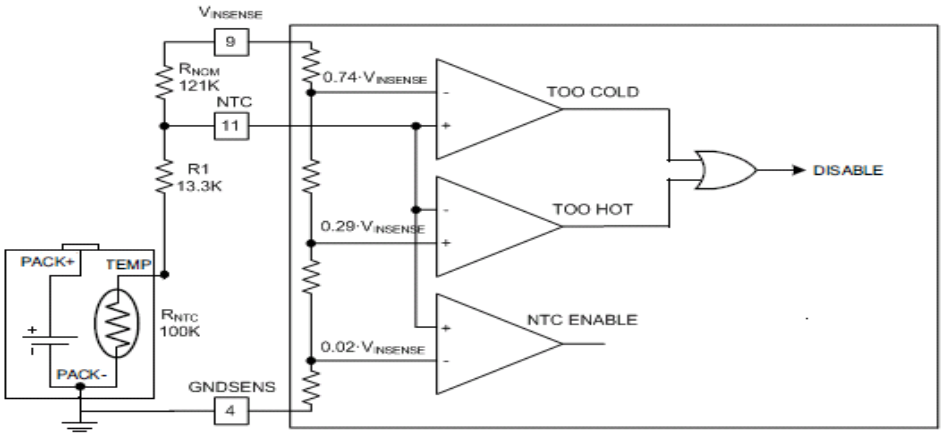


Figure 19. Extending the Delta Temperature

The values of the resistors are calculated as follows:

$$R_{NOM} = \frac{R_{COLD} - R_{HOT}}{2.815 - 0.4086}$$

$$R1 = \frac{0.4086}{2.815 - 0.4086} \bullet (R_{COLD} - R_{HOT}) - R_{HOT}$$

where R_{NOM} is the value of the bias resistor, R_{HOT} and R_{COLD} are the values of R_{NTC} at the desired temperature trip points. Continuing the example from before with a desired hot trip point of 50°C:

$$R_{NOM} = \frac{R_{COLD} - R_{HOT}}{2.815 - 0.4086} = \frac{100K \bullet (3.2636 - 0.3602)}{2.815 - 0.4086}$$

=120.8K, 121K is nearest 1%

$$R1 = 100K \bullet \left(\frac{0.4086}{2.815 - 0.4086} \bullet (3.266 - 0.3602) - 0.3602\right)$$

=13.3k, 13.3k is nearest 1%

The final solution is as shown if Figure 19 where R_{NOM} =121k, R1 = 13.3k and R_{NTC} = 100k at 25°C.

Charge Status Output

The CE3320 provides battery charge status via two status pins ($\overline{CHRG}$ and FAULT). $\overline{CHRG}$ pin is internally connected to an N-channel open drain MOSFET. FAULT pin is CMOS output, which can source or sink current. The status pins can indicate the following conditions:

Conditions	$\overline{CHRG}$	FAULT
Preconditioning-Current Mode (Trickle) Charge	ON	L
Preconditioning time out, V_{BAT}<3.1V	High impedance	H
Constant-Current Mode (Fast) Charge	ON	L
Constant-Voltage Mode (Taper) Charge, I_{BAT}>I_{IDET}	ON	L
End-of-Charge (IDET)	Connected a weak current source (30μA typical) to ground	L

Charge Stopped	High impedance	L
V_{IN} Undervoltage Lockout Mode	High impedance	L
Sleep Mode (V_{IN}< V_{SLP})	High impedance	L
No battery with Charge Enabled	FLASH Rate depends on output capacitance	L
No battery with Charge Enabled and safety timer disabled	FLASH Rate depends on output capacitance	L
Fault Condition (Battery Too Hot/Too Cold)	FLASH 1.5Hz, 50% Duty Cycle	H
Fault Condition (Battery Short Circuit)	FLASH 1.5Hz, 50% Duty Cycle	H
Fault Condition (Battery Overvoltage)	Connected a weak current source (30μA typical) to ground	L

Table 2. $\overline{\text{CHRG}}$ and FAULT Status Indicator

These status pins can be used to communicate to the host processor or drive LEDs.

The LEDs should be biased with as little current as necessary to create reasonable illumination, therefore, a ballast resistor should be placed between the LED cathode and the $\overline{\text{CHRG}}$ pin. LED current consumption will add to the overall thermal power budget for the device package, hence it is good to keep the LED drive current to a minimum 2mA should be sufficient to drive most low cost red or green LEDs. It is not recommended to exceed 10mA for driving an individual status LED. The required ballast resistor values can be estimated using the following formula:

$$R_{BALLAST} = \frac{V_{IN} - V_{F(LED)}}{I_{LED}}$$

Example:

$$R_{BALLAST} = \frac{5.0V - 2.0V}{2mA} = 1.5K\Omega$$

Note: Red LED forward voltage (V_F) is typically 2.0V@ 2mA.

Input and Output Capacitors Selection

The CE3320 uses a synchronous buck regulator to provide high battery charging current. A 10μF chip ceramic capacitor is recommended for both the input and output capacitors, because it provides low ESR and ESL and can handle the high RMS ripple currents. However, some high Q capacitors may produce high transients due to self-resonance under some start-up conditions, such as connecting the charger input to a hot power source.

EMI considerations usually make it desirable to minimize ripple current in the battery leads, and beads or inductors may be added to increase battery impedance at the 1.5MHz switching frequency. Switching ripple current splits between the battery and the output capacitor depending on the ESR of the output capacitor and the battery impedance. If the ESR of the output capacitor is 0.1Ω and the battery impedance is raised to 2Ω with a bead or inductor, only 5% of the ripple current will flow in the battery. Similar techniques may also be applied to minimize EMI from the input leads.

Inductor Selection

A high (1.5MHz) operating frequency was chosen for the buck switcher in order to minimize the size of the inductor. However, take care to use inductors with low core losses at this frequency. A good choice is the IHLP-2525AH-01from Vishay Dale.

To calculate the inductor ripple current:

$$\Delta I_L = \frac{V_{BAT} - \frac{{V_{BAT}}^2}{V_{IN}}}{L \bullet f}$$

where V_{BAT} is the battery voltage, V_{IN} is the input voltage, L is the inductance and f is the PWM oscillator frequency (typically 1.5MHz). Maximum inductor ripple current occurs at maximum V_{IN} and V_{BAT} = V_{IN}/2.

Peak inductor current will be:

$$I_{PK} = I_{BAT} + 0.5 \bullet \Delta I_L$$

where I_{BAT} is the maximum battery charging current.

When sizing the inductor make sure that the peak current will not exceed the saturation current of the inductors. Also, ΔI_L should never exceed 0.4(I_{BAT}) as this may interfere with proper operation of the output short-circuit protection comparator. 1.5μH provides reasonable inductor ripple current in a typical application. With 1.5μH and 2A charge current:

$$\Delta I_L = \frac{2.85V - \frac{2.85V^2}{5.5V}}{1.5\mu H \bullet 1.5MHz} = 0.61A_{P-P}$$

and

$$I_{PK} = 2.31A$$

Remote Sensing

For highest float voltage accuracy, tie GNDSENS and BATSENS directly to the battery terminals. In a similar fashion, tie BAT and PGND directly to the battery terminals. This eliminates IR drops in the GNDSENS and BATSENS lines by preventing charge current from flowing in them.

Operation with a Current Limited Wall Adapter

Wall adapters with or without current limiting may be used with the CE3320, however, lowest power dissipation battery charging occurs with a current limited wall adapter. To use this feature, the wall adapter must limit at a current smaller than the high rate charge current programmed into the CE3320. For example, if the CE3320 is programmed to charge at 2A, the wall adapter current limit must be less than 2A.

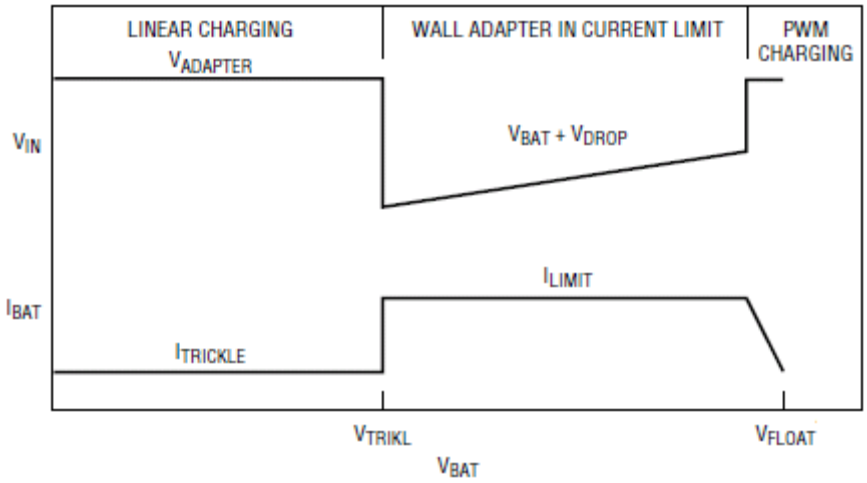


Figure 20. Charging Characteristic

To understand operation with a current limited wall adapter, assume battery voltage, V_{BAT}, is initially below V_{TRIKL}, the trickle charge threshold (Figure 20). Battery charging begins at approximately 50mA, well below the wall adapter current limit so the voltage into the CE3320 (V_{IN}) is the wall adapter's rated output voltage ($V_{ADAPTER}$). Battery voltage rises eventually reaching V_{TRIKL}. The linear charger shuts off, the PWM (high rate) charger turns on and a soft-start cycle begins. Battery charging current rises during the soft-start cycle causing a corresponding increase in wall adapter load current.

When the wall adapter reaches current limit, the wall adapter output voltage collapses and the CE3320 PWM charger duty cycle ramps up to 100% (the topside PMOS switch in the CE3320 buck regulator stays on continuously). As the battery voltage approaches V_{FLOAT}, the float voltage error amplifier commands the PWM charger to deliver less than I_{LIMIT}. The wall adapter exits current limit and the V_{IN} jumps back up to $V_{ADAPTER}$.

Battery charging current continues to drop as the V_{BAT} rises, dropping to zero at V_{FLOAT}. Because the voltage drop in the CE3320 is very low when charge current is highest, power dissipation is also very low.

Thermal Calculations (PWM and Trickle Charging)

The CE3320 operates as a linear charger when conditioning (trickle) charging a battery and operates as a high rate buck battery charger at all other times. Power dissipation should be determined for both operating modes.

For linear charger mode: $P_D = (V_{IN} – V_{BAT}) \bullet I_{TRIKL} + V_{IN} \bullet I_{IN}$, where I_{IN} is V_{IN} current consumed by the IC.

Worst-case dissipation occurs for V_{BAT} = 0, maximum V_{IN}, and maximum quiescent and trickle charge current. For example with 5.5V maximum input voltage and 65mA worst case trickle charge current, and 2mA worst-case chip quiescent current:

$$P_D = (5.5 – 0) \bullet 65mA + 5.5 \bullet 2mA = 368.5mW$$

CE3320 power dissipation is very low if a current limited wall adapter is used and allowed to enter current limit. When the wall adapter is in current limit, the voltage drop across the CE3320 charger is:

$$V_{DROP} = I_{LIMIT} \bullet R_{PFET}$$

where I_{LIMIT} is the wall adapter current limit and R_{PFET} is the on resistance of the topside PMOS switch.

The total CE3320 power dissipation during current limited charging is:

$$P_D = (V_{BAT} + V_{DROP}) \bullet (I_{IN} + I_P) + V_{DROP} \bullet I_{LIMIT}$$

where I_{IN} is the chip quiescent current and I_P is total current flowing through the IDET and PROG programming pins. Maximum dissipation in this mode occurs with the highest V_{BAT} that keeps the wall adapter in current limit (which is very close to V_{FLOAT}), highest quiescent current I_{IN}, highest PMOS on resistance R_{PFET}, highest I_{LIMIT} and highest programming current I_P.

Assume the CE3320 is programmed for 2A charging and 200mA IDET and that a 1.5A wall adapter is being used:

$$I_{LIMIT} = 1500mA,\ R_{PFET} = 125m\Omega,\ I_{IN} = 2mA,\ I_P = 4mA \text{ and}$$

$$V_{BAT} \approx V_{FLOAT} = 4.242V$$

then:

$$V_{DROP} = 1500mA \bullet 125m\Omega = 187.5mV$$

and: $P_D = (4.242V + 0.1875V) \bullet (2mA + 4mA) + 0.1905V \bullet 1500mA = 315.5mW$

Power dissipation in buck battery charger mode may be estimated from the dissipation curves given in the Typical Performance Characteristics section of the data sheet. This will slightly overestimate chip power dissipation, because it assumes all loss, including loss from external components, occurs within the chip.

Insert the highest power dissipation figure into the following equation to determine maximum junction temperature:

$$T_j = T_{opr} + (P_D \bullet 37°C/W)$$

The CE3320 includes chip overtemperature protection. If junction temperature exceeds 160°C (typical), the chip will stop battery charging until chip temperature drops below 150°C.

Using the CE3320 in Applications Without a Battery

The CE3320 is normally used in end products that only operate with the battery attached (Figure 21). Under these conditions the battery is available to supply load transient currents. For indefinite operation with a powered wall adapter there are only two requirements—that the average current drawn by the load is less than the high rate charge current, and that V_{BAT} stays above the trickle charge threshold when the load is initially turned on and during other load transients. When making this determination take into account battery impedance. If battery voltage is less than the trickle charge threshold, the system load may be turned off until V_{BAT} is high enough to meet these conditions.

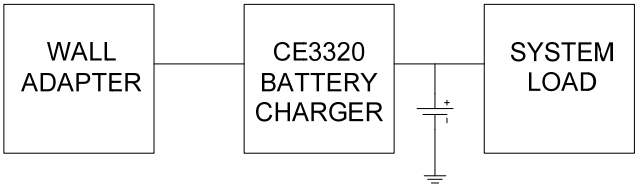


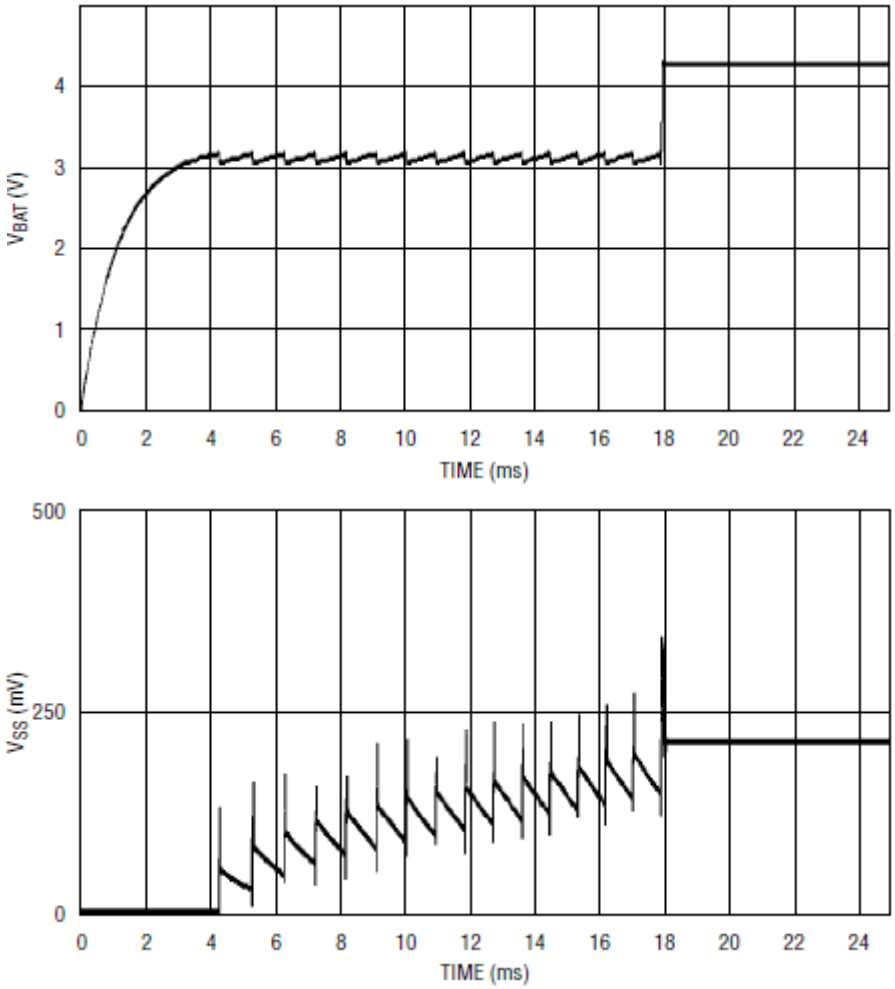
Figure 21. Typical Application

The situation changes dramatically with the battery removed (Figure 22). Since the battery is absent, V_{BAT} begins at zero when a powered wall adapter is first connected to the battery charger. With a maximum load less than the CE3320 trickle charge current, battery voltage will ramp up until V_{BAT} crosses

the trickle charge threshold. When this occurs, the CE3320 switches over from trickle charge to high rate (PWM) charge mode but initially delivers zero current (because the soft-start pin is at zero). Battery voltage drops as a result of the system load, crossing below the trickle charge threshold. The charger re-enters trickle charge mode and the battery voltage ramps up again until the battery charger re-enters high rate mode.

The soft-start voltage is slightly higher this time around (than in the previous PWM cycle). Every successive time that the charger enters high rate (PWM) charge mode, the soft-start pin is at a slightly higher voltage. Eventually high rate charge mode begins with a soft-start voltage that causes the PWM charger to provide more current than the system load demands, and V_{BAT} rapidly rises until the float voltage is reached.

For battery-less operation, system load current should be restricted to less than the worst case trickle charge current (preferably less than 30mA) when V_{BAT} is less than 3.15V (through an undervoltage lockout or other means). Above V_{BAT} = 3.15V, system load current less than or equal to the high rate charge current is allowed. If operation without a battery is required, additional low-ESR output filtering improves start-up and other load transients. Battery-less start-up is also improved if a 10k resistor is placed in series with the soft-start capacitor.



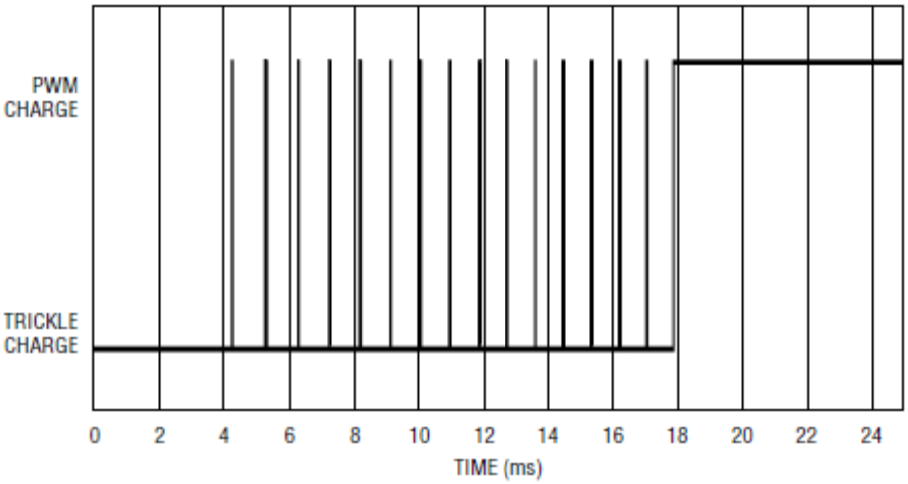


Figure 22. Battery-Less Start-Up

PCB Layout Considerations

Switch rise and fall times are kept under 5ns for maximum efficiency. To minimize radiation, the SW pin and input bypass capacitor leads (between PV_{IN} and PGND) should be kept as short as possible. A ground plane should be used under the switching circuitry to prevent interplane coupling. The Exposed Pad must be connected to the ground plane for proper power dissipation. The other paths contain only DC and/or 1.5MHz tri-wave ripple current and are less critical.

With the exception of the input and output filter capacitors (which should be connected to PGND) all other components that return to ground should be connected to GNDSENS.

Recommended Components Manufacturers

For a list of recommend component manufacturers, contact the Chipower application department.

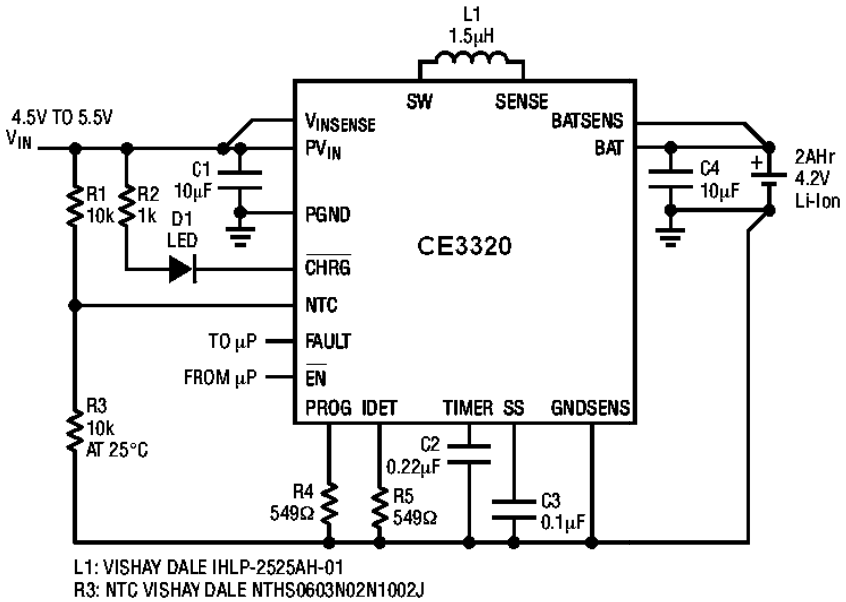
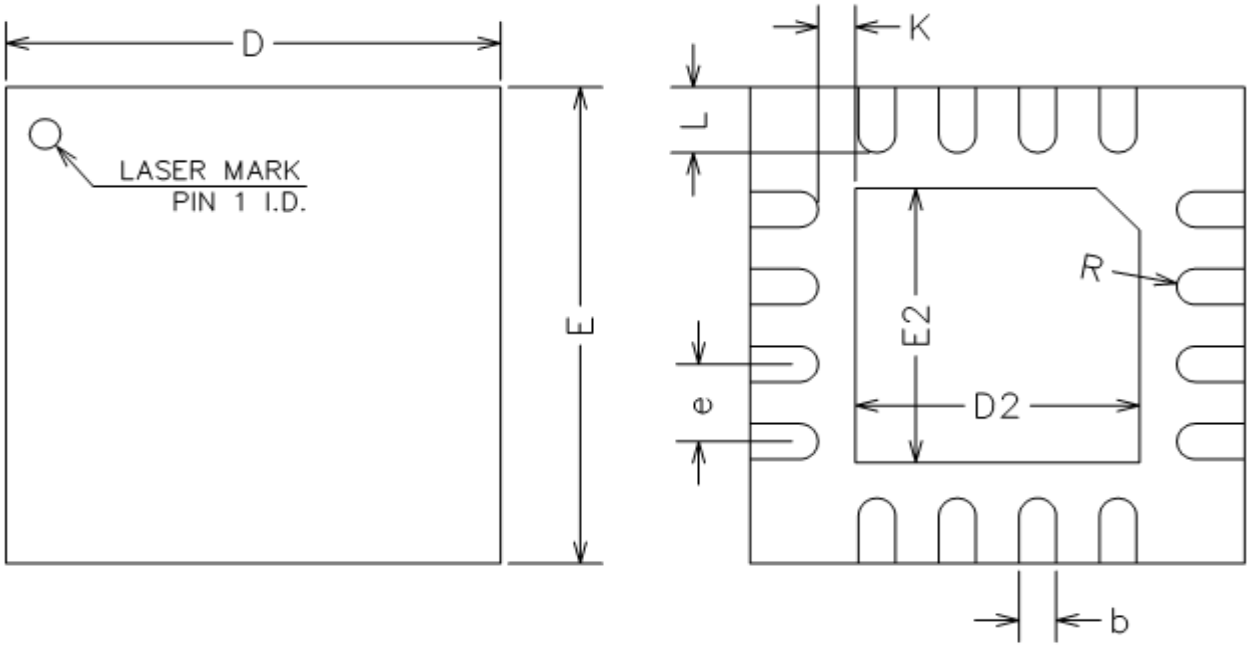
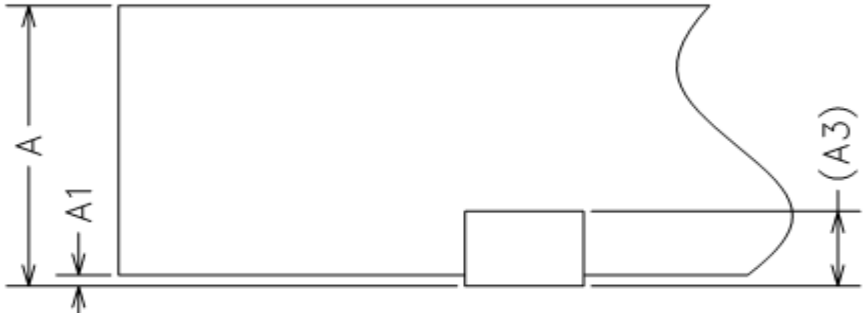


Figure 23. 2A Li-Ion Battery Charger with 3Hr Timer, Temperature Qualification, Soft-Start, Remote Sensing and C/10 Indication

■ PACKAGING INFORMATION

• QFN4×4-16 PACKAGE OUTLINE DIMENSIONS





Dimensions In Millimeters			
Symbol	Min	NOM	Max
A	0.70	0.75	0.80
A1	0.0	0.02	0.05
A3		0.20REF	
b	0.25	0.30	0.35
D	3.90	4.00	4.10
E	3.90	4.00	4.10
D2	2.20	2.30	2.40
E2	2.20	2.30	2.40
e	0.55	0.65	0.75
K	0.20	-	-
L	0.50	0.55	0.60
R	0.09	-	-