Incorporating Active-Clamp Technology to Maximize Efficiency in Flyback and Forward Designs

Brian King and David Strasser

ABSTRACT

For telecom and power-over-Ethernet (PoE) applications up to 25 W, single-ended forward and flyback topologies offer the lowest potential cost; however, utilizing active-clamp technology can increase the efficiency of both, particularly when synchronous rectification is appropriate for the outputs. Subjects to be addressed in this topic include obtaining zero-voltage switching; selecting and driving synchronous rectifier MOSFETs; optimizing transformer design; and comparing equivalent forward and flyback solutions side by side, emphasizing the performance benefits of each topology that can be achieved as a trade-off against circuit complexity and cost.

I. INTRODUCTION

Power-over-Ethernet (PoE) applications require high efficiency due to limited input power. The IEEE 802.3at specification limits the input power of a powered device to 13 W for low-power systems and 25.5 W for high-power systems. Telecom applications, which may have battery backup or demanding thermal requirements, also need high efficiency. For several reasons, employing an active reset is an excellent choice for optimizing efficiency in these and many other low-power applications. First, the transformer currents soften the switching losses of the primary MOSFETs. Second, the clamp provides near lossless snubbing on the primary. In the forward converter, the transformer is always driven into the first and third quadrants, providing better core utilization. There is no 50% duty-cycle limitation, allowing for wide input ranges and lowering the stresses on the switching components. Third and most significant, the secondary's voltage waveforms are ideal for implementing self-driven synchronous rectifiers.

II. BASIC OPERATION OF FLYBACK AND FORWARD CONVERTERS

The basic power stages of a flyback and a forward converter are shown in Fig. 1. They appear very similar, but operation is quite different. The flyback converter stores energy in the primary winding of the "transformer" while switch Q1 is on. (Since the transformer stores energy, it is really utilized as a coupled inductor; but, to conform to convention, it will be referred to here as a "transformer.") When switch Q1 in
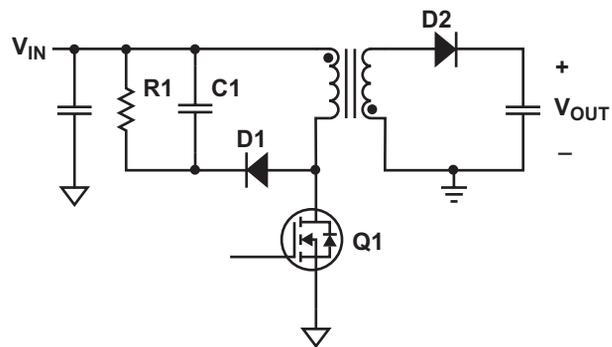
a. Flyback converter.
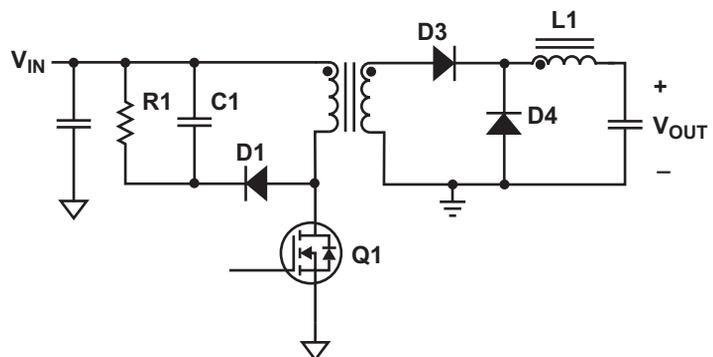
b. Forward converter.

Fig. 1. Basic power stages.

the flyback converter is turned off, the transformer releases energy to the output through the secondary winding. The forward converter transfers energy to the secondary while switch Q1 is on, storing part of the energy in L1. When switch Q1 turns off, the stored energy in L1 is delivered to the load.

In lower-voltage, higher-current applications, forward converters tend to offer a better solution than flyback converters. This is partly because the transformer's secondary currents are much tamer in forward converters, as shown in Fig. 2. If the ripple current is neglected, these waveforms can be treated as ideal square waves, and their RMS values can be calculated. For the flyback converter,

$$I_{sec\_RMS} = \frac{I_{OUT}}{\sqrt{1-D}}. \qquad (1)$$

For the forward converter,

$$I_{sec\_RMS} = I_{OUT} \times \sqrt{D}. \qquad (2)$$

Fig. 2. Transformer's secondary currents.

Fig. 3. Currents in the output capacitor.

Comparing the two topologies with a 50% duty factor shows that the secondary RMS current in the flyback converter is twice that of the forward converter. Compounding the problem, the ripple current in the output capacitors of the flyback converter becomes difficult to manage at higher load currents since the AC content of the secondary current flows through the output capacitors. The output capacitor in a forward converter conducts only output-inductor ripple current. The output capacitor's current waveforms are shown in Fig. 3.

Components C1, D1, and R1 clamp the voltage across Q1 to a safe level when Q1 is turned off. In the flyback converter, the leakage energy is clamped and dissipated in R1. In the forward converter, the clamp resets the magnetizing current to zero for each switching cycle to keep the transformer from saturating. The magnetizing energy is dissipated by the clamp. Q1 hard switches in both
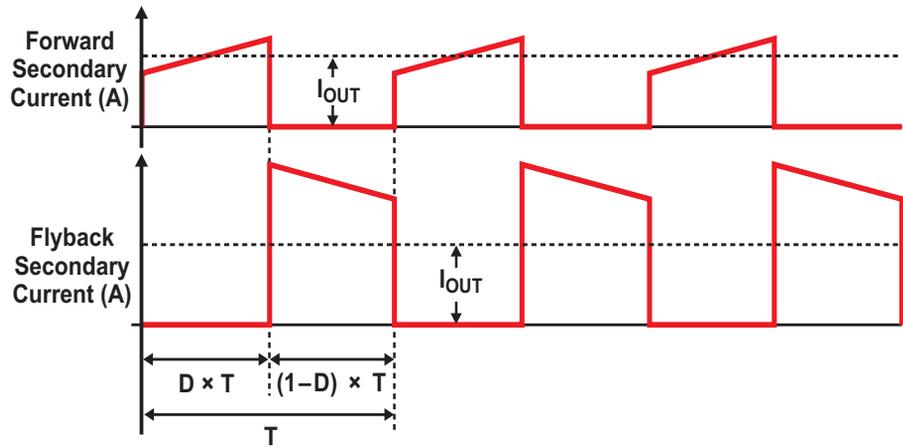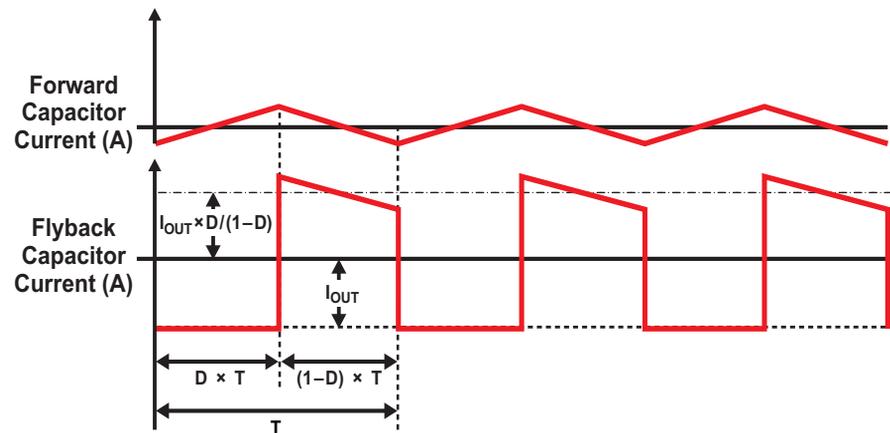
converters. As Q1 turns on, the drain current begins to rise before the drain-to-source voltage reaches zero. Similarly, as Q1 turns off, the peak primary current is flowing as the drain-to-source voltage transitions from zero to the clamped level. Power is dissipated during both transitions, since there is voltage across Q1 while current is simultaneously being conducted.

In Fig. 1, both converters are shown with diode-output rectifiers. Diodes are inexpensive but not very efficient in comparison to power MOSFETs (hereinafter referred to as "FETs"). The efficiency of a converter with a diode rectifier has a strong dependency on the ratio of the diode voltage drop to the output voltage. As the output voltage decreases, the efficiency decreases, since the diode drop is a larger portion of the output voltage. The diode rectifier is a better choice for higher output voltage and lower output current.

TABLE 1. EFFICIENCY LOSS DUE TO OUTPUT RECTIFIER FOR 25-W OUTPUT

V_{OUT} (V)	I_{OUT} (A)	V_{diode} (V)	$R_{DS(on)}$ (mΩ)	Efficiency Change (%)		
				Flyback or Forward Diode	Flyback FET	Forward FET
12	2	0.6	25	−9.1	−1.6	−0.4
5	5	0.45	10	−15.3	−3.8	−1.0
3.3	7.5	0.35	5	−17.5	−4.3	−1.1
1.8	14	0.35	2.5	−28.0	−7.2	−1.9

For lower output voltage and higher output current, the Schottky diode can be replaced with a synchronous FET to improve efficiency. Table 1 shows the efficiency losses that are due to just the forward drop of the rectifier. As the output voltage decreases, reducing the rectifier drop becomes critical to provide the best possible efficiency.

For the losses shown in Table 1, it is assumed that the converters are operating at a 50% duty cycle. It is interesting to note that the diode-rectifier loss is the same for a flyback as for a forward converter. The diode rectifier in a flyback converter sees a peak current of two times the output current for half the switching period. Each of the rectifiers in a forward converter sees a peak current equal to the output current, but there are two of them, each conducting for half the switching period. If synchronous FETs with the same ON resistance are used in both converters, the forward converter is the better choice for efficiency improvement due to the lower peak currents.

A. Active Reset

Since the best possible efficiency is required for PoE and telecom applications, the basic flyback or forward converter with an RCD clamp (R1/C1/D1 in Fig. 1) and diode rectifiers is not acceptable. Replacing the RCD clamp with an active-clamp circuit will greatly improve the efficiency and performance of both topologies, with the following benefits:

- The reset is nearly lossless, since there is no resistor to dissipate energy.
- As Q1 turns on, the active reset reduces the drain-to-source voltage, V_{DS}, before the drain current flows, reducing switching losses.
- The active reset results in power waveforms that are ideal for implementing self-driven synchronous rectifiers.

The primary-side active-clamp circuit can be the same for both the flyback and the forward converter. Both can use either of two possible configurations, as shown in Fig. 4 [1]. The circuit with the p-channel clamp is preferred because it can easily be driven by the pulse-width-modulation (PWM) controller. The n-channel clamp reduces the voltage stress on the clamp capacitor but requires a floating gate drive. Neglecting the effects of the clamp resonance, the voltage stresses of the two primary-side FETs are equal and can be calculated as

$$V_{DS\_Q1} = V_{DS\_Q2} = \frac{V_{IN}}{1-D}. \qquad (3)$$

For the PoE and telecom input-voltage range, both primary-side FETs (Q1 and Q2) are typically rated for 150 V_{DS}. The p-channel FET choices become limited
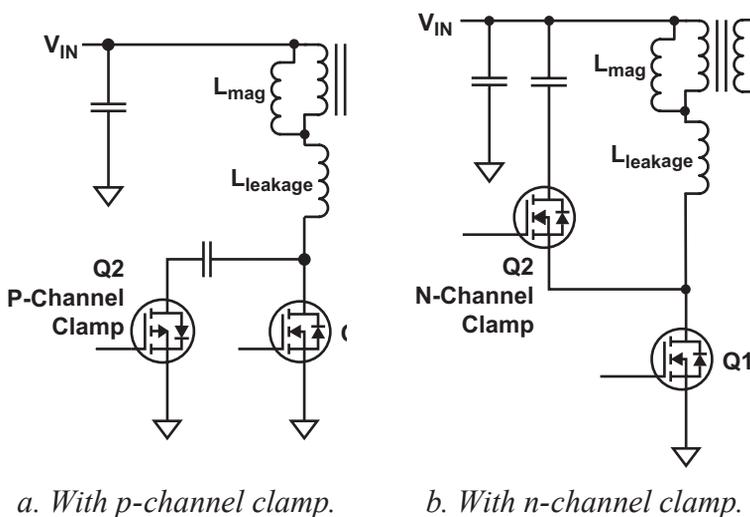

a. With p-channel clamp.   *b. With n-channel clamp.*

Fig. 4. Two different configurations of the clamp circuit.

when the V_{DS} rating exceeds 200 V. For off-line supplies, where higher voltage ratings are required, an n-channel clamp is a better choice.

Next, the benefits for each topology of combining an active reset with synchronous rectification will be investigated in detail.

B. Flyback Converter

When cost is a major concern, the flyback topology is usually the preferred choice. In its basic form, it utilizes a single primary FET and a single secondary rectifier. The latter can be either a diode or a synchronous FET. Many design references exist for the flyback converter, such as References [2], [3], and [4] of this topic. Adding synchronous rectification and active clamp to the flyback converter can provide significant gains in efficiency.

Fig. 5 shows the simplified power stage for a flyback converter with an active clamp and a synchronous-FET rectifier. A diode-rectified flyback converter allows the secondary current to flow in only one direction and can operate in discontinuous-conduction mode (DCM) at light loads. Interestingly, a flyback converter with synchronous rectifiers allows the secondary current to flow in both directions and forces a continuous-conduction mode (CCM) to occur over the entire load range. This can be seen by inspecting the power waveforms in Fig. 6, which shows how the transformer is driven into both the first and third quadrants at light loads. At light loads, this AC circulating current will reduce the efficiency (compared to a diode-rectified flyback) as it flows though the primary FET, secondary FET, and transformer [5]. Selecting the proper primary inductance for the power transformer can reduce the losses by reducing the AC circulating currents.

Transformer Design

When the primary inductance for the flyback transformer is selected, trade-offs need to be made. With lower inductance, losses at light loads will be higher due to the higher peak-to-peak AC circulating current. Higher inductance will improve light-load efficiency by reducing the peak-to-peak ripple current. But higher inductance will require more primary turns and/or a larger core. This will increase the winding
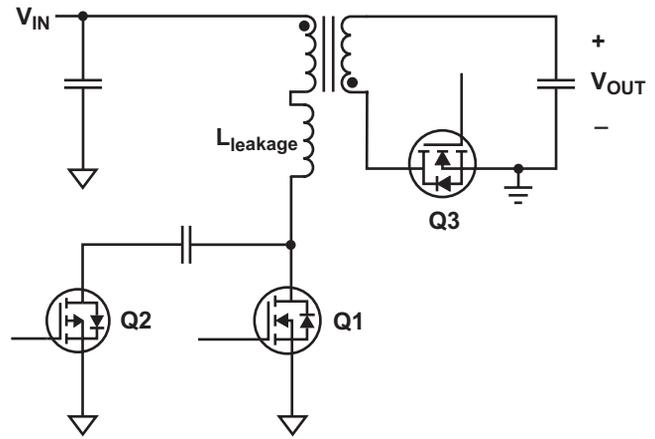

Fig. 5. Simplified power stage of an active-clamp flyback converter with a synchronous rectifier.

losses and reduce the efficiency at higher loads. Also, the right-half-plane zero (RHPZ) [6] in the control loop is inversely proportional to the primary inductance and is given by

$$\text{RHPZ} = \frac{R_{load} \times (1-D)^2}{2\pi LD}. \quad (4)$$

As the inductance increases, the RHPZ moves lower in frequency. To achieve acceptable phase and gain margins, the loop crossover frequency should be at least one decade below the RHPZ frequency. A primary inductance that results in a peak-to-peak ripple current of 25 to 50% of the maximum load current is usually a good compromise between peak-to-peak current, transformer size, and RHPZ frequency.
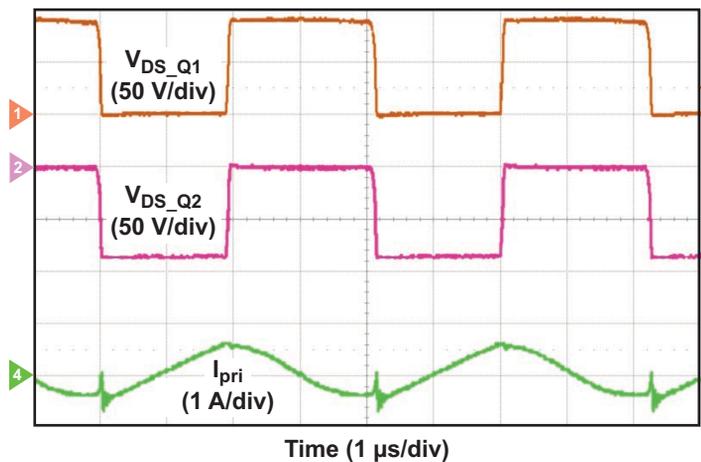

Fig. 6. Primary-side waveforms during no-load operation.

For a flyback converter operating in CCM, the transformer turns ratio and input-voltage range determine the duty-cycle range:

$$D = \frac{V_{OUT} \times \dfrac{N_{pri}}{N_{sec}}}{V_{IN} + V_{OUT} \times \dfrac{N_{pri}}{N_{sec}}} \qquad (5)$$

An input range of 36 to 75 V covers most PoE and telecom applications. For this input range, the transformer turns ratio is usually selected to achieve a maximum duty cycle of 60% at the minimum input voltage of 36 V. This results in a minimum duty cycle of approximately 42% at the maximum input voltage of 75 V. One of the benefits of the flyback topology is that it can accommodate a wide input range without severe changes in duty cycle. Fig. 7 shows how the choice of transformer turns ratio affects the V_{DS} ratings of the primary FETs (Q1 and Q2). In this figure, the sum of the input voltage and reflected output voltage is plotted versus the input voltage, where the duty cycle was set to 60% for a 36-V input. This neglects the effects of any peaking from the clamp resonance, which must also be considered before the V_{DS} rating of the primary FETs is determined.

Active-Clamp Circuit

Fig. 8a shows the waveform of primary FET Q1's V_{DS} with the commonly used RCD clamp. Because of the large voltage spike that occurs when Q1 turns off, a primary FET with a higher voltage rating is often required. FETs with higher voltage ratings generally have higher $R_{DS(on)}$ and slower switching times, both of which reduce efficiency. Resistor R1 in the clamp must also dissipate part of the energy in the leakage inductance, which can be significant. In addition, the voltage overshoot and ringing that occur when the primary FET's drain is turned off may create an EMI issue.

The active-clamp circuit, shown in Fig. 5, provides significant benefits versus an RCD clamp (Fig. 1a). Fig. 8b shows that the drain-to-source voltage of the primary FET no longer has the large voltage spike when it is turned off. Instead of being dissipated in a resistor, the leakage energy
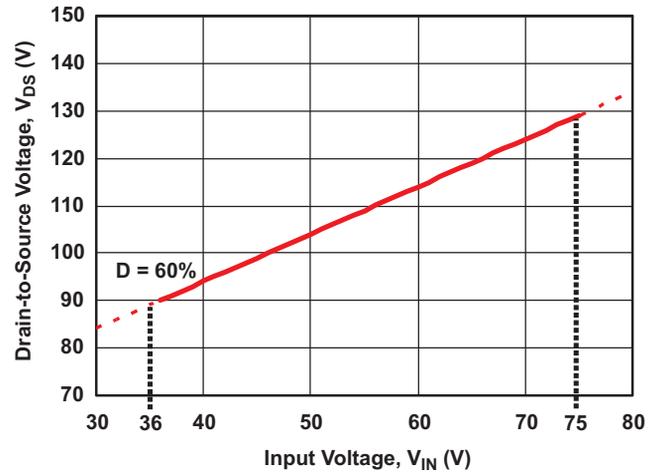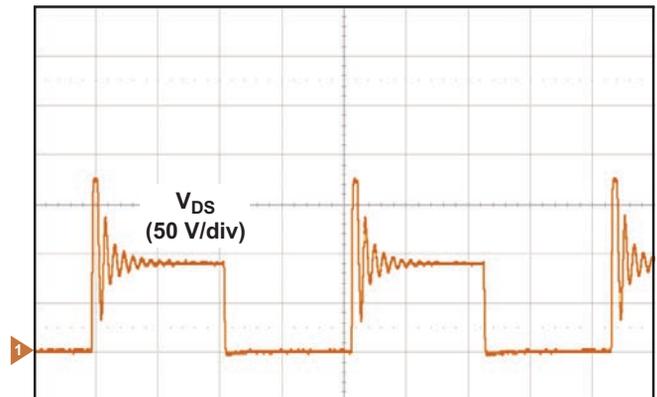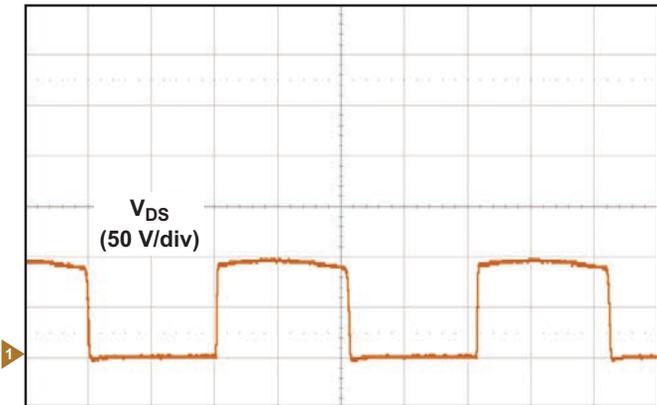
Fig. 7. Voltage stress of flyback converter's primary FETs, neglecting leakage spike (RCD) or resonance (active clamp).

a. With RCD clamp.

b. With active reset.

Fig. 8. Primary FET's drain-to-source voltage.

is mostly recovered and returned to the input capacitors. Eliminating the leakage spike allows a primary FET with a lower V_{DS} rating to be used, improving efficiency. Potential EMI issues are also significantly reduced.

In the operation of an active-clamp flyback converter, the transformer's primary leakage inductance plays a crucial role. A simplified schematic of the flyback converter's active-clamp power stage, including the leakage inductance, is shown in Fig. 9. When Q1 is on, operation is the same as with a standard flyback converter. The current flows into the transformer's primary, storing energy in the primary's magnetizing and leakage inductances. During this time, Q2 and Q3 are off, while the output capacitor supplies current to the load.

When Q1 turns off, Q2 and Q3 turn on. The stored energy in the magnetizing inductance is diverted by Q3, supplying current to the load and charging the output capacitor. The output capacitor is connected across the secondary winding and gets reflected through the transformer to the primary, essentially shorting the primary winding. With the voltage on the primary's magnetizing inductance held to the reflected output voltage, the current flowing in the clamp will resonate with
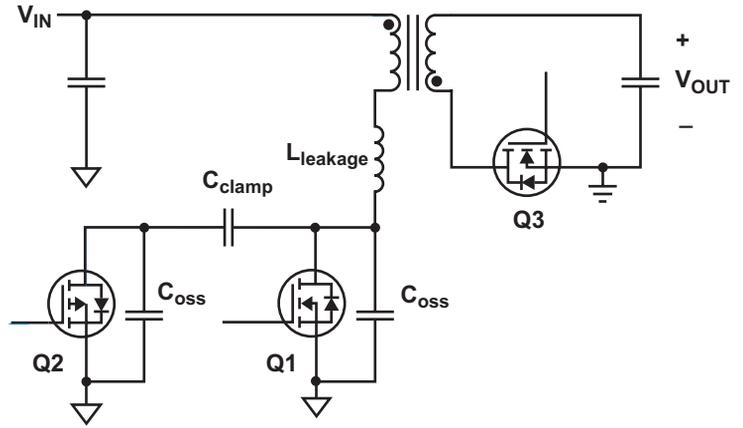

Fig. 9. Simplified schematic of flyback converter's power stage.

$L_{leakage}$ and C_{clamp} at a frequency of

$$f_{clamp} = \frac{1}{2\pi\sqrt{L_{leakage} \times C_{clamp}}}. \qquad (6)$$

The instantaneous current flowing in the clamp circuit at the moment when Q2 turns on is equal to the peak primary current. Neglecting circuit losses, the clamp current will resonate as a cosine waveform at frequency f_{clamp} while Q1 is off (see Fig. 10):

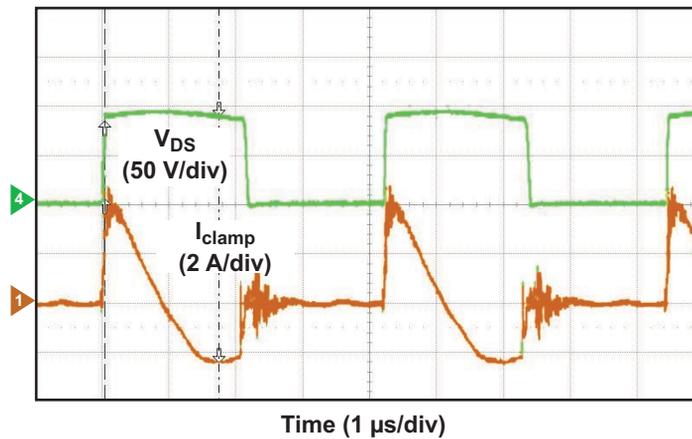$$I_{clamp}(t) = I_{pri\_pk} \times \cos(2\pi f_{clamp} \times t) \qquad (7)$$

Fig. 10. Measured clamp current.

The RMS current in the clamp, given by Equation (8), can become significant at heavy loads:

$$I_{clamp\_RMS}(D) = \sqrt{\frac{1}{T} \times \int_0^{\frac{1-D}{f_{sw}}} I_{clamp}^2(t) \times dt} \qquad (8)$$

The $R_{DS(on)}$ conduction losses must be considered when a clamp FET is selected.

As can be seen from the clamp current's waveform, the current will flow in both directions through Q2. The magnitude and direction of the clamp current when Q2 turns off depends on the duty cycle. If the clamp current is flowing from drain to source when Q2 turns off, the clamp current continues to flow through the body diode of Q2. In this scenario, when Q1 turns on, C_{clamp} discharges until the body diode of Q2 completes reverse recovery and turns off. This results in significantly increased power dissipation in Q1. To prevent this condition, it is necessary for f_{clamp} to be selected such that the clamp current is flowing from source to drain through Q2 when Q1 turns on. If f_{clamp} is set equal to the switching frequency, the current will be flowing in the correct direction for duty cycles between 25% and 75%. (The cosine waveform crosses 0 at π and $3\pi/2$.)

C_{clamp} is typically selected to obtain an acceptable value for f_{clamp}, per Equation (6). The leakage inductance can be measured or taken from the transformer specification. The measured leakage inductance can be much lower than the maximum rated leakage from the transformer specification. To account for variations in the leakage inductance, f_{clamp} should be about 20% lower than the switching frequency.

Soft Switching

Fig. 11 shows the primary-side switching waveforms that occur as Q1 turns off. Before Q1 turns off, the peak primary current is flowing through the transformer's magnetizing inductance, leakage inductance, and Q1 to ground. When the gate of Q1 is pulled low, the current stored in the magnetizing inductance (gap) begins to transfer to the secondary winding, but only after the voltage on the secondary transitions up to the point where the internal diode of Q3 is forward-biased. When Q1 is completely off, the current flowing in the leakage
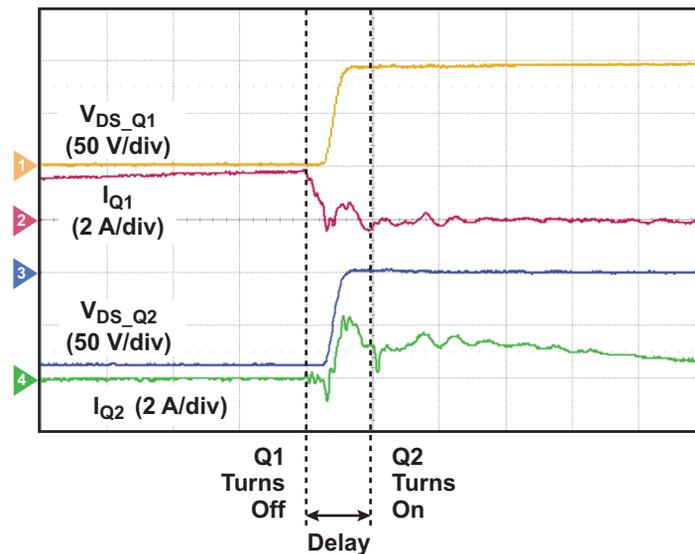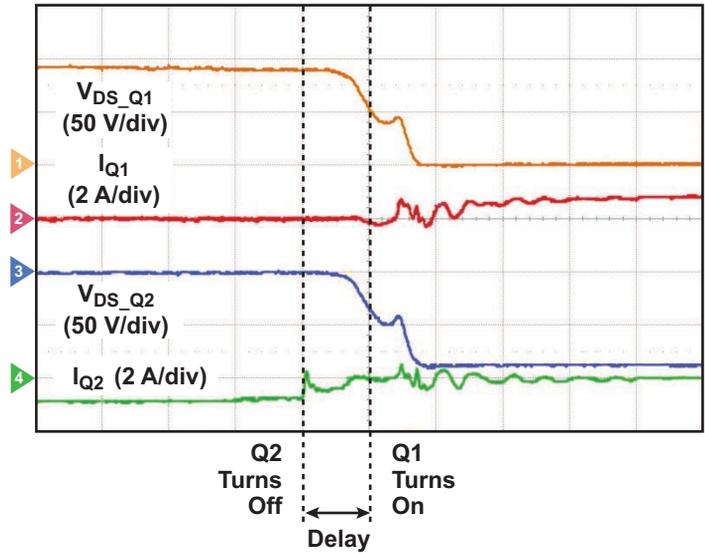

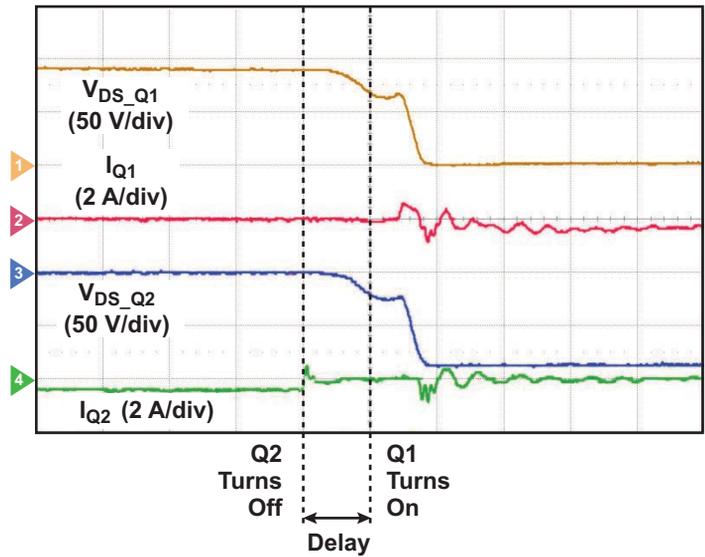*Fig. 11. Flyback converter's primary-side switching waveforms as Q1 turns off.*

inductance is commuted from Q1 through the clamp capacitor and body diode of Q2 before Q2 actually turns on. After a delay time, Q2 is turned on with 0 V across it. The load and duty cycle have no effect, because the peak current is always flowing in the same direction during this transition.

Fig. 12 shows the primary-side switching waveforms that occur while Q1 is turning on. Assuming that the clamp frequency was properly chosen, the clamp current will flow from source to drain through Q2 before Q1 turns on. When Q2 is turned off, the clamp current will continue to flow through the body capacitance of Q2, resonating with the leakage inductance. The clamp current also commutates to the body capacitance of Q1, again resonating with the leakage inductance. It can be seen that Q2 switches off with 0 V across it. After a delay, the gate of Q1 transitions high, and Q1 begins to turn on. As can be seen from the waveforms, this transition does not take place with the voltage fully at zero. At maximum load (Fig. 12a), the drain of Q1 resonates down toward ground before Q1 is switched on, achieving partial zero-voltage switching. At lighter loads (Fig. 12b), Q1's drain voltage does not resonate as far down because there is less energy stored in the leakage before this transition occurs.

Since the resonant frequency of the falling drain voltage depends on various parasitic capacitances and the leakage inductance of the transformer, it is difficult to precisely calculate the required delay time. The best way to select a delay time is to measure these waveforms on an actual converter with maximum load. The delay time should be set such that Q1 turns on just before Q1's drain voltage reaches the resonant valley. This is shown as the time between the dashed lines in Fig. 12.

a. Maximum-load operation.

b. No-load operation.

Fig. 12. Flyback converter's primary-side switching waveforms as Q1 turns on.
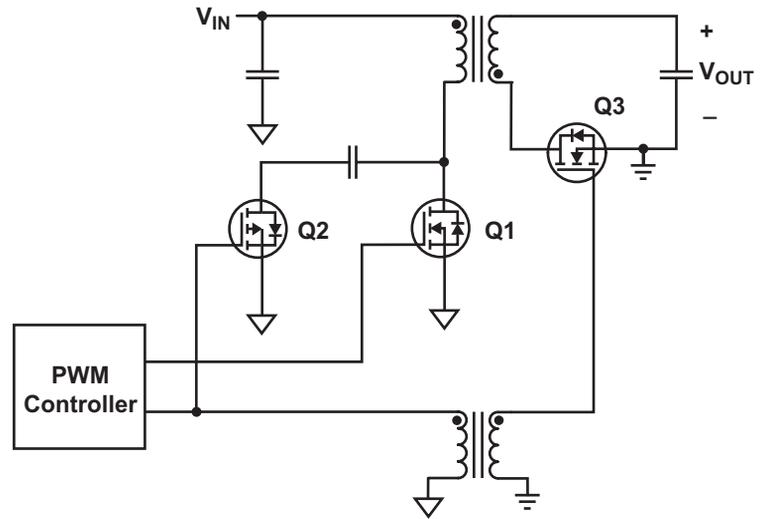
Synchronous Rectification

Fig. 13 shows two ways of controlling the synchronous FET (Q3) in the flyback converter. Q3 can be driven from the primary controller through a separate gate-drive transformer and a few signal-conditioning components as shown in Fig. 13a [5]. However, the cost of using a gate-drive transformer may be unacceptable. A more cost-effective means of driving Q3 is a "self-driven" architecture that uses a gate-drive winding on the main power transformer, as shown in Fig. 13b.

In the self-driven architecture, Q3 does not begin to turn off until the primary FET (Q1) has turned on and the magnetic field in the transformer reverses [1, 5]. There is some overlap time when Q1 and Q3 are simultaneously conducting. During this time, the input is shorted to the output through the power transformer. "Shoot-through" current during conduction overlap is limited only by the leakage inductance of the power transformer and by stray circuit/component resistances. Therefore it is essential for Q3 to turn off as fast as possible to reduce shoot-through current. Q3 should have a short turn-off delay time and a fast fall time. For operation at 250 kHz, the typical turn-off delay should be less than 50 ns, and the typical fall time should be less than 25 ns.

The gate-drive voltage of Q3 remains constant with input voltage, but the reverse voltage on the Q3 gate changes with input voltage. This reverse voltage when referenced to ground is

$$V_{gate\_reverse(max)} = \frac{V_{IN(max)}}{N_{pri\_gate}}. \qquad (9)$$

The input-voltage range for PoE converters is 36 to 57 VDC. A PoE flyback converter with a 60% maximum duty cycle will have a transformer turns ratio of 12:1 for a 3.3-V output and a gate-drive turns ratio of 6:1. The maximum reverse gate voltage from Equation (9) will be 9.5 V. This is well within the 20-V gate rating of most FETs with a 30-V drain-to-source rating. The resistor/Zener clamp (R2/D5/D6 in Fig. 13b) reduces

a. With a gate-drive transformer.
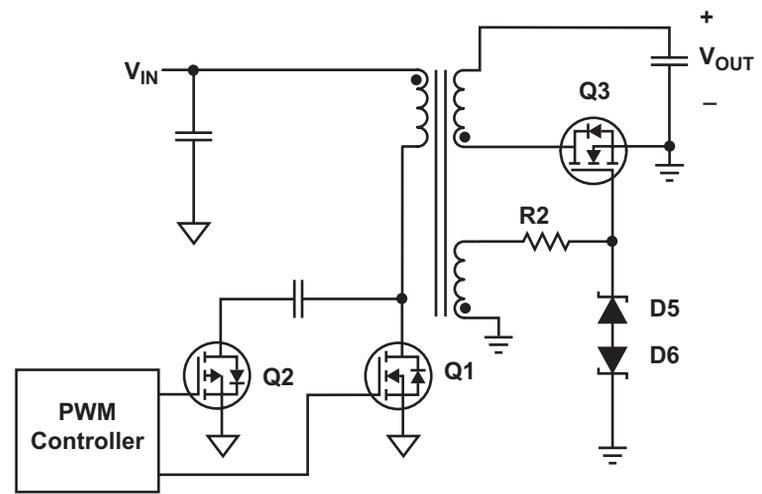
b. Self-driven.

Fig. 13. Gate drives for synchronous-rectified flyback converter.

voltage spikes that may appear on the gate due to stray inductance.

If the PoE converter needs to operate from a 12-V wall adapter as well as PoE, the input-voltage range will be 10 to 57 VDC. To allow the converter to be on as long as possible at maximum input voltages, a 70% maximum duty cycle should be used. For this PoE supply, the transformer will have a 6:1 turns ratio for a 3.3-V output and a gate-drive turns ratio of 3:1. From Equation (9), the maximum reverse gate voltage will be 19 V,

which does not provide much margin for a FET with a 20-V gate rating. A drive-conditioning circuit must be added to the synchronous FET to provide a reverse voltage clamp when there is a wide input-voltage range, as shown in Fig. 14.

When the voltage on the gate-drive winding is positive with respect to ground, C13 provides a spike of current through D5 to charge the Miller capacitance of Q3. Q3 is turned on by charging the gate capacitance through D2/R2. When the voltage on the gate-drive winding is negative with respect to ground, D2 and D5 block the negative voltage from appearing at the gate of Q3. C13 provides a spike of current to the base of Q5, which discharges the gate capacitance, turning off Q3 fast. Current through R7 keeps Q5 on and Q3 off for the remainder of the cycle.

In addition to clamping the reverse gate voltage of the synchronous FET, this circuit also provides a slight improvement in efficiency. When reverse clamping is not needed, the conditioning circuit can be used to improve the turn-on and turn-off switching times of the synchronous FET. This will result in improved efficiency by reducing the shoot-through current.

A drive-conditioning circuit added to the primary FET also helps reduce shoot-through current. This circuit consists of a low-cost diode, a PNP transistor, and a small resistor (D3/R3/Q4 in Fig. 15). The resistor slows the turn-on time of the primary FET by limiting the peak gate current, allowing the synchronous FET more time to turn off. The PNP transistor speeds turn-off time by providing a low-impedance clamp from gate to source. This reduces the turn-off loss of the primary FET.

Examples of Flyback-Converter Design

Two prototype flyback converters were designed and tested for common output-voltage rails, one converter for 3.3 V and the other for 12 V. These voltages were selected to show how the advantages of active clamp and synchronous rectifiers are dependent on output voltage. The specifications for these converters are shown in Table 2.
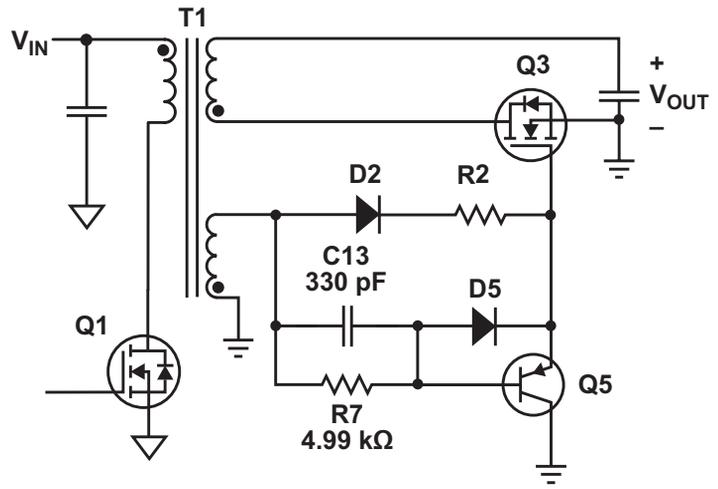
a. Gate-clamp circuit.
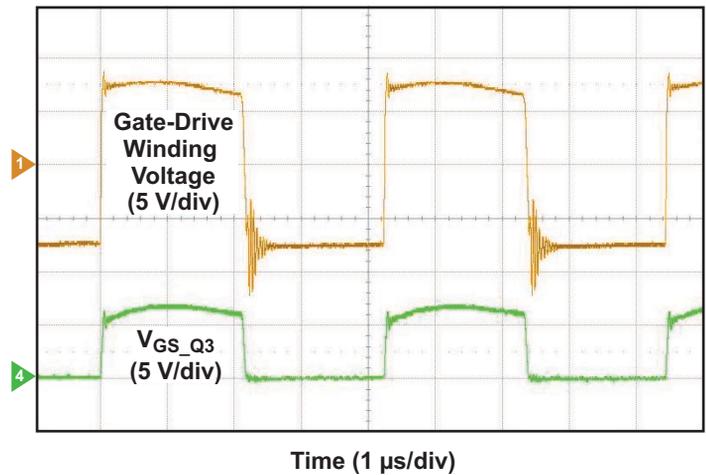
b. Measured gate-drive waveforms.

Fig. 14. Reverse voltage clamp on synchronous FET.

TABLE 2. SPECIFICATIONS FOR EXAMPLE FLYBACK CONVERTERS

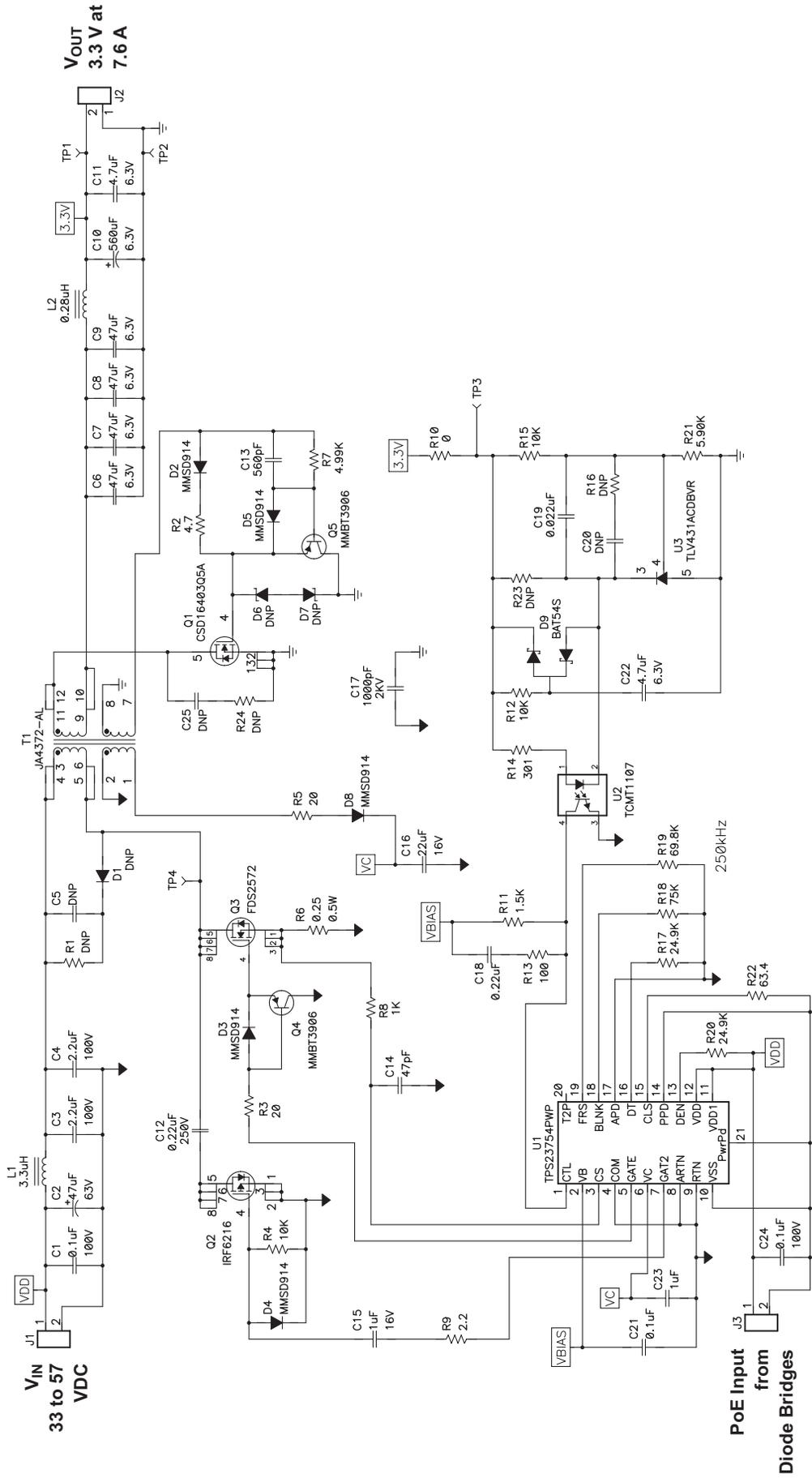| Parameter	3.3-V Converter	12-V Converter
Input Voltage (VDC)	33 to 57	33 to 57
Output Voltage (VDC)	3.3	12
Output Current (A)	7.6	2.08
Switching Frequency (kHz)	250	250

Fig. 15. Schematic of 3.3-V, 7.6-A flyback converter.

The TPS23754 controller was used in both example converters, which were designed for PoE applications. The TPS23754 contains both the pulse-width-modulation (PWM) controller and the PoE switch. Features include:

- Two gate drives for driving the primary FET and active-clamp FET
- Adjustable delay time between gate drives
- Adjustable leading-edge blanking on the current-sense signal
- PWM for use with an optocoupler/secondary-side error amplifier

For telecom applications that do not require the PoE switch, the UCC2897A (not considered here) can be used. It contains the same functionality as the TPS23754, with the additional features of undervoltage and overvoltage lockout.

The schematic of the 3.3-V converter is shown in Fig. 15 on page 2-11. This design was tested with an RCD clamp and then with an active reset. With a maximum output power of 25 W, the 3.3-V output current could be up to 7.6 A. At this current level, diode rectification of the secondary is not an option, so self-driven synchronous rectifiers were used in both the RCD-clamp design and the active-reset design. Note that the converter with the RCD-clamp circuit requires a higher voltage rating for both the primary FET and the synchronous FET. This is due to the large voltage spike that results from the leakage inductance (see Fig. 8).

The efficiency of the 3.3-V converter with the RCD clamp and active clamp is shown in Fig. 16. The converter utilizing active clamp is 4% more efficient at maximum load, resulting in a power savings of 1.37 W at a maximum load of 7.5 A. This significant gain in efficiency is due to soft switching of the primary FETs, reduced conduction losses (due to lower-voltage FETs), and the nondissipative clamp. This extra 1.37 W can be delivered to the output instead of being dissipated by the converter.

The schematic of the 12-V converter is shown in Fig. 17 (see next page). With the same maximum output power of 25 W, the 12-V output current is only 2.08 A. At this current level, a Schottky diode is a viable alternative for the secondary rectifier. The 12-V converter was tested with an RCD clamp
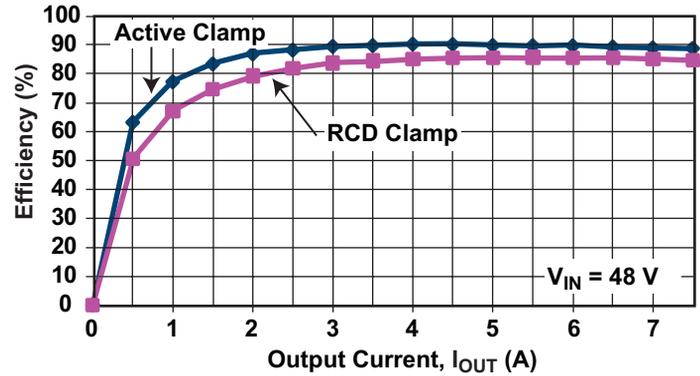

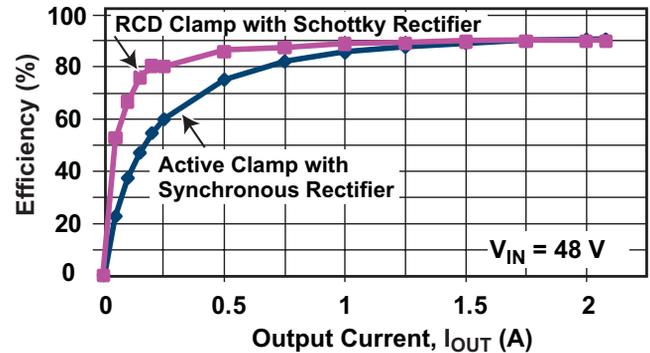Fig. 16. Efficiency of 3.3-V, 7.6-A flyback converter.

Fig. 18. Efficiency of 12-V, 2.08-A flyback converter

and a Schottky-diode rectifier and compared to the same converter with an active clamp and a synchronous rectifier. The efficiency for these two converter configurations is shown in Fig. 18. Compared to the 3.3-V design, the active clamp on the 12-V design offers no improvement in efficiency. This is partly because the leakage inductance of the 12-V transformer happened to be much lower than that of the 3.3-V transformer. At loads below approximately 1.5 A, the RCD clamp is more efficient than the active clamp. The power dissipated in the resistor of the RCD clamp is small due to the low leakage. Also, with the diode rectifier, the converter is operating in discontinuous-conduction mode (DCM). Therefore, the primary current does not reverse and there are no losses due to the circulating AC current as there are with the active clamp. At higher loads, the active clamp and the RCD clamp have about the same efficiency.
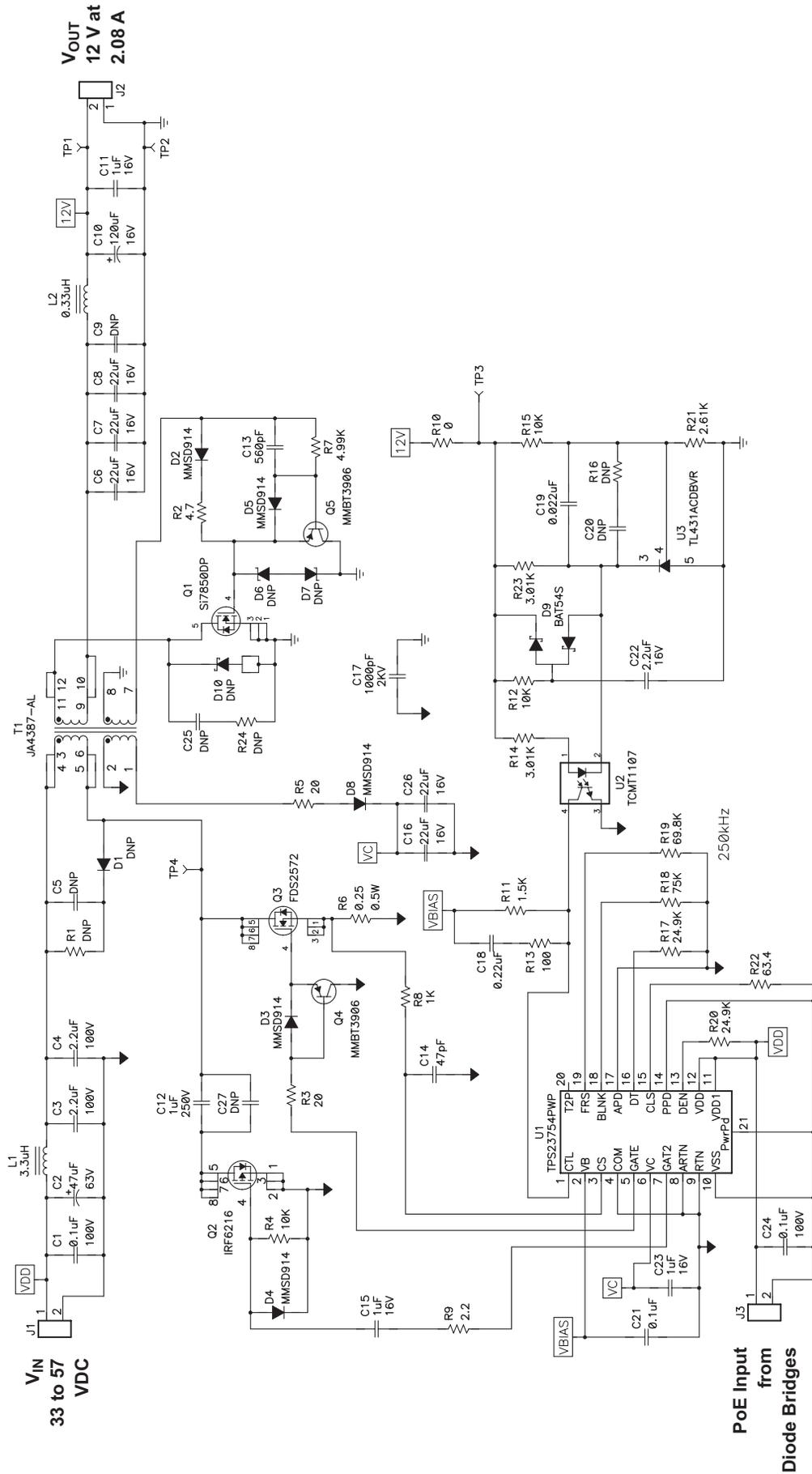
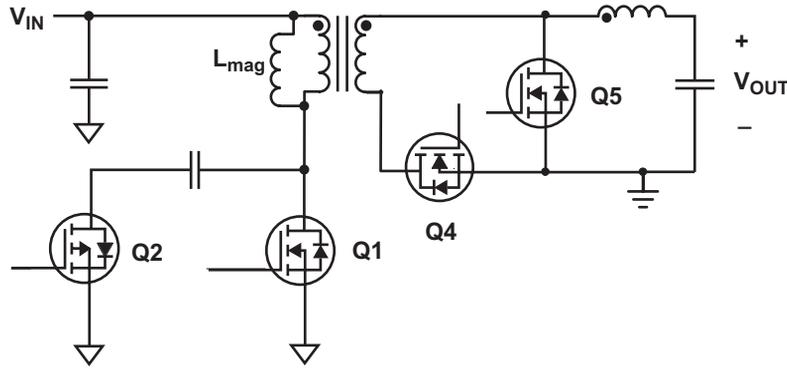Fig. 17. Schematic of 12-V, 2.08-A flyback converter.

Fig. 19. Simplified power stage of an active-clamp forward converter with synchronous rectifiers.

C. Forward Converter

The forward topology is usually the preferred choice for low-voltage, high-current conversion. Compared to the flyback converter, the transformer's lower secondary and capacitor currents reduce losses, leading to better efficiency. Similar to the flyback converter, the efficiency of the forward converter can be improved by adding synchronous rectification and an active clamp. Fig. 19 shows a simplified power stage for a forward converter with an active clamp and synchronous FET rectifiers.

Transformer Design

One of the interesting things about the active-clamp forward converter is that the transformer is always reset into the third quadrant. This can be seen in Fig. 20, which shows the transformer's primary current during the reset portion of the switching cycle.

In the forward converter, there is no right-half-plane zero (RHPZ) to worry about because power is transferred when Q1 is on. However, the selection of the primary inductance does impact the performance of the design. An inductance that is too small can lead to excessive magnetizing current, reducing efficiency. Conversely, an inductance that is too large may not store enough energy to drive the active clamp. For switching frequencies in the
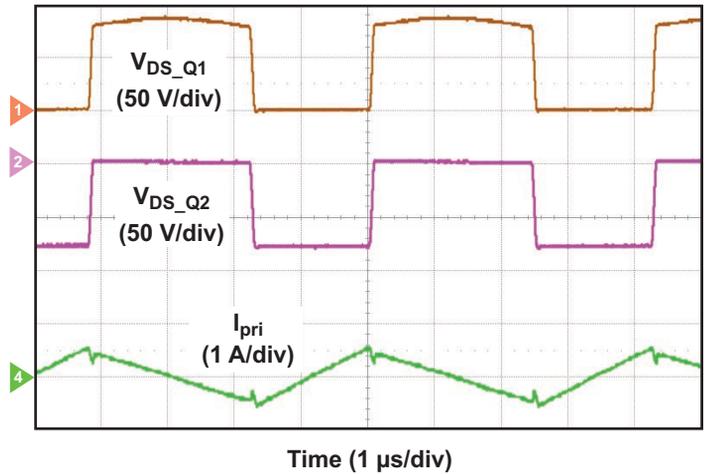

Fig. 20. Primary-side waveforms during no-load operation.

PoE and telecom input range of 100 to 400 kHz, a primary inductance of 100 µH works well.

Compared to the flyback converter, the duty cycle of the forward converter is more sensitive to changes in input voltage. The transformer's turns ratio and input range determine the duty-cycle range:

$$D = \frac{V_{OUT} \times \frac{N_{pri}}{N_{sec}}}{V_{IN}} \qquad (10)$$

When determining the transformer turns ratio, it is good practice to limit the maximum duty cycle to 75% or less to prevent excessive voltage stress at low input voltages. In Fig. 21, the voltage stress on the primary FETs, given by Equation (3), is plotted against the input voltage. At input voltages of less than 36 V, the duty cycle was set at 70%. At low input voltages, the denominator $(1 - D)$ in Equation (3) dominates, and the drain-to-source voltage can quickly get out of hand if the duty cycle is not limited by the controller.

Active-Clamp Circuit

As with the flyback converter, most of the energy stored in the primary leakage inductance is recycled in the clamp capacitor instead of being wasted in a lossy snubber. However, contrary to the flyback converter, in which the clamp capacitor resonates with the leakage inductance, in the forward converter the clamp capacitor resonates with the series combination of the leakage and magnetizing inductances. Typically, the leakage inductance is equal to 1 to 2% of the magnetizing inductance, so the value of the magnetizing inductance dominates. The clamp frequency of the forward converter is given by

$$f_{clamp} = \frac{1}{2\pi\sqrt{L_{magnetizing} \times C_{clamp}}}. \tag{11}$$

The clamp resonance occurs while Q1 is off and Q2 is on. This produces the distinctive "hump" on the drain waveform of Q1. Using a clamp capacitor that is too small allows the magnitude of the hump to become excessive. However, a clamp capacitor that is too large can create problems due to a sluggish duty-cycle response to large-signal changes [7]. The magnitude of the "hump" is given by

$$V_{hump} = \frac{V_{IN} \times D \times (1-D)}{8 \times L_{magnetizing} \times f^2 \times C_{clamp}}. \tag{12}$$

Soft Switching

Inspecting the transitions of the switching waveforms reveals some of the power-saving advantages of using the active-clamp topology in a
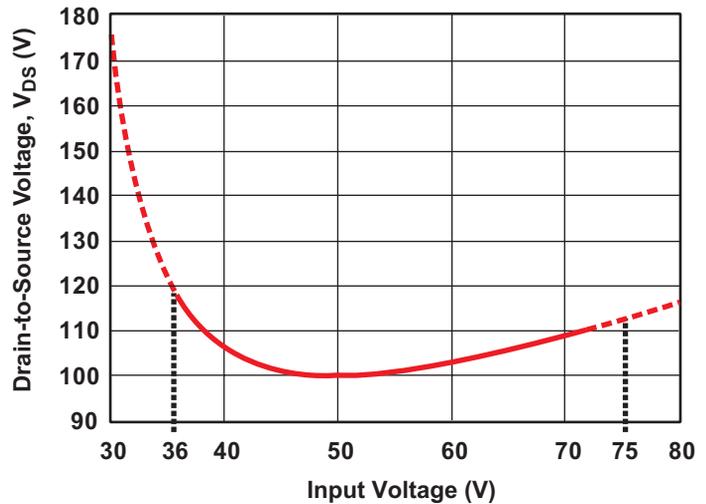

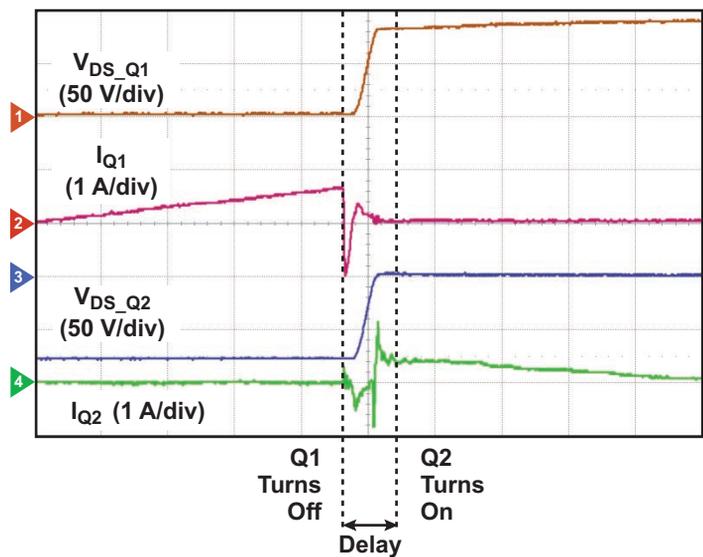Fig. 21. Duty cycle clamped at 70% with input below 36 V.

Fig. 22. Forward converter's primary-side switching waveforms as Q1 turns off.

forward converter. The main power-handling FET on the primary is Q1. Before Q1 turns off, the sum of the magnetizing current and the reflected output current is flowing through Q1. After Q1 turns off, this combined current is commutated through the clamp capacitor and body diode of Q2. After a small delay time, Q2 is turned on with zero voltage across its drain to source. This is shown in Fig. 22, which provides a close-up view of this transition.

This switching event results in zero-voltage switching of Q2 under all loading conditions.

The other switching transition, Q1 turning on, is more complicated and may or may not result in zero-voltage switching, depending on the load current. Before this switching event occurs, both Q2 and Q5 are on. After Q2 is switched off, the transformer's winding voltage falls, and Q5 is subsequently turned off. During heavy-load conditions, the output inductor current continues to flow through the body diodes of Q4 and Q5. This clamps the transformer's winding voltage to a low level, preventing zero-voltage switching of Q1. This can be seen in Fig. 23, where the drain voltage of Q1 is clamped to the input-voltage level during the delay period.

At lighter loads, the output inductor current is flowing in the reverse direction before Q2 is turned off. After Q2 and Q4 are turned off, the inductor current is blocked by the body diodes of the synchronous rectifiers. Since the winding voltage is no longer clamped, the drain voltage on Q1 is allowed to fall all the way to ground before Q1 is turned on. This results in zero-voltage switching of Q1 as shown in Fig. 24. It is possible to obtain zero-voltage switching of Q1 over the entire load range by using a very small output inductance. However, the resulting excessive peak currents make this impractical.

Self-Driven Synchronous Rectification

The turns ratio and input-voltage range determine the voltage stress on the two synchronous FETs, which (neglecting the effect of the clamp resonance) can be calculated as

$$V_{DS\_Q4} = V_{IN} \times \frac{D}{1-D} \times \frac{N_{sec}}{N_{pri}} \qquad (13)$$

and

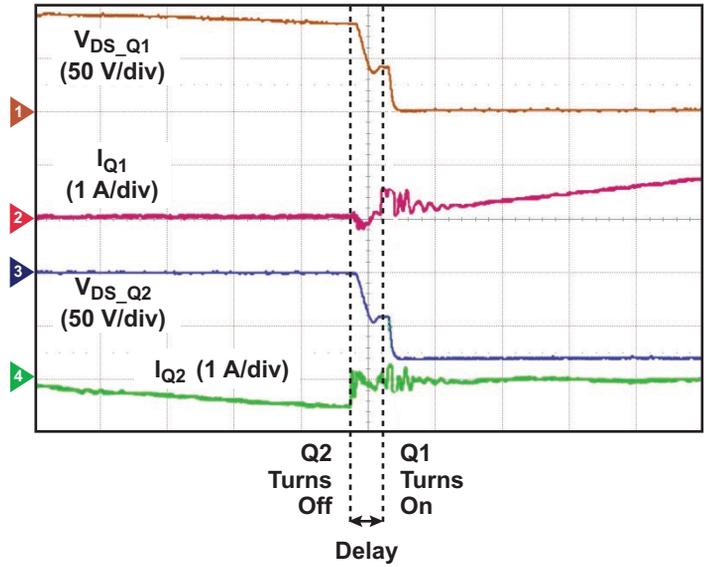$$V_{DS\_Q5} = V_{IN} \times \frac{N_{sec}}{N_{pri}}. \qquad (14)$$

Fig. 23. Forward converter's primary-side switching waveforms as Q1 turns on during heavy-load operation.
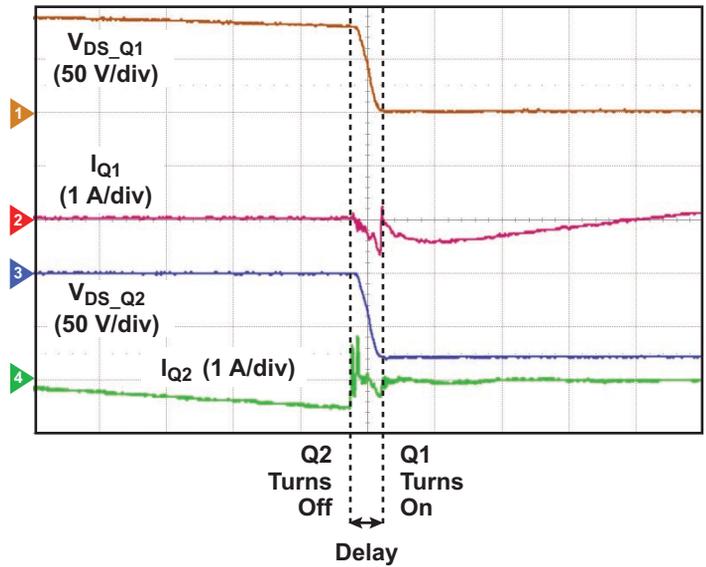

Fig. 24. Forward converter's primary-side switching waveforms as Q1 turns on during no-load operation.

In Fig. 25, these voltage stresses are plotted for a 3.3-V application using a 6:1 turns ratio. In this situation, FETs rated for 20 V_{DS} would easily suffice for both synchronous rectifiers.

In order to implement self-driven synchronous FETs, the drain of Q4 is connected to the gate of Q3, and the drain of Q3 is connected to the gate of Q4. This eliminates the clunky circuitry associated with sending the gate-drive signals across the isolation boundary from the controller. The gate-drive voltages need to be sufficiently high to ensure that the FET is fully enhanced over the entire line range. In addition, the gate voltage must be low enough to prevent an overvoltage condition at the gate. Using FETs with fast turn-off times is critical. If not fast enough, both synchronous FETs can be on simultaneously during the transitions, resulting in excessive shoot-through current. Turn-on time is not as critical, as the body diode will allow the proper flow of current, with one exception. During light-load operation, the inductor current is reversed when Q4 is turned on. This can result in a voltage spike on the secondary if Q4 turns on too slowly. Sometimes small gate resistors may be added to filter high-frequency noise spikes from the gates of the synchronous rectifiers. If a gate resistor is used, a parallel diode should also be added to allow a quick turn-off time.

At higher output voltages, the secondary voltages become more difficult to manage. For example, a 12-V output with a 1.88:1 turns ratio results in the voltage stresses shown in Fig. 26. For this example, 60-V FETs could be used. However, additional circuitry is required to prevent catastrophic damage to the gates of the synchronous rectifiers. Fig. 27 shows a simple gate-drive-conditioning circuit. The Zener diode, D8, clamps the gate voltage to an acceptable level, while Q6 provides a high-gain path to turn on the FET. Diode D7 provides a path to quickly discharge the gate and turn off the synchronous rectifier. If needed, a small capacitor can be added in parallel with R3 to speed up the turn-on transition. The power losses in the gate-drive components can be calculated as follows:

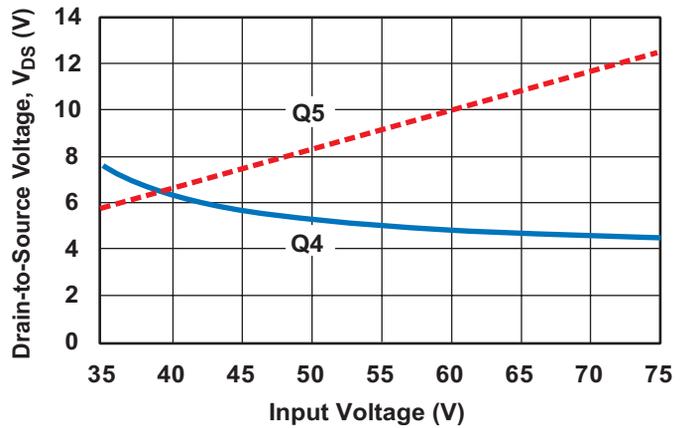$$P_{R3} = D \times \frac{(V_{DRV} - V_{D8})^2}{R3} \qquad (15)$$

Fig. 25. Voltage stresses on 3.3-V synchronous rectifiers.
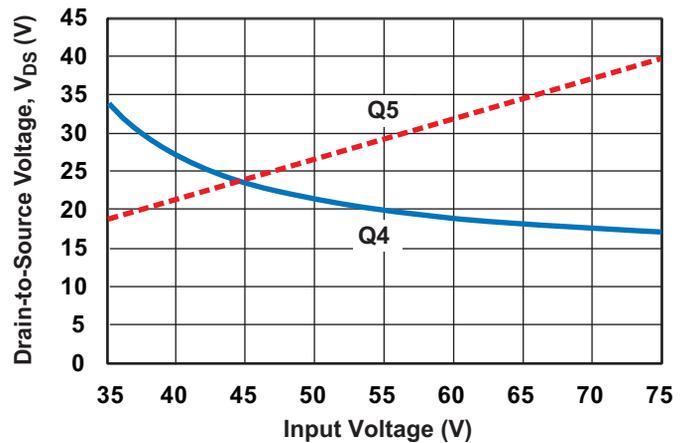

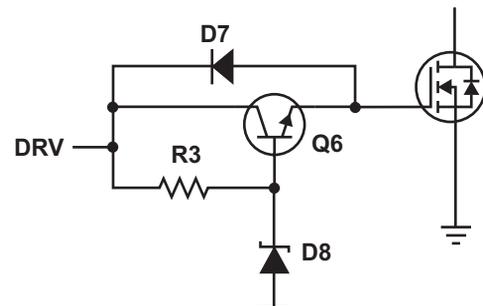
Fig. 26. Voltage stresses on 12-V synchronous rectifiers.

Fig. 27. Gate-drive-conditioning circuit for a forward converter.

$$P_{D7} = D \times V_{D7} \times \frac{V_{DRV} - V_{D8}}{R3} \qquad (16)$$

$$P_{Q6} \approx Q_{gate} \times f_{sw} \times (V_{DRV} - V_{D7}) \qquad (17)$$

At very high output voltages, losses in the gate-drive circuitry become excessive. At these voltages, currents are typically lower, and diodes are a better choice for the secondary switching devices. Alternatively, controller-driven synchronous rectifiers could be used. Table 3 lists the FET voltage ratings for common output-voltage levels.

TABLE 3. SYNCHRONOUS-FET RATINGS FOR COMMON OUTPUT VOLTAGES

Output Voltage (V)	Primary-to-Secondary Turns Ratio	Synchronous FET V_{DS} (V)
3.3	6:1	20
5	4.5:1	30
12	1.88:1	60

Examples of Forward-Converter Design

The schematic in Fig. 28 (see next page) shows a design example of a 3.3-V, 7.6-A active-clamp forward converter for PoE applications. The circuit is very similar to the example 3.3-V active-clamp flyback converter previously discussed. The biggest difference is the secondary side of the power stage. The synchronous rectifiers consist of two 6-mΩ FETs in small QFN 3.3 × 3.3-mm plastic packages. These FETs are rated for a V_{DS} of 25 V.
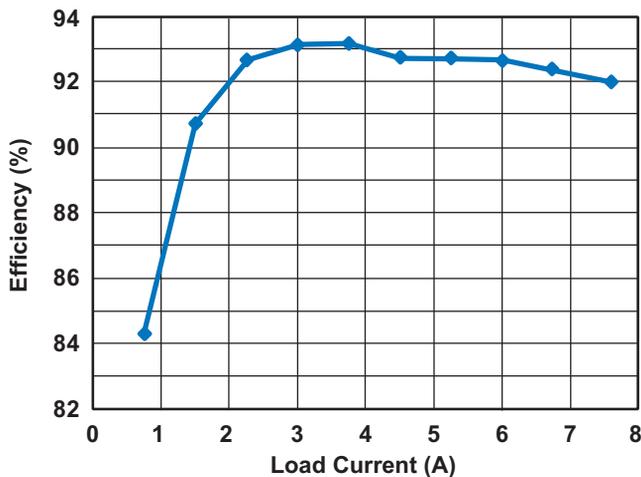
Some 10-Ω gate resistors were added to the gates of the synchronous FETs to filter any high-frequency voltage spikes. The resulting efficiency, shown in Fig. 29, peaks at 93% at 3.5 A with a 48-V input. With a high efficiency, this supply consumes less of the limited input power, allowing the load to use more.

In the forward converter, the active-clamp circuit conditions the transformer's winding voltage during the reset portion of the switching cycle. This provides a smooth and predictable voltage that is ideal for driving synchronous rectifiers directly from the power transformer. Without an active clamp, the drive signals for the synchronous rectifiers are typically sent from the primary-side controller across the isolation boundary and require significant additional circuitry. For more information on forward converters with the RCD clamp, see References [8] and [9].

The schematic in Fig. 30 (see page 2-20) shows a design example of a 12-V, 2.1-A active-clamp forward converter for PoE applications. This design uses 60-V synchronous rectifiers and requires the gate-drive-conditioning circuit. The resulting efficiency, shown in Fig. 31, peaks at 92%, compared to only 87% for a 12-V forward converter with an RCD clamp and diode rectifiers. Compared to the 3.3-V active-clamp forward converter, the extra loss associated with the gate-drive-conditioning circuit offsets the lower conduction losses that are due to the lighter load current.

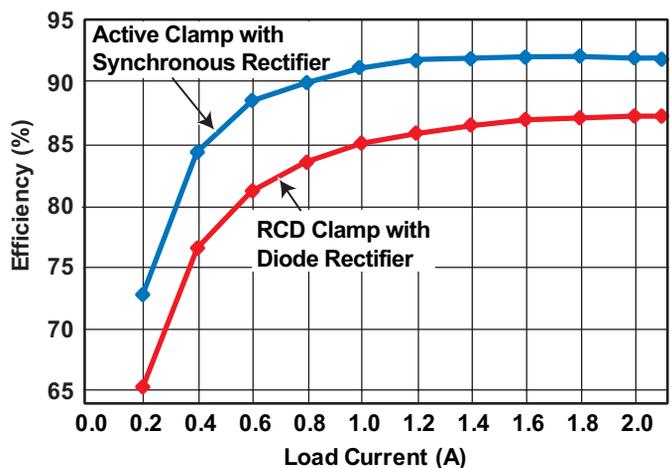Fig. 29. Efficiency of 3.3-V active-clamp forward converter.

Fig. 31. Efficiency of 12-V forward converter.

Fig. 28. Schematic of a 3.3-V, 7.6-A active-clamp forward converter for PoE applications.
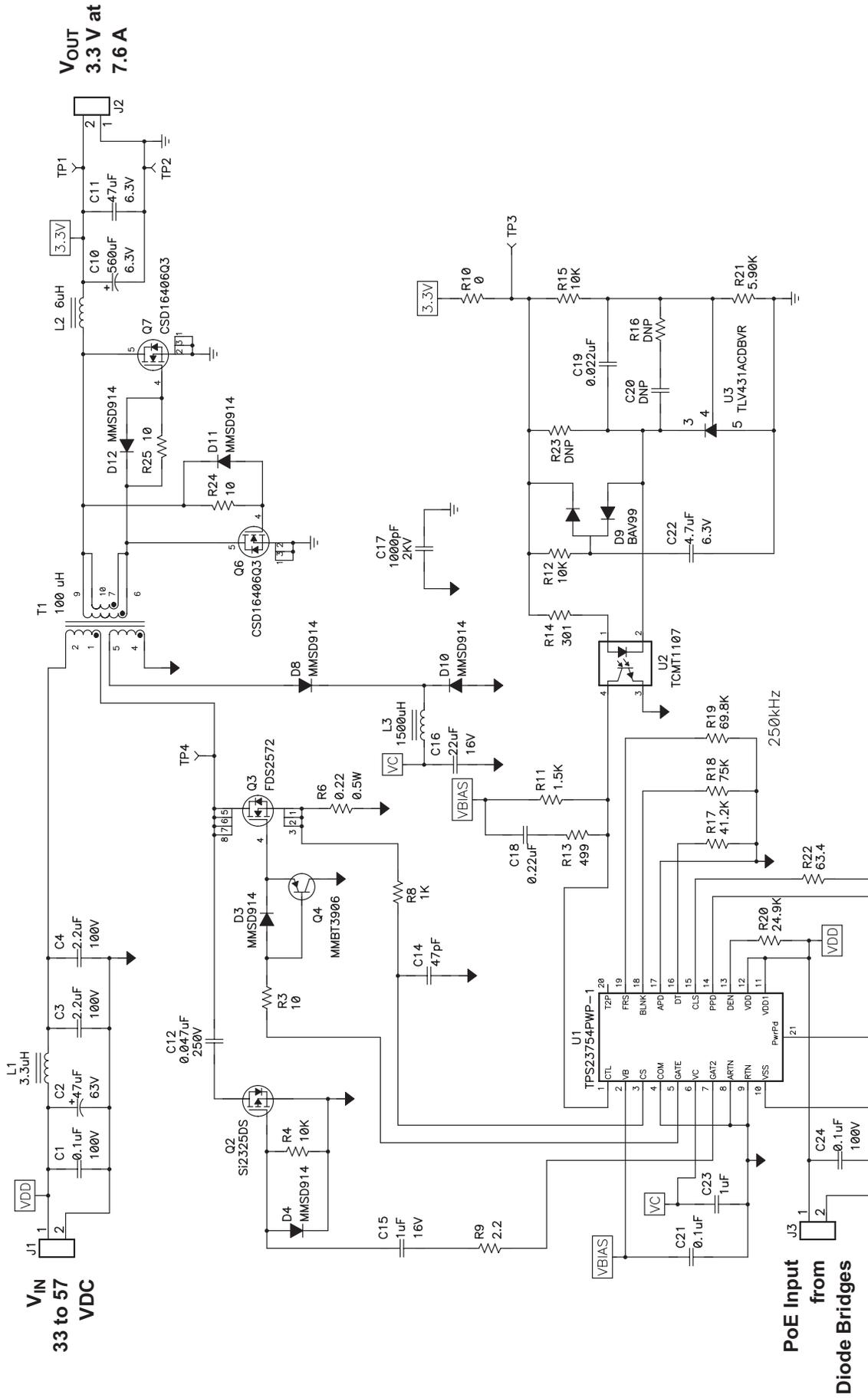
Fig. 30. Schematic of a 12-V, 2.1-A active-clamp forward converter for PoE applications.

III. Choosing the Right Converter

With the addition of an active-clamp circuit and synchronous recti-fiers, the flyback and forward con-verters can both achieve efficiencies of greater than 90%. Higher conduction losses in the flyback converter give the forward topology better efficiency, particularly at lower output voltages. In addition, using a flyback converter with synchronous FETs and an active-clamp circuit raises other concerns that require a more complicated design.

A. Converter Size

Fig. 32 shows the difference in the size of the two topologies. The primary components of both converter types are almost identical, with two major differences. First, the flyback converter requires a larger reset FET due to higher peak and RMS currents in the clamp circuit. Second, the bias voltage on the forward converter requires two rectifiers and an inductor, whereas the bias voltage on the flyback converter needs only a single rectifier. The flyback converter is larger because it has a larger power transformer and requires more ceramic capacitors on the output to handle a much larger RMS current. The forward converter's power transformer is smaller because it operates in the first and third quadrants and does not store energy, but a larger output inductor is required to store energy. The flyback inductor is for filtering only and does not need to store energy.
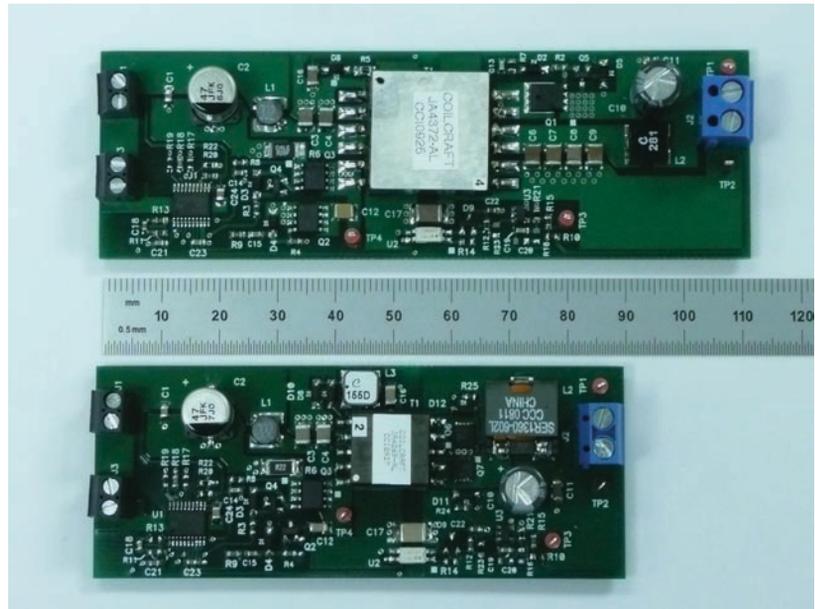

Fig. 32. Size comparison of flyback (top) and forward (bottom) converters.

B. Converter Cost

Table 4 compares the relative cost of the fly-back and forward converters. The forward converter has higher costs associated with a larger output inductor and a bias inductor. Even though the forward converter uses two synchronous FETs, they are smaller than the single, larger synchro-nous FET used in the flyback converter; so cost is about the same for either converter. The flyback converter has higher costs due to a larger trans-former, more ceramic output capacitors, and a larger reset FET. For low-voltage outputs at a power level of 25 W, the forward converter has the cost advantage.

TABLE 4. COST COMPARISON OF FLYBACK AND FORWARD CONVERTERS

Component	Flyback Converter		Forward Converter	
	Size	Cost	Size	Cost
Power Transformer	EFD20	$$$	EP13	$$
Output Inductor	Smaller	$	Larger	$$
Bias Inductor	—	—	Small	$
Reset FET	SO-8	$$	SOT-23	$
Synchronous FET	One PWRPAK SO-8	$$	Two 3 × 3-mm QFNs	$$
Ceramic Output Capacitors	Four 1210	$$$$	One 1206	$

With a 12-V output at 25 W, using a diode rectifier and an RCD clamp is a viable option for the flyback converter. The reset FET and synchronous FETs are replaced with less expensive diodes. The drive circuits for both FETs are also eliminated. In this case the cost advantage goes to the flyback converter.

The added efficiency resulting from lower internal losses can also result in additional cost savings from reduced heat-sinking requirements. At the 25-W power level, heat sinking is usually not required, but at higher power levels significant cost savings can be realized.

C. Converter Efficiency

Fig. 33 compares typical efficiencies that can be achieved with different topologies from a 48-VDC source. At lower power levels, the diode-rectified flyback converter is very cost-effective and usually provides acceptable efficiency, but it is generally limited to a maximum output current of 3 A due to losses in the output diode. Adding synchronous rectifiers and an active clamp extends the flyback converter's range to about 35 W regardless of the output voltage. At power levels of 25 W and higher, the active-clamp forward converter with synchronous rectifiers provides the most efficient solution.

It is interesting to note that at these higher power levels, there is an overlap between the possible topologies. For 3.3-V and 5-V outputs, the forward converter is usually the best choice. However, for a 12-V output, the difference in efficiency is not as significant. If cost is the overriding requirement, a diode-rectified flyback converter is usually selected for a 12-V output. If efficiency is the main concern, the synchronous forward converter is the clear choice for a 12-V output.

In general, if cost is more important than size or efficiency, the flyback converter is usually the best choice. If the only goal is maximizing efficiency, the forward converter is usually best. However, the flyback converter provides excellent cross-regulation for multiple output supplies, eliminating the need for postregulators. Restrictions on the leakage inductance and clamp-capacitor values for the flyback converter suggest that an active clamp is not suitable for low-leakage flyback transformers.
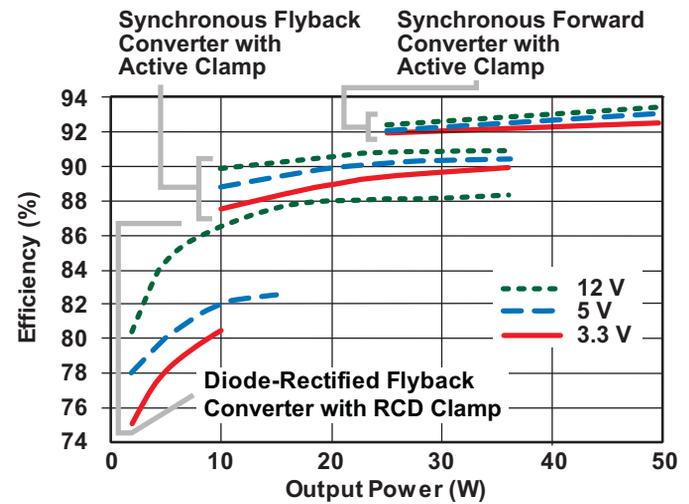

Fig. 33. Efficiency comparisons of flyback and forward converters.

IV. Acknowledgments

V. References

[1] John Betten and Brian King, "Benefits of Adding an Active Clamp to a Synchronous Flyback Power Supply," *EDN*, Dec. 14, 2006[Online]. Available: www.edn.com/article/461729-Benefits_of_adding_an_active_clamp_to_a_synchronous_power_supply.php

[2] Robert Kollman, "Achieving High Efficiency with a Multi-Output CCM Flyback Supply Using Self-Driven Synchronous Rectifiers," Unitrode Power Supply Design Seminar, 2003, TI Literature No. SLUP204

[3] Eric Wright, "Designing with the TPS23753 Powered-Device and Power Supply Controller," Application Report, TI Literature No. SLVA305A

[4] Yuri Panov and Milan Jovanovic, "Small Signal Analysis and Control Design of Isolated Power Supplies With Optocoupler Feedback," presented at Applied Power Electron. 2004 Conf., Anaheim, CA, Session 20.

[5] John Betten and Brian King, "Boost Efficiency for Low-Cost Flyback Converters," *EDN*, April 2, 2008 [Online]. Available: www.edn.com/article/472292-Boost_efficiency_for_low_cost_flyback_converters.php

[6] Lisa Dinwoodie, "Design Review: Isolated 50 Watt Flyback Converter Using the UCC3809 Primary Side Controller and the UC3965 Precision Reference and Error Amplifier," Application Note, TI Literature No. SLUA086

[7] Qiong M. Li, Fred C. Lee, and Milan M. Jovanovic, "Large Signal Transient Analysis of Forward Converter With Active-Clamp Reset," *IEEE Trans. Power Electron.*, Vol. 17, No. 1, pp. 15–24, Jan. 2002.

[8] Christopher Bridge, "The Implication of Synchronous Rectifiers to the Design of Isolated, Single-Ended Forward Converters," Unitrode Power Supply Design Seminar, 2001, TI Literature No. SLUP175

[9] C. S. Leu, F. C. Lee, and Chen Zhou, "Analysis and Design of R-C-D Clamp Forward Converter," *High Frequency Power Conf.*, San Diego, CA, May 1992, pp. 198–208.

[10] Dhaval Dalal, "Design Considerations for Active Clamp and Reset Technique," TI Literature No. SLUP112

[11] John Bottrill, "The Effects of Turning Off a Converter with Self-Driven Synchronous Rectifiers," *Bodo's Power Systems*, May 2007, pp. 34–36.

[12] John Bottrill, "A Discussion of the Active Clamp Topology," *Bodo's Power Systems*, Sept. 2007, pp. 46–49.

Topic 2