Accurate Point-of-Load Voltage Regulation Using Simple Adaptive Loop Feedback

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Introduction

Accurate point-of-load (POL) voltage control is essential for highly dynamic electronic loads. 'Adaptive loop' is a technique for efficient, feed-forward compensation of isolated power management systems based on PRM™ Regulator and VTM™ Voltage Transformer combinations. This application note describes the design methodology for optimal DC set point compensation of PRM and VTM combinations[a], including small arrays of two identical VTMs driven by one PRM.

For your reference, an automated spreadsheet version of the following procedure is available at www.vicorpower.com/dcaldesign.

Adaptive Loop Regulation Concept

Adaptive loop is a model-based, positive-feedback compensation technique that can easily complement negative feedback, voltage mode regulation. Figure 1 shows the conceptual block diagram.

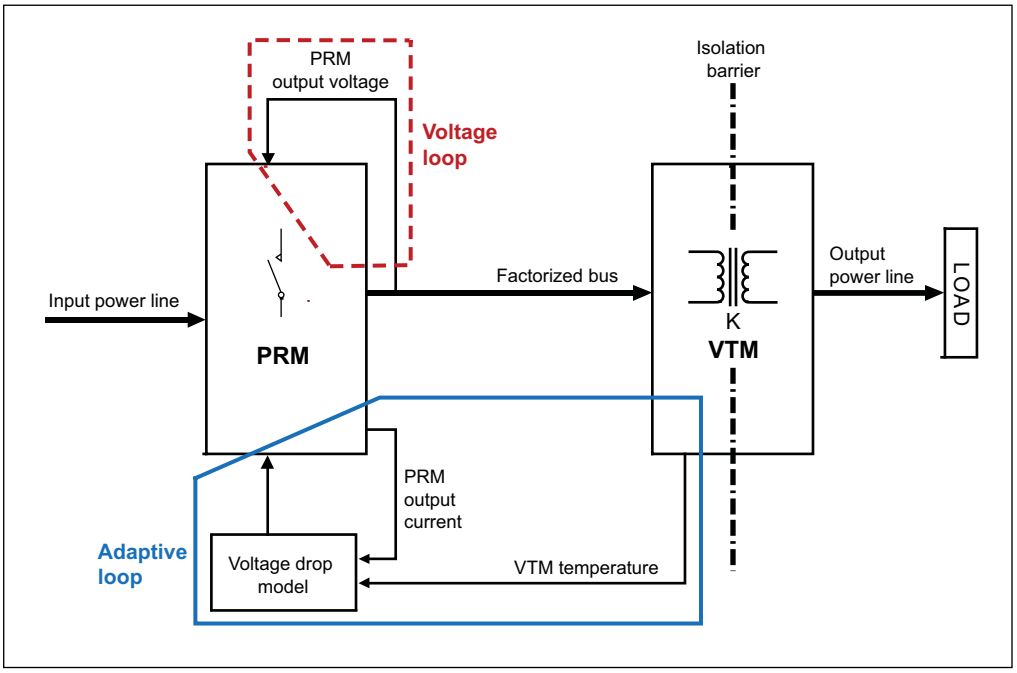


Figure 1
Adaptive loop regulation conceptual diagram

While the local voltage feedback loop maintains regulation at the PRM output, the adaptive loop (AL) provides compensation for the voltage drops that occur from the PRM output to the actual load. As stated before, AL is based on a model that requires VTM temperature and factorized bus current as inputs. The resistive behavior of power lines (factorized bus and output line) as well as the VTM, enables accurate modeling of their voltage drops.

[a] The calculations represented in this application note apply to 24 V, 36 V and 48 V input PRMs. Though the same methodology applies to 28 V input MIL-COTS PRMs, care should be taken to apply the correct values. For further assistance, please contact a Field Applications Engineer via your local Technical Support Center.

Major benefits of this approach are:

- No signals need to be transmitted across VTM's isolation barrier
- Simpler circuit, lower component count

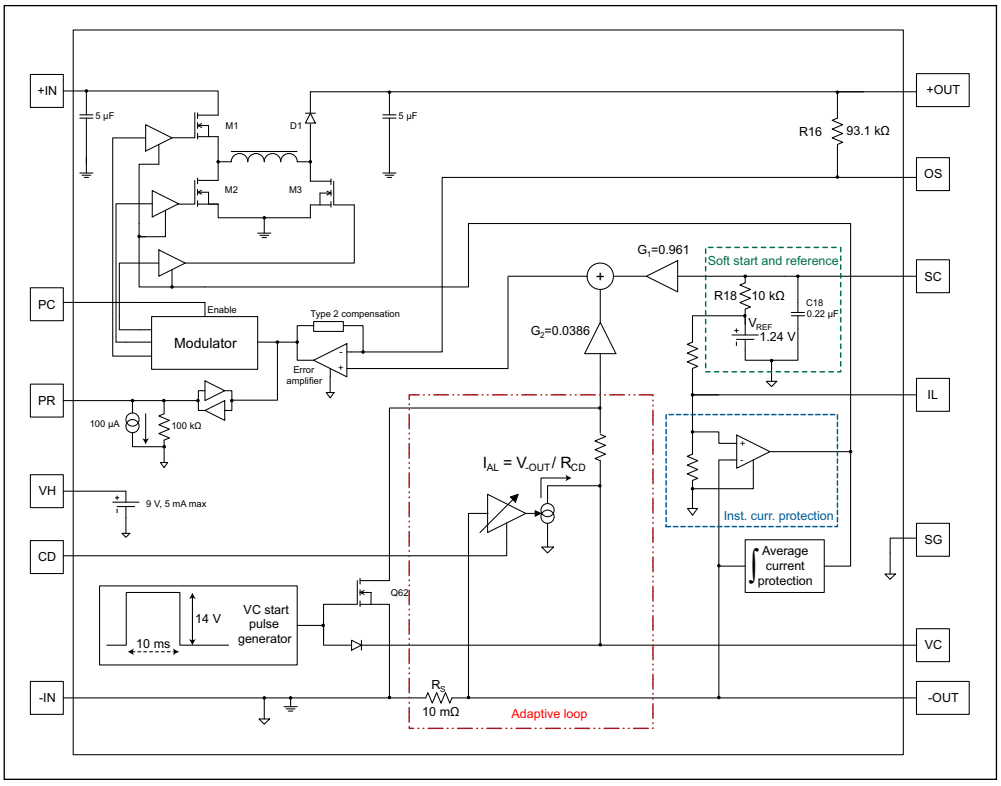
Regulation accuracy is affected by the accuracy of this model; this application note explains how to optimize the model for a given system, and how to estimate the obtained accuracy.

Standard regulation techniques are based on direct observation and integral error compensation of POL voltage, and the steady state error (compared to the reference) is therefore forced to be zero. AL only asymptotically approaches the zero error state, therefore widening the total distribution of the POL voltage.

PRM-AL Block Diagram

Figure 2 shows the functional block diagram for a full-chip PRM-AL regulator (e.g. P045F048T32AL). The OS and SC pins provide for local voltage feedback loop setting, while the VC and CD pins provide for settings and connections of the downstream system model.

Figure 2
PRM-AL functional block diagram



In summary:

- Local voltage feedback loop:
  - V_{REF}, through R18, provides a reference voltage source on the SC pin. This is routed to the non-inverting input of the error amplifier, through the gain stage G1.
  - The factorized bus (+OUT) voltage is fed back to the inverting input of the error amplifier through R16.
  - SC and OS provide for the connection of the external resistor dividers.

- Adaptive loop circuit:

– The voltage controlled current source has variable gain, controlled by the resistance connected between CD and signal ground (SG) pins. The current injected on the VC line by the variable gain transconductance amplifier is:

— directly proportional to the voltage across the sense resistor R_S

— inversely proportional to the resistor connected between CD and SG

according to the following relationship:

Equation 1

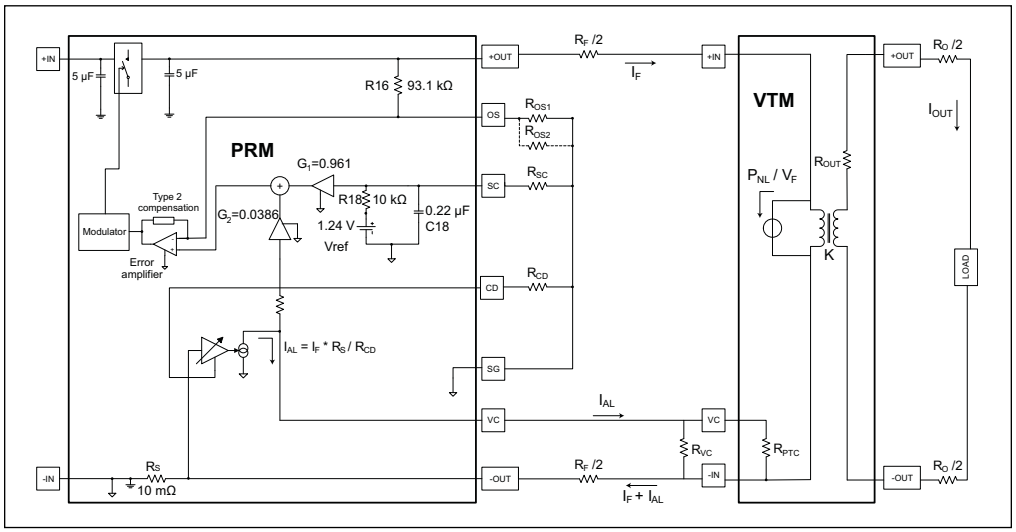
$$I_{AL} = \frac{V_{-OUT}}{R_{CD}} = \frac{R_S I_F}{R_{CD}}$$

where I_F is the factorized bus (PRM output) current and V_{-OUT} is the voltage drop across R_S.

– The VC pin voltage is added to the reference pin voltage SC through the gain stage G_2.

A PRM and VTM system is considered, as shown in the block diagram in Figure 3. The system PCB adds further voltage drops from the PRM output to the load: the factorized bus resistance, R_F, and the output line resistance, R_O, which are assumed to be constant and equally divided on the positive and negative trace / wire. In order to account for them, these resistances must be estimated or measured.

Figure 3
Factorized Power Architecture (FPA™) system with adaptive loop control block diagram



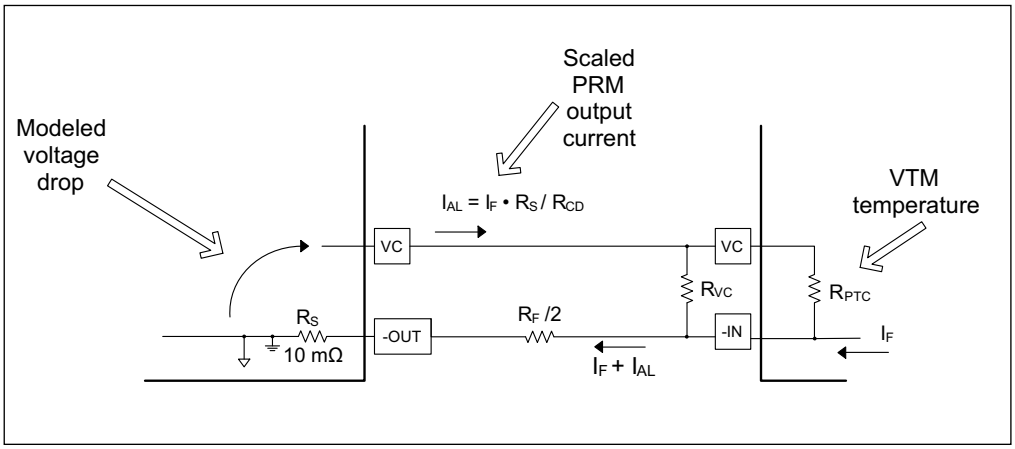
It is important to correctly identify the total voltage drop parameters, which are R_F, R_{OUT} and R_O in this specific case. Their compensation model must therefore be resistive, and temperature dependent.

Such a model is easy to implement, thanks to:

- The PTC resistor embedded in the VTM module, which will change its value according to the VTM temperature.
- R_{VC} resistor, which allows precise match of R_{PTC} to VTM R_{OUT} temperature characteristic.

The parallel of R_{VC} and R_{PTC} resistors, in series with $R_F/2$ and R_S resistors constitutes the voltage drop model. The AL circuitry forces a scaled version of the PRM output current (I_{AL}) in the VC line, which then merges with the factorized bus current I_F on its return path (as shown in Figure 4).

Figure 4
Voltage drop model for the considered system



The voltage obtained on the VC pin, with some scale factor, is the model of the total voltage drop in the system.

DC Set Point Calculation

The necessary inputs to the procedure are shown in Table 1.

Table 1
Adaptive loop calculation procedure inputs

Standard Full-Chip VTM Characteristics	Power System Characteristics
• R_{OUT_25}: 25°C output resistance • R_{OUT_100}: 100°C output resistance • K: transformer ratio • R_{PTC_25}: PTC resistance at 25°C • R_{PTC_100}: PTC resistance at 100°C • P_{NL}: no load power dissipation at nominal input voltage	• V_{F_NOM}: nominal factorized bus voltage at no load • I_{OUT}: maximum system (VTM) output current • R_F: factorized bus (PRM to VTM) total resistance • R_O: output bus (VTM to point of load) total resistance

Table 2 summarizes the data for standard full-chip VTM transformers. It is important to note that the internal resistors in the PRM have 1% tolerance.

Table 2
Standard full-chip VTM data required (typical)

VTM Part Number	Output Resistance			Temperature Sensor		
	R_{OUT_25}	R_{OUT_100}	Tolerance	R_{PTC_25}	Temp. Coeff.(TCR)	Tolerance
	[mΩ]	[mΩ]	[%]	[Ω]	[%/°C]	[%]
V048F015T100	0.99	1.17	11	3000		
V048F020T080	1.31	1.56	10	2000		
V048F030T070	1.61	1.97	10	1000	0.39	5
V048F040T050	2.76	3.29	8			
V048F060T040	5.76	6.73	5			
V048F080T030	7.54	8.76	8	560		
V048F096T025	9.84	11.97	10			
V048F120T025	10.85	13.39	6	510		
V048F160T015	29.76	32.80	7			
V048F240T012	48.11	57.17	4			
V048F320T009	79.48	96.10	6			
V048F480T006	177.44	215.63	5			

With reference to Figure 3:

A. Calculate the maximum voltage drop (at 25ºC and 100ºC) due to VTM output resistance R_{OUT}.

Equation 2

$$\Delta V_{ROUT\_25} = R_{OUT\_25} \cdot I_{OUT}$$

Equation 3

$$\Delta V_{ROUT\_100} = R_{OUT\_100} \cdot I_{OUT}$$

B. Calculate the maximum current flowing on the factorized bus.

Equation 4

$$I_F = K \cdot I_{OUT} + \frac{P_{NL}}{V_{F\_NOM}}$$

Although the no load power (P_{NL}) required by the VTM is input voltage dependent, the variation has only a minor influence on the AL compensation, and will therefore be neglected in the following steps.

C. Calculate the total PRM output voltage increase that will compensate all the drops (factorized bus resistance, VTM output resistance and output bus resistance).

Equation 5

$$\Delta V_{F\_25} = \frac{\Delta V_{ROUT\_25} + R_O I_{OUT}}{K} + (R_F + R_S) \cdot I_F$$

Equation 6

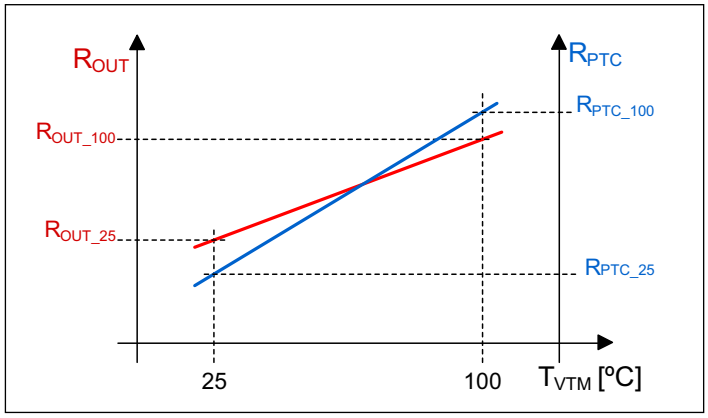
$$\Delta V_{F\_100} = \frac{\Delta V_{ROUT\_100} + R_O I_{OUT}}{K} + (R_F + R_S) \cdot I_F$$

D. Calculate the total temperature coefficient of the power circuit and the R_{VC} resistor needed to match it.

The PTC resistor and the VTM R_{OUT} resistance are subject to the same temperature, but they have different rates of change, as shown in Figure 5.

Figure 5

R_{OUT} and R_{PTC} vs. VTM internal temperature



In order for the model to precisely match the voltage drop over temperature, its slope must match the system slope. The R_{VC} resistor in parallel to R_{PTC} can be calculated in order to meet this condition.

$$\Delta R_{TOT} = \frac{\Delta V_{F\_100}}{\Delta V_{F\_25}} = \frac{\frac{R_{VC} \cdot R_{PTC\_100}}{R_{VC} + R_{PTC\_100}}}{\frac{R_{VC} \cdot R_{PTC\_25}}{R_{VC} + R_{PTC\_25}}} \quad \Rightarrow$$

Equation 7

$$R_{VC} = (1 - \Delta R_{TOT}) \frac{R_{PTC\_25} \cdot R_{PTC\_100}}{\Delta R_{TOT} \cdot R_{PTC\_25} - R_{PTC\_100}}$$

There is an important reason for choosing a parallel rather than a series resistor to match the system temperature coefficient. At start-up, the PRM issues a 14 V, 10 ms pulse on the VC line to synchronously start the VTM. A series resistor would cause significant amplitude change on this signal, avoided by the parallel arrangement. However, the designer should exercise judgment and avoid extreme cases, where the temperature dependency might be so low as to cause the R_{VC} value to fall below 200 Ω (which would cause overload during the 14 V, 10 ms startup pulse).

E. Calculate the maximum VC pin voltage for the given system at 25°C (100°C should provide the same value, given the temperature dependency has been taken care of through R_{VC}, [7]):

$$V_{C\_MAX\_25} = I_{AL} \cdot \frac{R_{PTC\_25} \cdot R_{VC}}{R_{PTC\_25} + R_{VC}} + (I_F + I_{AL}) \cdot \left(\frac{R_F}{2} + R_S \right) =$$

Equation 8

$$= R_S \frac{I_F}{R_{CD\_MIN}} \cdot \frac{R_{PTC\_25} \cdot R_{VC}}{R_{PTC\_25} + R_{VC}} + (I_F + R_S \frac{I_F}{R_{CD\_MIN}}) \cdot \left(\frac{R_F}{2} + R_S \right)$$

Minimum allowable R_{CD} value for current products is 20 Ω.

F. Calculate the needed (if any) V_{SC} trim that allows enough AL dynamic range under the worst case: $V_{C\_MAX\_25}$ and ΔV_{F_100} (this will allow enough design margin).

The voltage on VC, through the gain stage G_2, is summed to the reference voltage SC in order to compensate for the voltage drop ΔV_F. Because the VC voltage dynamic range is set, V_{SC} might be reduced in order to match the relative changes of factorized bus and adaptive loop compensation.

Equation 9

$$\frac{\Delta V_{F\_100}}{V_{F\_NOM}} \le \frac{G_2 \cdot V_{C\_MAX\_25}}{G_1 \cdot V_{SC}} \Rightarrow V_{SC} \le \frac{G_2 \cdot V_{C\_MAX\_25}}{G_1 \frac{\Delta V_{F\_100}}{V_{F\_NOM}}}$$

G_1 and G_2 gains are 0.961 and 0.0386 respectively.

If $V_{SC} \le V_{ref}$ = 1.24 V, the external resistor to be connected on SC will be easily calculated as following:

Equation 10

$$R_{SC} = R_{18} \frac{V_{SC}}{V_{ref} - V_{SC}}$$

The absolute minimum value for V_{SC} is 0.25 V, because of the characteristic of the internal error amplifier. The minimum resistance value for R_{SC} is therefore 2550 Ω.

G. Calculate the voltage feedback divider resistor needed to set the nominal output voltage.

Equation 11

$$V_{F\_NOM} = G_1 \cdot V_{SC} \frac{R_{16} + R_{OS}}{R_{OS}} \Rightarrow R_{OS} = G_1 \cdot R_{16} \frac{V_{SC}}{V_{F\_NOM} - G_1 \cdot V_{SC}}$$

R_{OS} defines the gain on the voltage feedback, which accommodates for the chosen reference voltage V_{SC}. It is recommended to calculate its value using the V_{SC} voltage obtained with a standardized value resistor as R_{SC}. Moreover, if a standard value resistor is not available to match (within 0.2%) the calculated R_{OS} value, it is strongly recommended to use a parallel configuration.

H. Calculate the R_{CD} resistor that allows AL to compensate for the drops (25°C or 100°C will give the same result, because of R_{VC}).

First, substitute the VC line voltage at full I_F current (room temperature):

Equation 12

$$V_{C\_25} = \frac{R_S \cdot I_F}{R_{CD}} \cdot \frac{R_{PTC\_25} \cdot R_{VC}}{R_{PTC\_25} + R_{VC}} + \left(\frac{R_S \cdot I_F}{R_{CD}} + I_F \right) \cdot \left(\frac{R_F}{2} + R_S \right)$$

into the expression for the related factorized bus increase:

$$\Delta V_{F\_25} = G_2 \cdot V_{C\_25} \frac{R_{16} + R_{OS}}{R_{OS}} =$$

$$= G_2 \cdot \frac{R_S \cdot I_F}{R_{CD}} \cdot \frac{R_{PTC\_25} \cdot R_{VC}}{R_{PTC\_25} + R_{VC}} + \left(\frac{R_S \cdot I_F}{R_{CD}} + I_F \right) \cdot \left(\frac{R_F}{2} + R_S \right) \frac{R_{16} + R_{OS}}{R_{OS}}$$

Then solve for R_{CD}:

Equation 13

$$R_{CD} = \frac{G_2 \frac{R_{16} + R_{OS}}{R_{OS}} R_S I_F \left(\frac{R_{PTC\_25} \cdot R_{VC}}{R_{PTC\_25} + R_{VC}} + \frac{R_F}{2} + R_S \right)}{\Delta V_{F\_25} - G_2 \frac{R_{16} + R_{OS}}{R_{OS}} \left(\frac{R_F}{2} + R_S \right) I_F}$$

Considerations

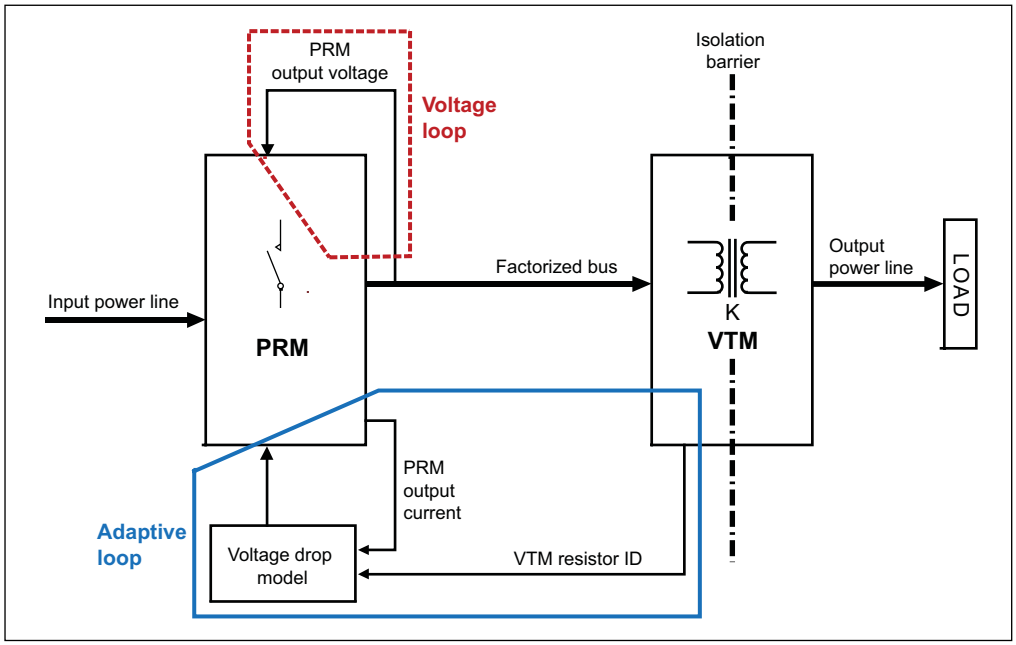
In order to improve regulation accuracy, the following guidelines should be followed:

- Discrepancy between the model and the system will directly affect regulation accuracy. System characterization is strongly recommended during the design phase, specifically factorized bus (R_F) and output line (R_O) resistances.
- Statistical distribution of components values plays also a key role on accuracy distribution. To this end, 'Monte Carlo' (or similar) analysis and optimization is strongly encouraged. It should include all the components directly affecting regulation, i.e. setting resistors, model resistors and component characteristics. Any extra component designed in the system, i.e. filter inductors, connectors, etc., should also be included if affected by variability.
- While the impact of R_S and R_F on VC voltage may be neglected in a few cases, it normally affects accuracy distribution. In order to evaluate it, both resistors should be included in the analysis.

Adaptive Loop with Half-Chip VTMs

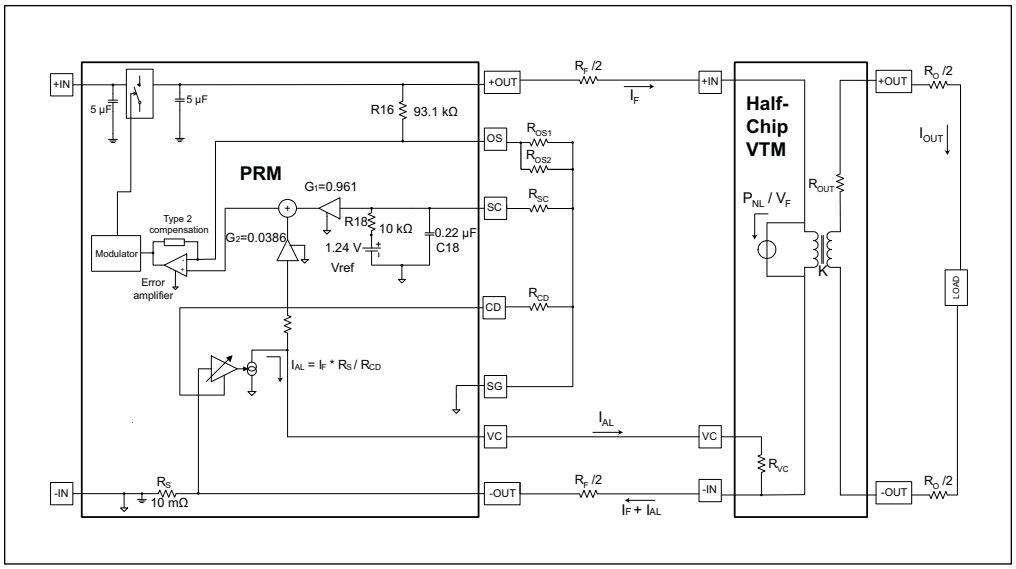
The major difference between full- and half-chip VTMs is the absence of temperature feedback. While the full-chip VTMs implement a PTC resistor, the half-chip modules use a simple precision resistor, as shown in Figure 6.

Figure 6
Adaptive loop regulation concept without temperature feedback



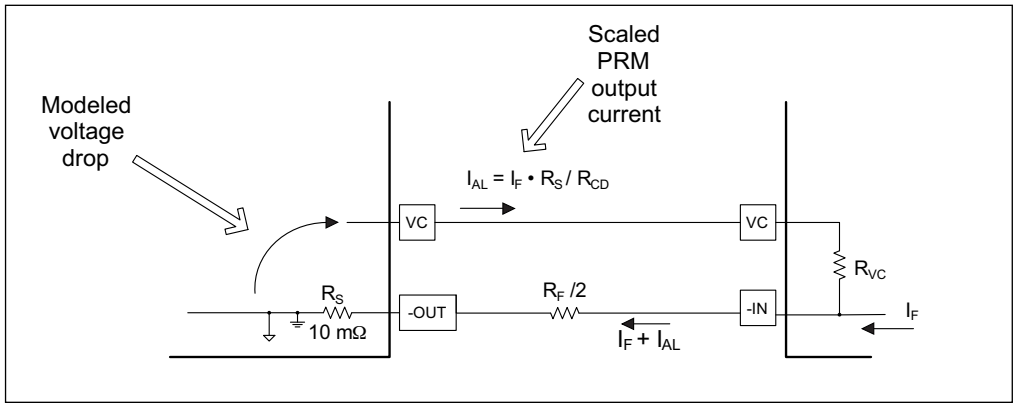
The absence of temperature feedback slightly degrades the regulation accuracy; however, the half-chip units have tighter parameter distributions, which partially compensate for the reduced model accuracy. The control configuration in this case is shown in Figure 7.

Figure 7
Adaptive loop control with half-chip VTM



The voltage drop model also differs with the one for the full-chip version (Figure 3), resulting in the simpler one shown in Figure 8.

Figure 8
Voltage drop model in systems with half-chip VTMs



Having explained the differences, it is now possible to revise the design procedure in this specific case. Table 3 shows the necessary inputs.

Table 3
Adaptive loop calculation procedure inputs for half-chip VTMs

Half-Chip VTM Characteristics	Power System Characteristics
• R_{OUT_25}: 25°C output resistance • R_{OUT_100}: 100°C output resistance • K: transformer ratio • R_{VC}: VTM VC pin internal resistance • P_{NL}: no load power dissipation at nominal input voltage	• V_{F_NOM}: nominal factorized bus voltage at no load • I_{OUT}: maximum system (VTM) output current • R_F: factorized bus (PRM to VTM) total resistance • R_O: output bus (VTM to point of load) total resistance

Table 4 summarizes the data for the half-chip VTMs.

Table 4
Half-chip VTM data required (typical)

VTM Part Number	Output Resistance			ID Resistor	
	R_{OUT_25}	R_{OUT_100}	Tolerance	R_{VC}	Tolerance
	[mΩ]	[mΩ]	[%]	[Ω]	[%]
VIV0102THJ	2.72	3.22	8	1430	1.0
VIV0103THJ	3.03	3.78	11	9310	
VIV0104THJ	6.86	8.07	8	8870	
VIV0105THJ	13.80	16.24	7	4640	
VIV0101THJ	44.32	57.65	6	2050	

For sake of clarity, only the steps that differ from the procedure already explained for the full-chip VTMs are reported.

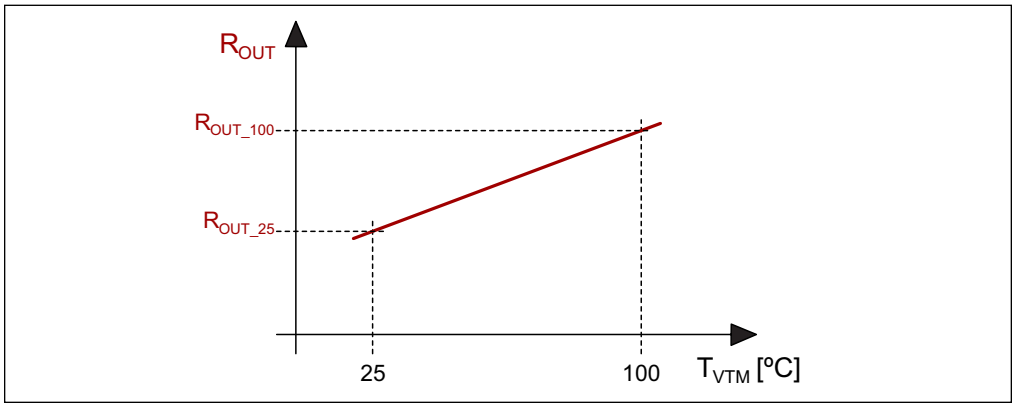
Step(s):

A., B., C.: unchanged

D. Calculate the total temperature coefficient of the power circuit at the estimated VTM working temperature.

The VTM R_{OUT} resistance is temperature dependent, as shown in Figure 9.

Figure 9
Half-chip VTM R_{OUT} vs. module internal temperature



In order for the model to match the system voltage drop better, the VTM operating temperature should be estimated. In cases where temperature is unknown, a conservative approach would be to assume the module will operate at half of its temperature range, for example 75ºC:

Equation 14

$$\Delta V_{F\_75} = \Delta V_{F\_25} + \frac{\Delta V_{F\_100} - \Delta V_{F\_25}}{75} \cdot 50$$

Linear interpolation used in [14] is acceptable in this case, as R_{OUT} temperature dependency is linear.

E. Calculate the maximum VC pin voltage for the given system.

Equation 15

$$V_{C\_MAX} = I_{AL} \cdot R_{VC} + (I_F + I_{AL}) \cdot \left(\frac{R_F}{2} + R_S \right) =$$

$$= R_S \frac{I_F}{R_{CD\_MIN}} \cdot R_{VC} + (I_F + R_S \frac{I_F}{R_{CD\_MIN}}) \cdot \left(\frac{R_F}{2} + R_S \right)$$

F., G.: unchanged

H. Calculate the R_{CD} resistor that allows AL to compensate for the drops.

First, substitute the VC line voltage at full I_F current (ambient temperature):

Equation 16

$$V_C = \frac{R_S \cdot I_F}{R_{CD}} \cdot R_{VC} + \left(\frac{R_S \cdot I_F}{R_{CD}} + I_F \right) \cdot \left(\frac{R_F}{2} + R_S \right)$$

into the expression for the related factorized bus increase:

$$\Delta V_{F\_75} = G_2 \cdot V_C \frac{R_{16} + R_{OS}}{R_{OS}} =$$

$$= G_2 \cdot \frac{R_S \cdot I_F}{R_{CD}} \cdot R_{VC} + \left(\frac{R_S \cdot I_F}{R_{CD}} + I_F \right) \cdot \left(\frac{R_F}{2} + R_S \right) \frac{R_{16} + R_{OS}}{R_{OS}}$$

Then solve for R_{CD}:

Equation 17

$$R_{CD} = \frac{G_2 \frac{R_{16} + R_{OS}}{R_{OS}} R_S I_F \left(R_{VC} + \frac{R_F}{2} + R_S \right)}{\Delta V_{F\_75} - G_2 \frac{R_{16} + R_{OS}}{R_{OS}} \left(\frac{R_F}{2} + R_S \right) I_F}$$

Design Example with V•I Chip Customer Boards

System requirements:

Input: 36-75 V
Output: 5 V, 36 A, 180 W

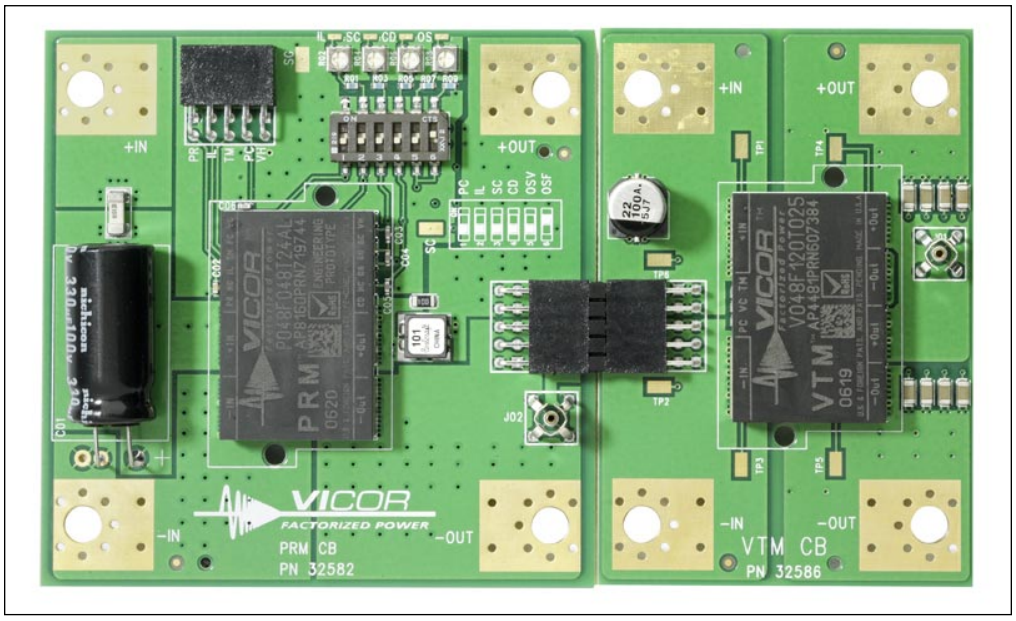
V•I Chip selection:

PRM: P048F048T24AL (due to the wide range input voltage and the power level).

VTM: V048F060T040 (due to output voltage and current requirements).

Corresponding customer boards are P048F048T24AL-CB and V048F060T040-CB respectively. They come with a connector which routes factorized bus and VC line, as explained in the User Guide UG:003. Figure 10 shows the two selected boards once connected.

Figure 10
PRM and VTM customer boards



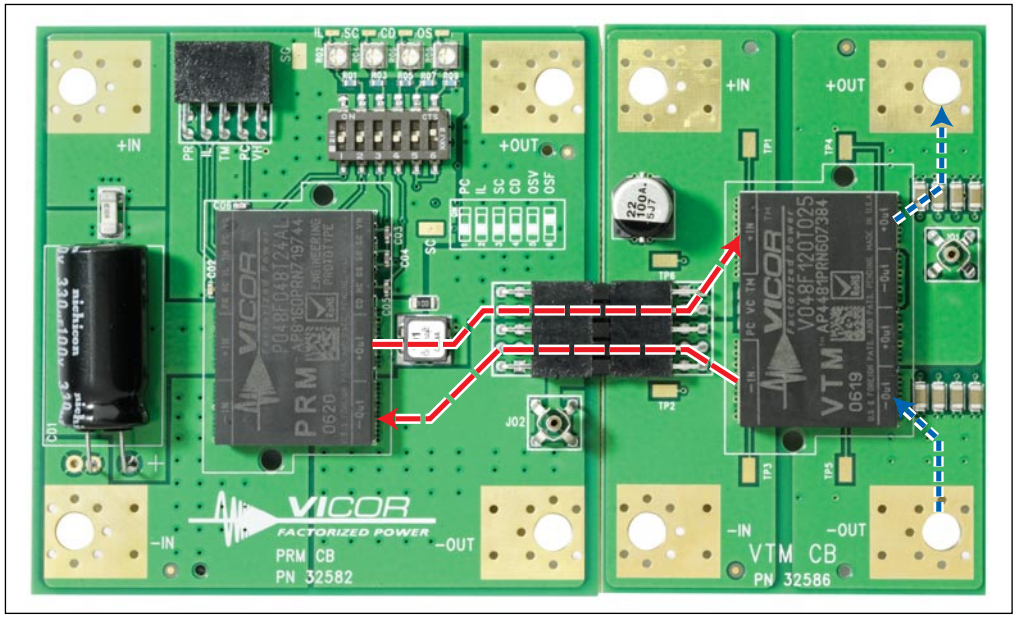
First, collect the characteristics from the VTM's data sheet and from Table 2:

- R_{OUT_25}: 5.76 mΩ
- R_{OUT_100}: 6.73 mΩ
- K: 1/8
- R_{PTC_25}: 1000 Ω
- R_{PTC_100}: 1000·(1+0.0039·75) = 1293 Ω
- P_{NL}: 2.7 W

Second, calculate or measure the power system characteristics:

- V_{F_NOM}: V_{OUT}/K = 40 V
- I_{OUT}: 36 A
- R_F and R_O: these values are strictly related to the board traces or cables used to route power. A convenient way to obtain these values is to identify the current paths of interest, as shown in Figure 11.

Figure 11
Factorized bus current path (long-dash red) and output current path (short-dash blue)



Then, a simple DC impedance measurement from terminal to terminal will provide R_F and R_O values. In this particular case:

➢ R_F= 10 mΩ

➢ R_O= 80 uΩ

It is now possible to apply the proposed procedure.

A. Calculate the maximum voltage drop (at 25°C and 100°C) due to VTM output resistance, R_{OUT}.

$$\Delta V_{ROUT\_25} = R_{OUT\_25} \cdot I_{OUT} = 0.00576 \cdot 36 = 0.207\ V$$

$$\Delta V_{ROUT\_100} = R_{OUT\_100} \cdot I_{OUT} = 0.00673 \cdot 36 = 0.242\ V$$

B. Calculate the maximum current flowing on the factorized bus.

$$I_F = K \cdot I_{OUT} + \frac{P_{NL}}{V_{F\_NOM}} = \frac{1}{8} \cdot 36 + \frac{2.7}{40} = 4.568\ A$$

C. Calculate the total PRM output voltage increase that will compensate all the drops (factorized bus resistance, VTM output resistance and output bus resistance).

$$\Delta V_{F\_25} = \frac{\Delta V_{ROUT\_25} + R_O I_{OUT}}{K} + (R_F + R_S)\cdot I_F = \frac{0.207 + 80\,\mu\cdot 36}{1/8} + (10\,m + 10\,m)\cdot 4.568 = 1.77\,V$$

$$\Delta V_{F\_100} = \frac{\Delta V_{ROUT\_100} + R_O I_{OUT}}{K} + (R_F + R_S)\cdot I_F = \frac{0.242 + 80\,\mu\cdot 36}{1/8} + (10\,m + 10\,m)\cdot 4.568 = 2.05\,V$$

D. Calculate the total temperature coefficient of the power circuit and the R_{VC} resistor needed to match it.

$$\Delta R_{TOT} = \frac{\Delta V_{F\_100}}{\Delta V_{F\_25}} = \frac{2.05}{1.77} = 1.158 \quad \Rightarrow$$

$$R_{VC} = (1 - \Delta R_{TOT})\frac{R_{PTC\_25}\cdot R_{PTC\_100}}{\Delta R_{TOT}\cdot R_{PTC\_25} - R_{PTC\_100}} = (1 - 1.158)\frac{1000\cdot 1293}{1.158\cdot 1000 - 1293} = 1513\ \Omega$$

The R_{VC} value is greater than 200 Ω, therefore valid. The nearest available 1% resistor value chosen for R_{VC} is 1500 Ω.

E. Calculate the maximum VC pin voltage for the given system at 25°C. From the PRM-AL data sheet, R_{CD_MIN} = 20 Ω:

$$V_{C\_MAX\_25} = R_S\frac{I_F}{R_{CD\_MIN}}\cdot\frac{R_{PTC\_25}\cdot R_{VC}}{R_{PTC\_25} + R_{VC}} + (I_F + R_S\frac{I_F}{R_{CD\_MIN}})\cdot\left(\frac{R_F}{2} + R_S\right) =$$

$$= 10\,m\frac{4.568}{20}\cdot\frac{1000\cdot 1500}{1000 + 1500} + (4.568 + 10\,m\frac{4.568}{20})\cdot\left(\frac{10\,m}{2} + 10\,m\right) = 1.44\,V$$

F. Calculate the needed (if any) V_{SC} trim that allows enough AL dynamic range under the worst case: $V_{C\_MAX\_25}$ and ΔV_{F_100}.

$$V_{SC} \le \frac{G_2\cdot V_{C\_MAX\_25}}{G_1\frac{\Delta V_{F\_100}}{V_{F\_NOM}}} = \frac{0.0386\cdot 1.44}{0.961\frac{2.05}{40}} = 1.12\,V$$

As $V_{SC} \le V_{ref}$ = 1.24 V, R_{SC} must be installed:

$$R_{SC} = R_{18}\frac{V_{SC}}{V_{ref} - V_{SC}} = 10\,k\frac{1.12}{1.24 - 1.12} = 93.3\,k\Omega$$

R_{SC} is greater than 2550 Ω, therefore acceptable. The closest 1% tolerance value is chosen, R_{SC} = 93.1 kΩ, which provides for an obtained V_{SC} = 1.12 V

G.Calculate the voltage feedback divider resistor needed to set the nominal output voltage.

$$R_{OS} = G_1 \cdot R_{16} \frac{V_{SC}}{V_{F\_NOM} - G_1 \cdot V_{SC}} = 0.961 \cdot 93.1\,k \frac{1.12}{40 - 0.961 \cdot 1.12} = 2574\ \Omega$$

The closest standard value would be 2550 Ω, which is almost 1% off the target. In order to gain accuracy, the highest standard value is chosen, 2610 Ω, and a parallel resistor is used in order to closely match the required value:

R_{OS1} = 2610 Ω and R_{OS2} = 187 kΩ

H.Calculate R_{CD} resistor that allows AL to compensate for the drops.

$$R_{CD} = \frac{G_2 \frac{R_{16} + R_{OS}}{R_{OS}} R_S I_F \left(\frac{R_{PTC\_25} \cdot R_{VC}}{R_{PTC\_25} + R_{VC}} + \frac{R_F}{2} + R_S \right)}{\Delta V_{F\_25} - G_2 \frac{R_{16} + R_{OS}}{R_{OS}} \left(\frac{R_F}{2} + R_S \right) I_F} =$$

$$= \frac{0.0386 \frac{93.1\,k + 2574}{2574} 10\,m \cdot 4.568 \left(\frac{1\,k \cdot 1.5\,k}{1\,k + 1.5\,k} + \frac{10\,m}{2} + 10\,m \right)}{1.77 - 0.0386 \frac{93.1\,k + 2574}{2574} \left(\frac{10\,m}{2} + 10\,m \right) \cdot 4.568} = 23.5\ \Omega$$

The nearest standard value is chosen, R_{CD} = 23.7 Ω.

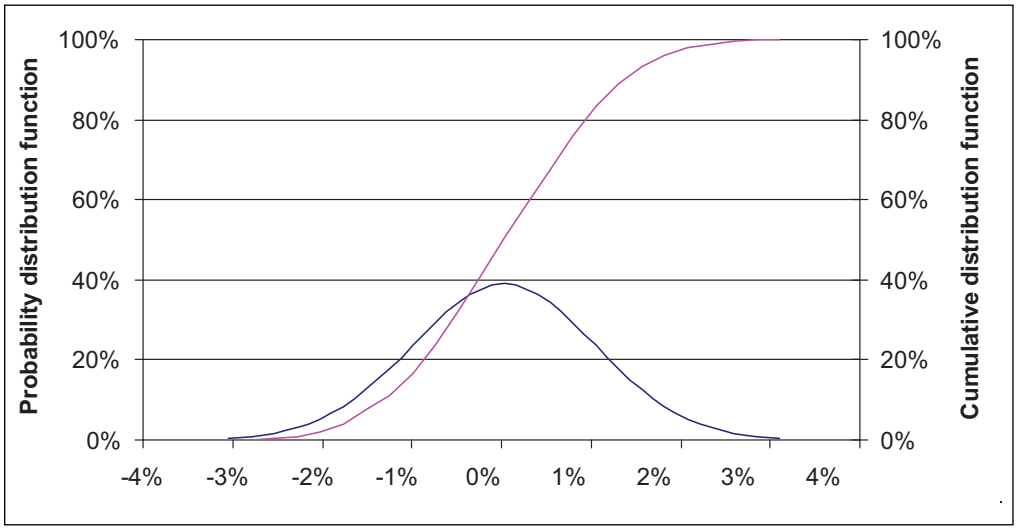
The design is now complete, the calculated resistors:
R_{SC} = 93.1 kΩ, R_{OS1} = 2610 Ω, R_{OS2} = 187 kΩ, R_{VC} = 1500 Ω and R_{CD} = 23.7 Ω
can be implemented in the two customer boards and regulation accuracy verified.

Conclusion

This procedure highlights the adaptive loop regulation concept and the design procedure to achieve good voltage regulation for a simple PRM/VTM combination.

Monte Carlo analysis shows that 1% regulation accuracy over line, load and temperature can be statistically achieved 82% (or greater) of the time. Figure 12 shows accuracy distribution for the design example previously illustrated.

Figure 12
Accuracy distribution over line, load and temperature for the design example



The same design concepts are directly applicable to arrays of V·I Chips if proper modeling applied. It is recommended to contact V·I Chip Application Engineering for any array involving 2 or more PRMs and 3 or more VTMs. The automated spreadsheet version of the procedure is available at www.vicorpower.com/dcaldesign.