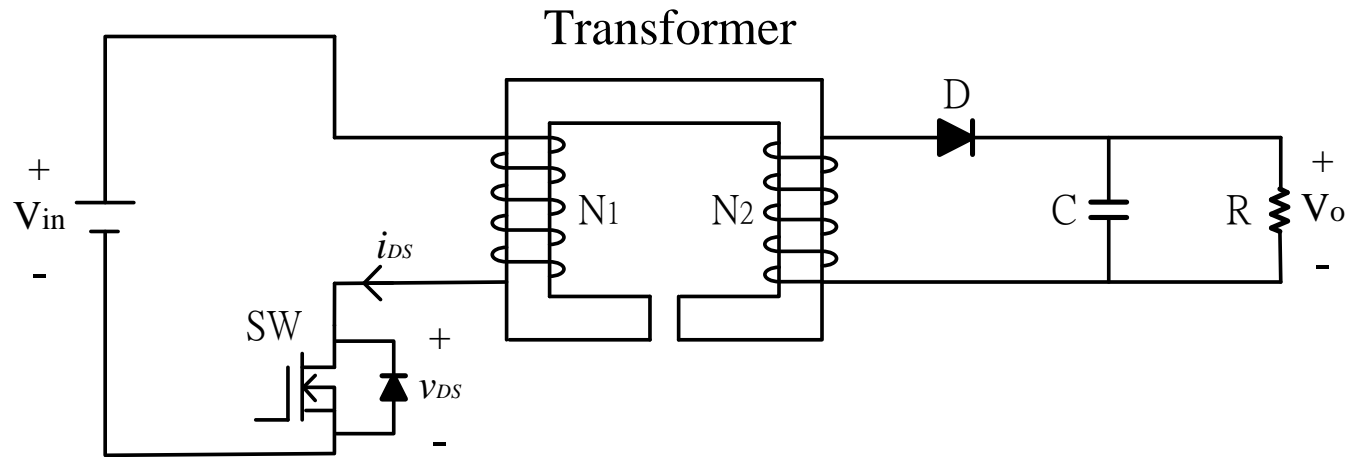


太陽能光伏電子系統理論與應用

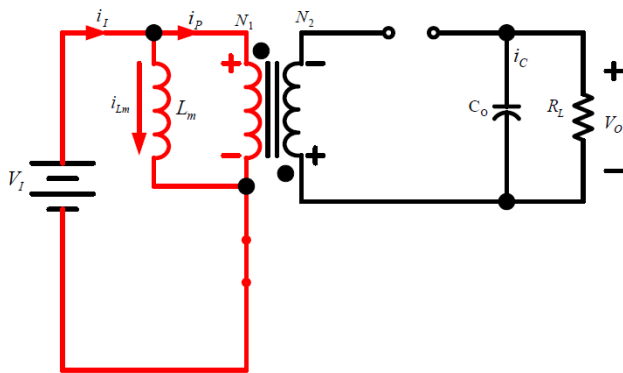
返馳式轉換器 Flyback Converter

實習課上課講義：2013/05/20

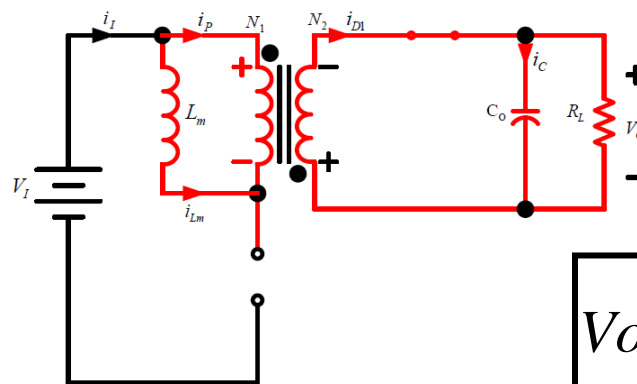
Flyback Converter Operation



Mode 1



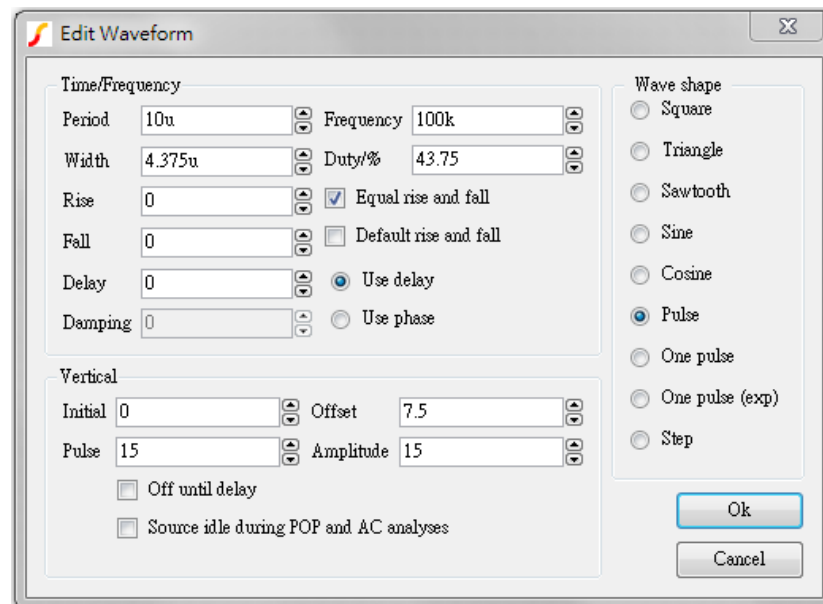
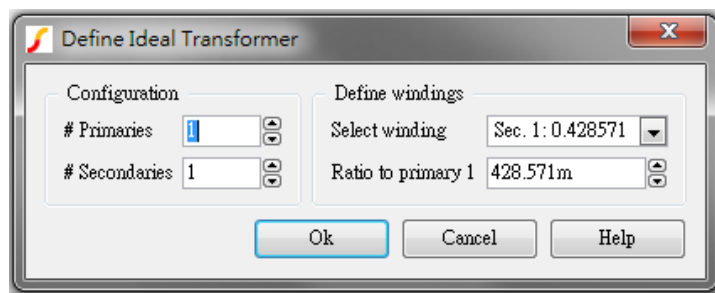
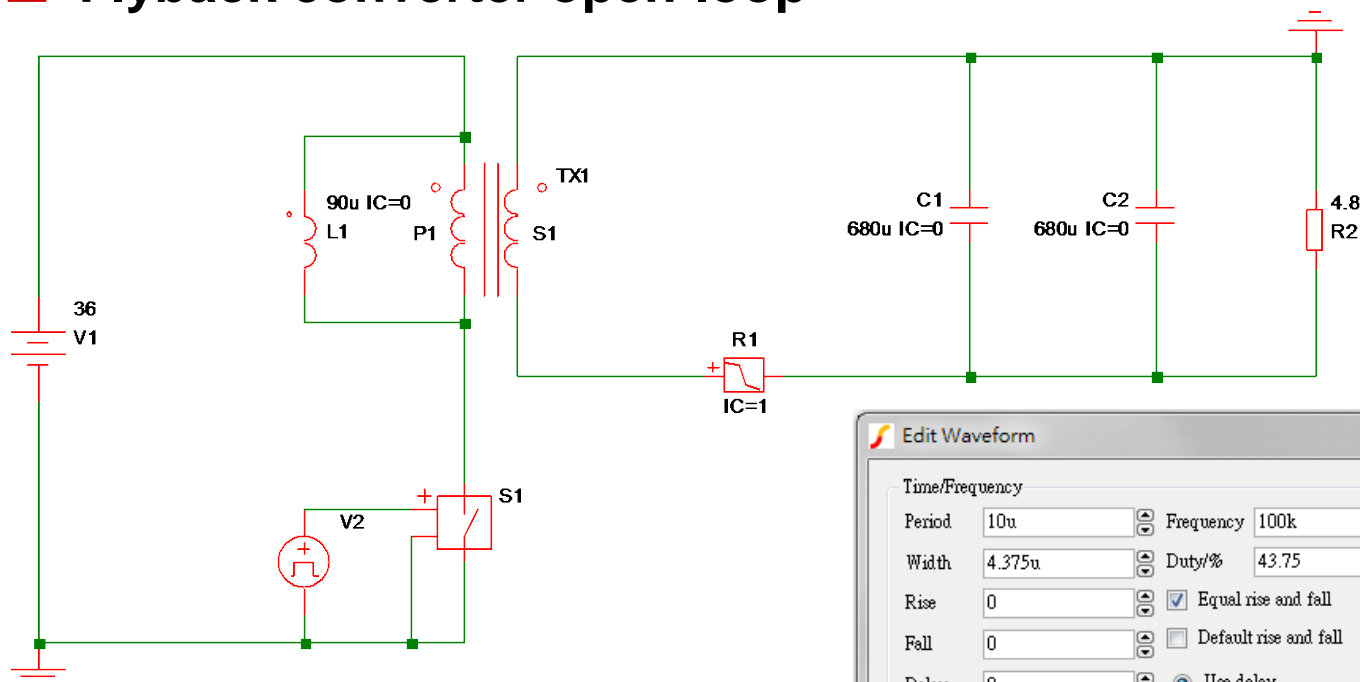
Mode 2



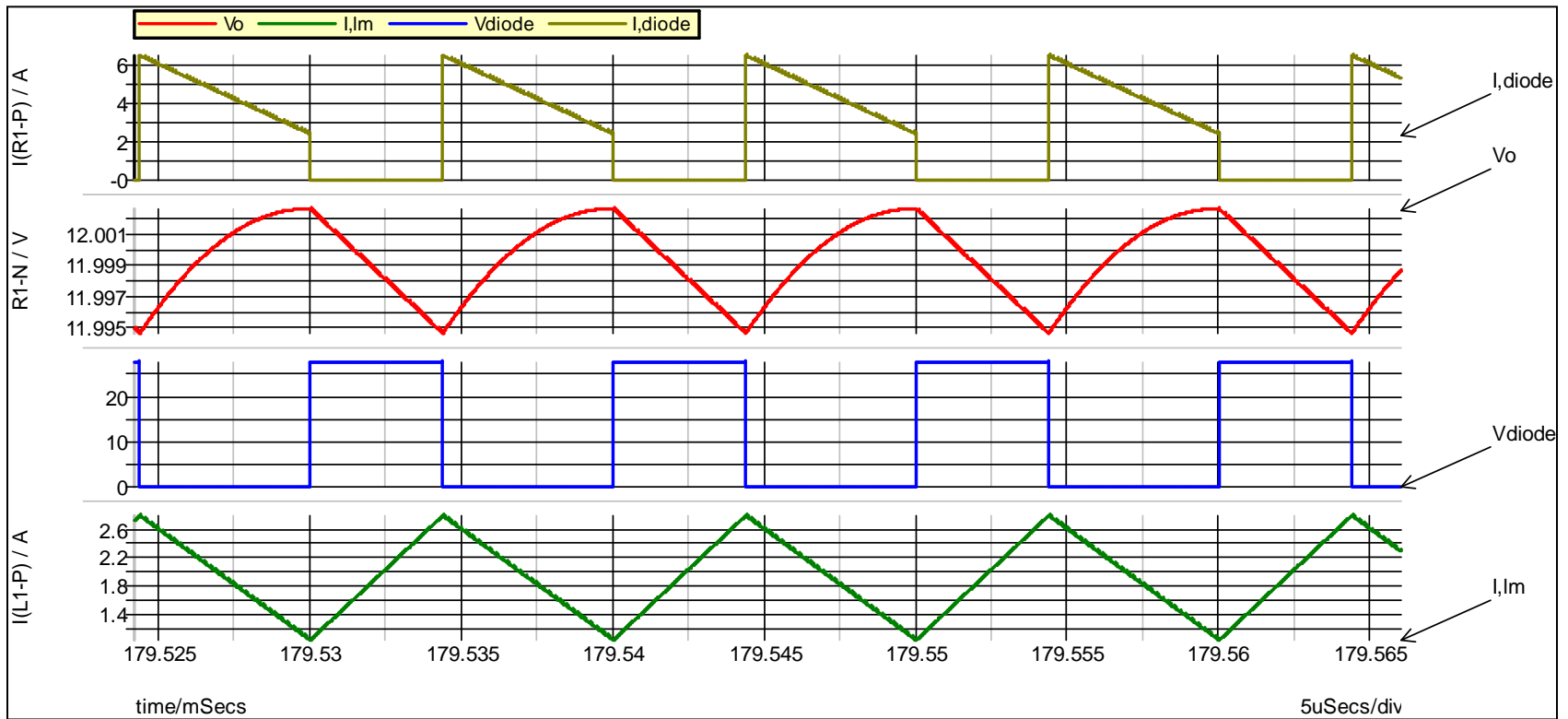
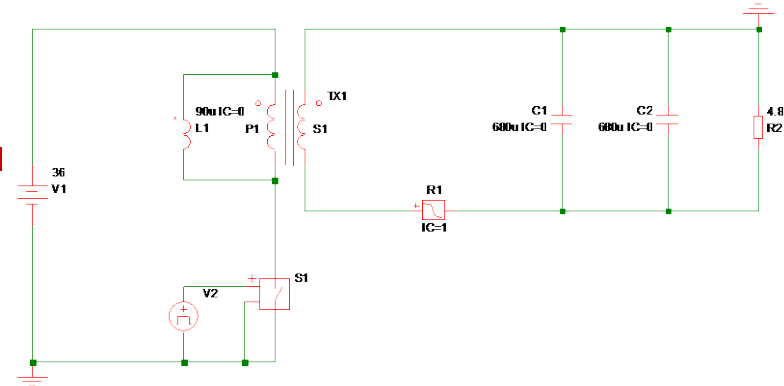
$$V_o = \frac{N_2}{N_1} \times \frac{D}{1-D} \times V_{in}$$

SIMPLIS Simulation

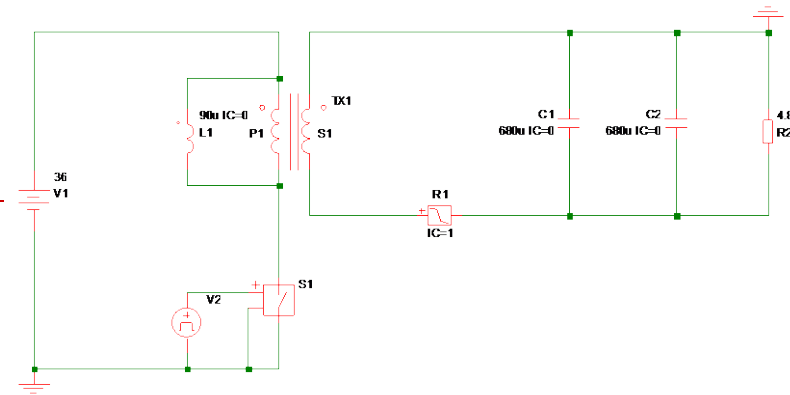
□ Flyback converter open-loop



Simulation Result



CCM VS DCM



□ Inductor & Capacitor Design

□ 參考講義”ch4_太陽光電能之直流直流隔離”，page13，
page20

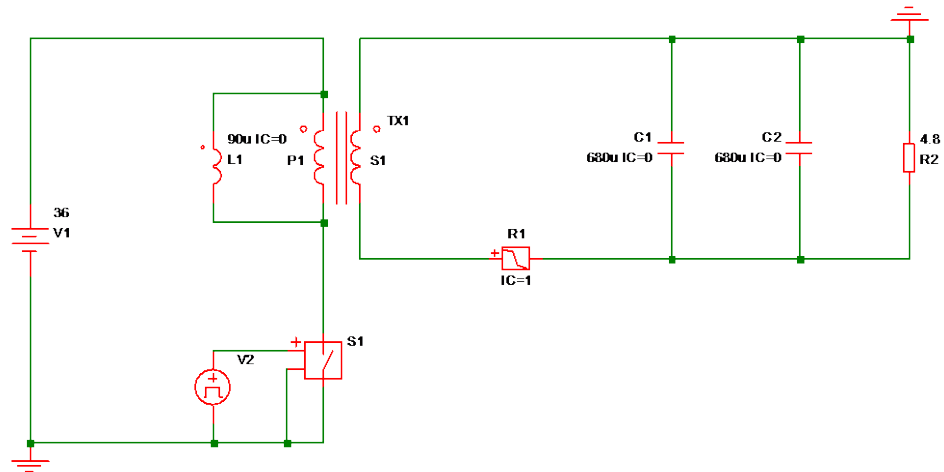
$$L_m > L_{mB} = \frac{V_o}{n^2 I_{OB}} (1-D) T_s \quad \text{for CCM condition} \quad (13)$$

$$\frac{\Delta V_o}{V_o} = \frac{D T_s}{R_L C_o} \times 100\% \quad (20)$$

Homework

1. 輸入電壓換成 48V, 56V, 找出正確的duty cycle, 使輸出穩定在12V
2. 承上，輸入電壓48V時，固定duty cycle, 將負載換成 6Ω , 12Ω , 觀察輸出電壓的變化，並加以說明討論
3. *BONUS: 重新設計電感電容值, 使電路在 $V_{in} = 56V$, $I_o = 0.2 A$ 的情形下可以操作在CCM，輸出電壓漣波 $< 1\% \cdot V_o$

作業打成PPT報告，含
作業、上課模擬檔
壓縮成一個檔案上傳



Voltage Mode VS Current Mode

Voltage mode

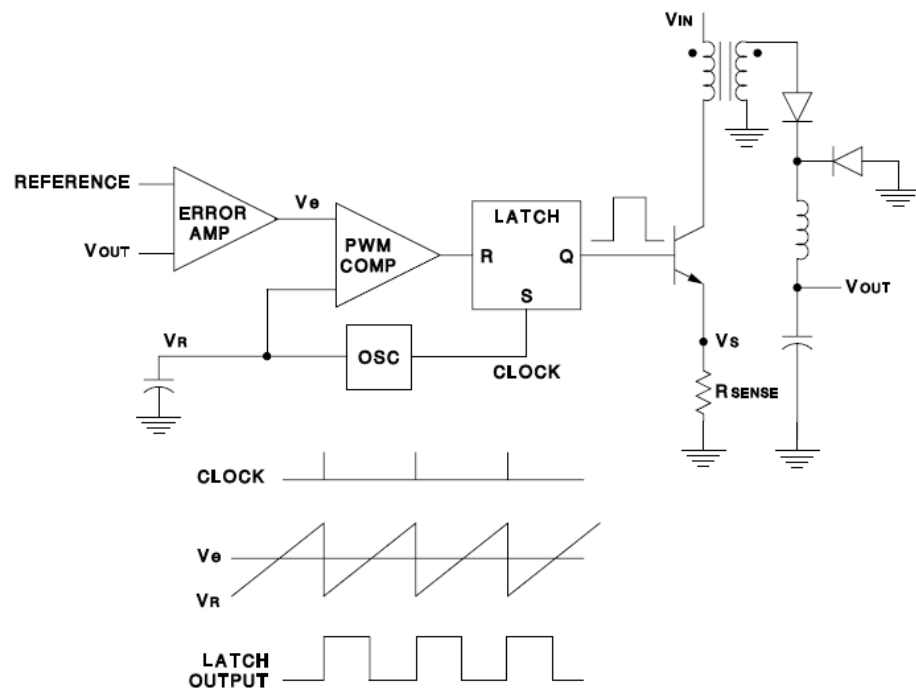


FIGURE 1. VOLTAGE MODE CONTROL

current mode

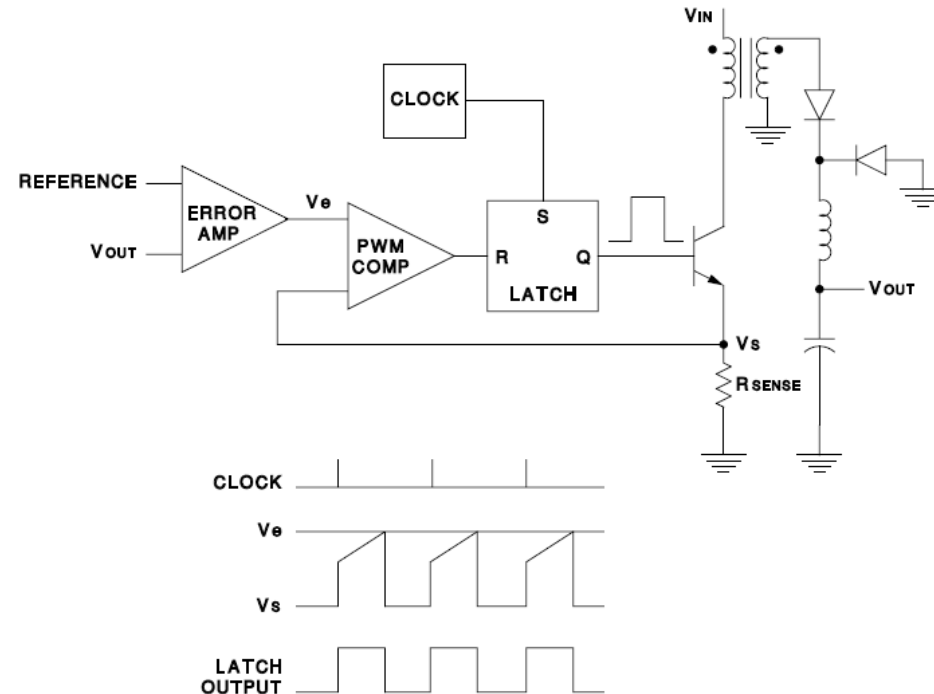
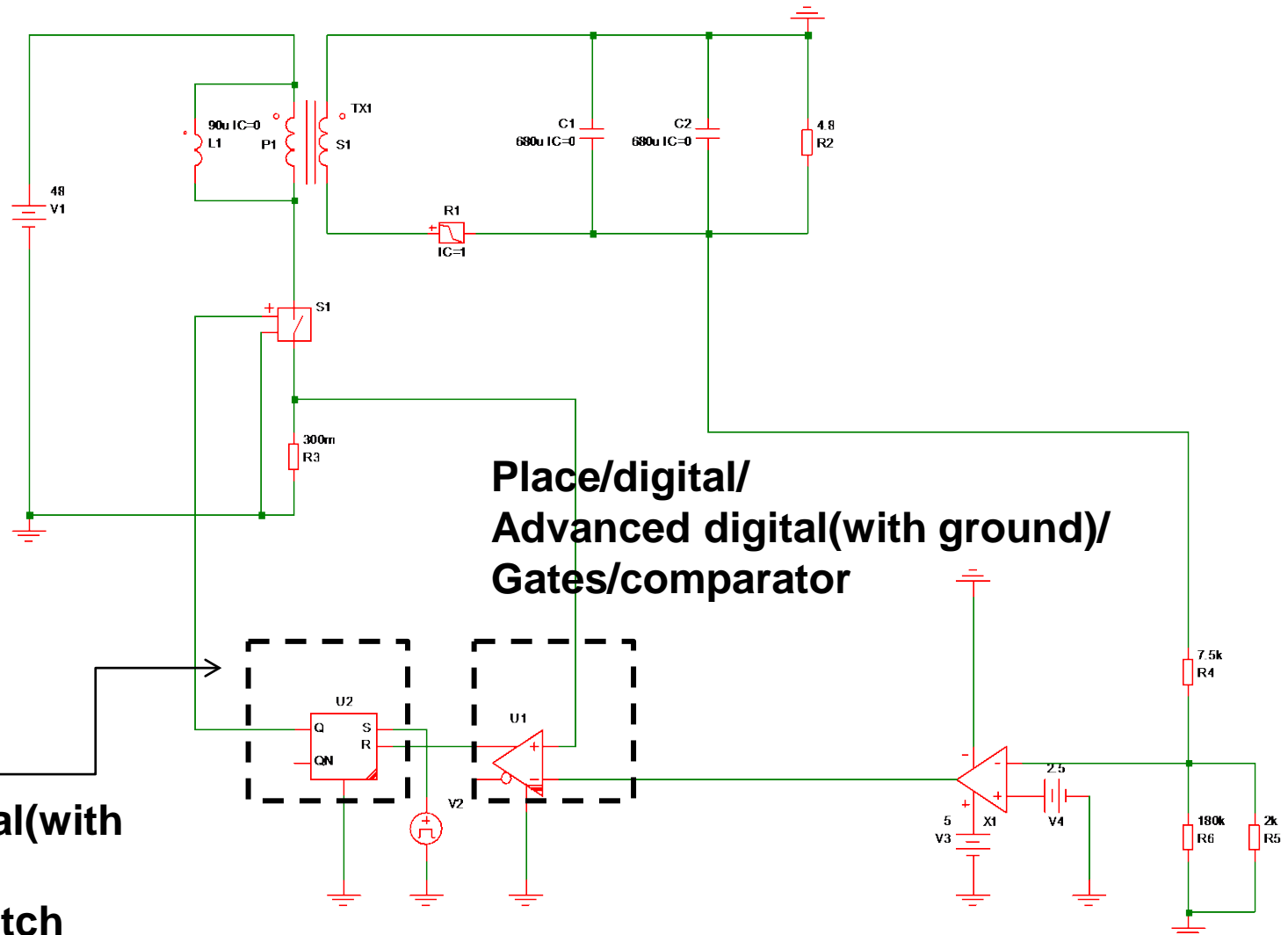


FIGURE 2. CURRENT MODE CONTROL

SIMPLIS Simulation

□ Flyback converter closed-loop

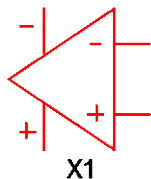


Place/digital/
Advanced digital(with
ground)/
Latches/ S/R Latch

Place/digital/
Advanced digital(with ground)/
Gates/comparator

Simulation Setting

□ OP amplifier

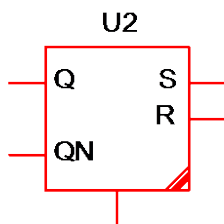


Edit Device Parameters

Model Level	2	Offset Voltage	0	Bias Current	100n
Offset Current	1n	Open-loop Gain in V/V	100k	Gain-bandwidth in Hz (Level 2)	1Meg
Pos. Slew Rate in V/s (Level 2)	1Meg	Neg. Slew Rate in V/s (Level 2)	1Meg	CMRR	100k
PSRR	100k	Input Resistance	1Meg	Max. Output Source Current (Level 2)	5m
Max. Output Sink Current (Level 2)	5m	Output Resistance	100	Output AC Resistance	50
Power Diss.	1m	Headroom Pos. (Level 2)	0	Headroom Neg. (Level 2)	0

☒ Use back-annotated info. for init. cond. if available

Ok Cancel Help



Edit Device Parameters

Input Resistance	10Meg	Output Resistance	10
Threshold	2.5	Hysteresis	1
Output Low Voltage	0	Output High Voltage	15
Delay	20p		

Initial Condition: 0 Set/Reset Level: 1

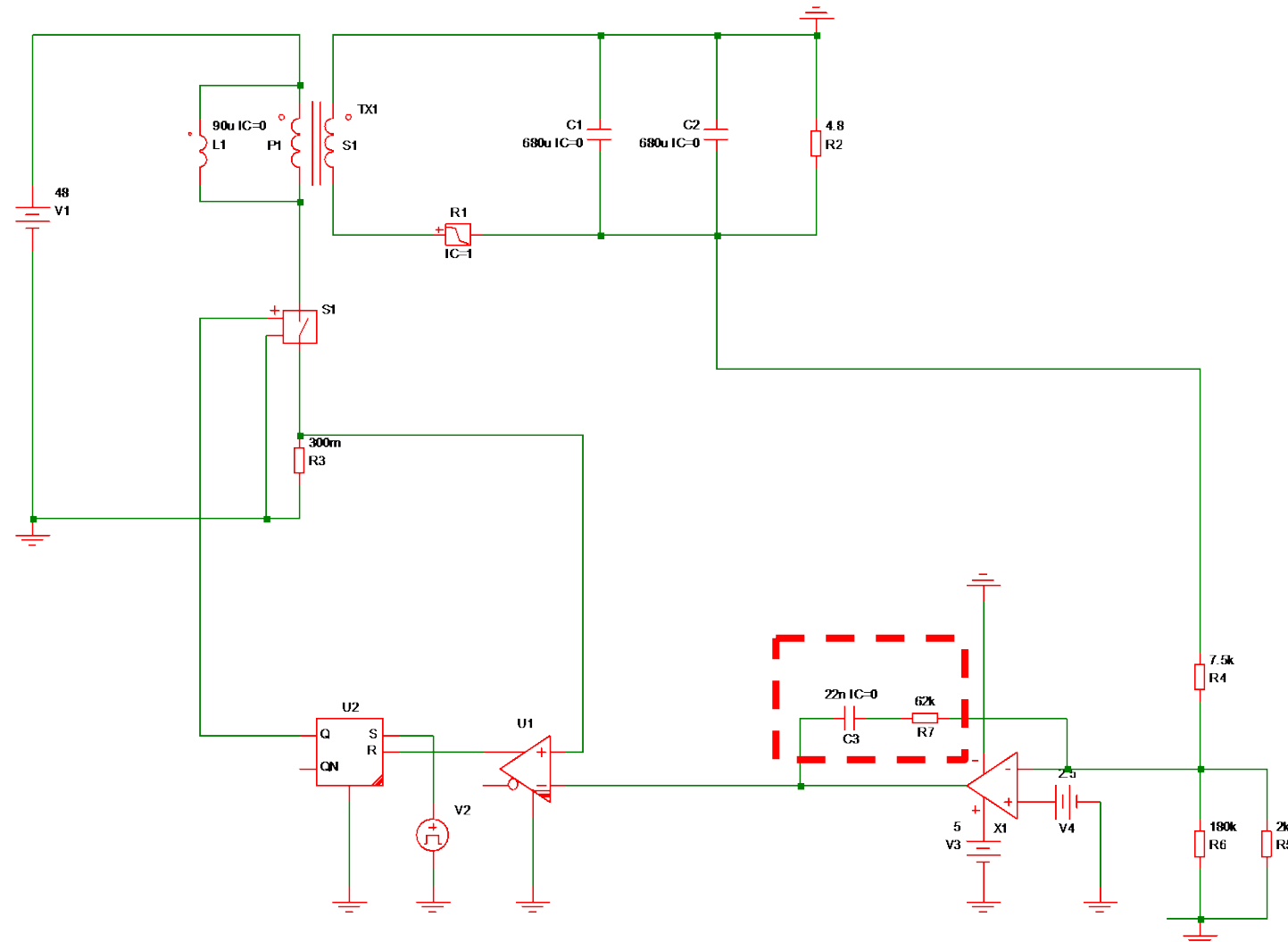
Ground Ref: 'Y' Enable: 'N'

S/R Dominance: NONE

Ok Cancel

SIMPLIS Simulation

□ Flyback converter closed-loop with compensator



[illegible]