Buck PFC Controller

Check for Samples: UCC29910

FEATURES

- **Buck Power Factor Correction for High Efficiency Across Line**
- **Low Off-Line Startup Current, With SmartStart Algorithm for Fast Startup With Soft-Start**
- **Compatible With Resistive or Pass Transistor Fed Startup from the AC Line**
- **Low Power SmartBurst Mode for Standby and Light-Load Conditions**
- **Current Sense Inputs for PFC control and Overload Protection**
- **Line Sense UVLO**
- **Sense and Drive Control for External Startup Depletion Mode FET**
- **Latching Fault Input Pin**

APPLICATIONS

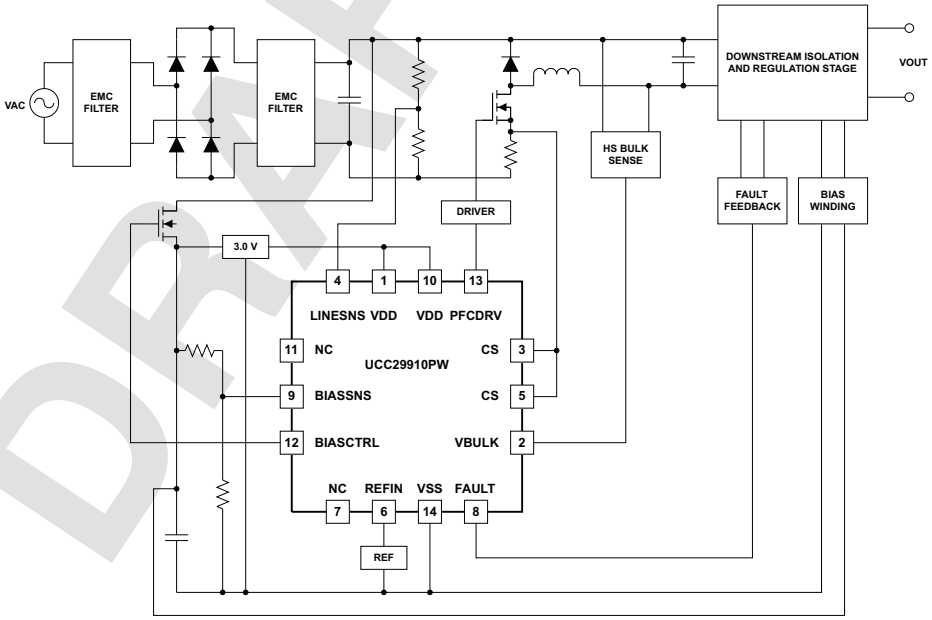
- **High Efficiency AC-DC Adapters**
- **Low Profile & High Density Adapters**

DESCRIPTION

The UCC29910 Buck Power Factor Correction (PFC) controller provides a relatively flat high-efficiency performance across universal line for designers requiring a high power factor (>0.9) and wishing to meet the requirements of IEC 61000-3-2. Based on a Buck Topology, inherent inrush current limiting eliminates the need for additional components. With a typical bus voltage of 84 V, the topology is ideally suited for use with low voltage stress downstream regulation/isolation power trains, such as half-bridge stages controlled by the UCC29900, (Texas Instruments Literature Number, SLUS923). This combination offers low common mode noise generation allowing reduced filtering and exceptionally high conversion efficiency.

The UCC29910 is a highly integrated controller designed for ease of use, which incorporates all the control features needed for high efficiency designs. It incorporates AC mains UVLO and controlled soft start for fast start-up and with “no spark” will not require the use of additional inrush protection circuitry. A particular design goal of the part is enhanced light-load efficiency, achieved through advanced management algorithms for best-in-class no-load and light-load performance.

SIMPLIFIED APPLICATION DIAGRAM



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ORDERING INFORMATION

PART NUMBER	PACKAGE	PACKING
UCC29910PW	Plastic, 14-Pin TSSOP (PW)	90-Pc. Tube
UCC29910PWR	Plastic, 14-Pin TSSOP (PW)	2000-Pc. Tape and Reel

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted) (1)(2)(3)

		VALUE	UNIT
V_{DD}	Supply Voltage	4.1	V
		-0.3	
	Voltage: All pins	−0.3 to VDD + 0.3	
	Diode Current: All pins	+/- 2	mA
T_A	Operating free air temperature, (4)	−40 to 105	°C
T_J	Operational junction temperature, (4)		
T_{STG}	Storage temperature (4)	−40 to 105	
	Lead temperature (10 seconds)	260	

(1) These are stress limits. Stress beyond these limits may cause permanent damage to the device. Functional operation of the device at these or any conditions beyond those indicated under RECOMMENDED OPERATING CONDITIONS is not implied. Exposure to absolute maximum rated conditions for extended periods of time may affect device reliability.
(2) All voltages are with respect to GND.
(3) All currents are positive into the terminal, negative out of the terminal.
(4) Higher temperature may be applied during board soldering process according to the current JEDEC J-STD-020 specification with peak reflow temperatures not higher than classified on the device label on the shipping boxes or reels.

RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
T_A	Operating free air temperature	−40		105	°C
	VDD Input Voltage	3.0		3.6	V
	All Inputs	0		VDD	

ELECTRICAL CHARACTERISTICS

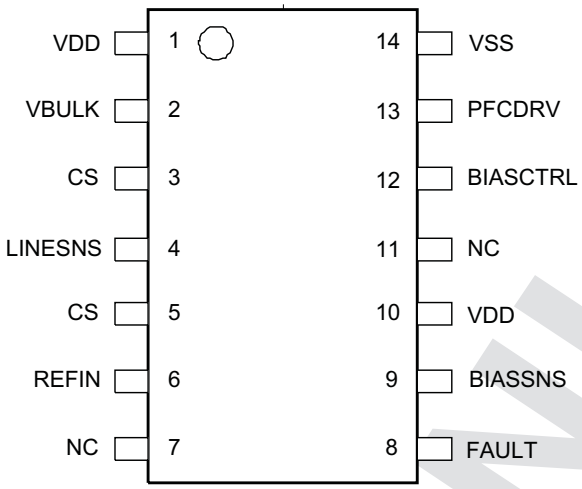
over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Voltage Biasing						
I_{VDD}	VDD Current			5		mA
	BIASCTRL	BIASCTRL hi level	Iow = -1.5 mA	VDD-0.25 V		VDD
		BIASCTRL low level	Iow = 1.5 mA	0	0.25	
Voltage Monitoring						
V_{STE}	Start-up phase endpoint	VBULK		1.074		V
V_{NM}	VBULK nominal			1.049		
V_{OV}	VBULK over voltage			1.124		
V_{LL}	Light load, lower threshold			1.074		
V_{LU}	Light load, upper threshold			1.087		
V_{IM}	Full scale current range(1)	CS pin voltage		0.35		
V_{BH}	Start-up voltage	Measured at LINESNS pin		264		mV_{RMS}
V_{BL}	Brownout voltage			249		
V_{RS}	Line reset voltage(2)			217		
V_{LM}	Max line voltage			932		
$V_{B(max)}$	During start-up	Measured at BIASSNS pin		913		mV
$V_{B(min)}$	During start-up and LL mode			457		
V_{BLO}	During LL mode			495		
Light Load Mode						
t_B	LLM burst			1.2		ms
t_{BI}	LLM burst interval		5.0			
FAULT Input						
	FAULT internal pull-up		20	35	50	kΩ
	FAULT falling threshold		0.8		1.85	V
	FAULT rising threshold		1.45		2.53	
	Hysteresis		0.3		1	
	Response time			100		µs
Start Up						
T_{ST}	Start-up timeout			600		ms
Power On Reset (POR)						
V_{POR}	Falling threshold	Measure at VDD falling			1.71	V
	Hysteresis		70	130	210	mV
	POR delay	Duration of VDD < V_{POR}		2		µs
Oscillator Output						
	Switching Frequency	Normal Mode		100		kHz
	D_{MAX}	Measured at PFCDRV output			90%	
	PFCDRV hi level	Iow = -1.5 mA	VDD-0.25V		VDD	V
	PFCDRV low level	Iow = 1.5 mA	0		0.25	
t_r	PFCDRV rise time			15		ns
t_f	PFCDRV fall time			22		
Reference						
V_{REF} (3)	REFIN		1.485	1.5	1.515	V

(1) The CS signal must be scaled so that the maximum allowed inductor current produces 350mV at this pin
(2) Line voltage must persist below V_{RS} for more than 120 ms. Reset follows 10 seconds later.
(3) Variations in VREF from the nominal 1.5 V affect all other measured parameters proportionally.

DEVICE INFORMATION

UCC29910 14- Pin TSSOP (PW)



TERMINAL FUNCTIONS

TERMINAL		I/O	DESCRIPTION
NAME	NO.		
VDD	1	-	Provides power to the device; should be decoupled with ceramic capacitor 1uF, connected directly across pins 1-14.
VBULK	2	I	Voltage sensing of the bulk capacitor.
CS	3	I	Current sense input for PFC stage.
LINESNS	4	I	Rectified AC line sense input.
CS	5	I	Current sense input for PFC stage.
REFIN	6	I	Reference input for internal comparators/error amp.
NC	7	-	NC This pin is not used, and should be left open.
FAULT	8	I	Latched Fault input from second stage for over-voltage or over-load protection.
BIASSNS	9	I	Sense input for the bias rail for startup control.
VDD	10	I	This pin must always be connected to pin 1.
NC	11	-	No connection should be made to this pin.
BIASCTRL	12	O	Control output for the external startup fet for startup control.
PFCDRV	13	O	Drive for PFC FET.
VSS	14	-	Ground for internal circuitry.

Detailed Pin Description

Pin 1 – VDD: This pin supplies power to the device. A minimum supply voltage level of 3.0 V and maximum of 3.6 V is recommended.

Pin 2 – VBULK: The bulk capacitor voltage level is sensed on this pin. A level of 84 V nominal on the bulk capacitor is normally indicated and this corresponds to a level of 1.05 V on the pin. The Thevenin equivalent feed impedance is optimally below 20 kΩ, with appropriate capacitance provided for noise containment. Note that the V_{BULK} scaling and LINESNS scaling must maintain a ratio of close to 4:1 to ensure optimum operation of the SmartStart algorithm.

Pin 3 – CS: This pin senses the current in the PFC stage. Note that two current sense pins are used, pins 3 and 5. Both pins must be connected together to the CS signal. The CS pin is intended to sense low side PFC fet current directly. A 50-mΩ current sense resistor value is typically optimal for powers of 90 W, with appropriate scaling for higher power levels. The recommended feed impedance level is approximately 10 kΩ, and a capacitor of 10 nF is also recommended to act as a filter on the input current and to minimise noise pickup. A smaller value capacitor may result in possible current loop instability. A larger cap value may result in poor Power Factor (PF) due to excessive current signal phase shift.

Pin 4 – LINESNS: This pin senses the rectified line voltage. The internal reference for this pin is internally scaled to ¼ of the V_{BULK} reference. Note that the LINESNS scaling and V_{BULK} scaling must maintain a ratio of close to 1:4 to ensure optimum operation of the SmartStart algorithm. A peak of high line voltage (typically 373 V for 264 V_{AC} input) should be scaled to correspond to 1.158 V. A pin feed impedance of less than 20 kΩ is recommended, along with a filter capacitor of at least 10 nF for noise filtering.

Pin 5 – CS: See pin 3 description above. This pin senses the current in the PFC stage, pins 3 and 5 must be connected together.

Pin 6 – REFIN: This pin must be connected to an external accurate 1.500-V reference source, e.g. using a suitable shunt regulator with voltage setting resistors such as TLVH431A.

Pin 7 – NC: This pin is not used, and should be left open.

Pin 8 – FAULT: This pin when pulled low causes a latch-off condition which is reset only when the line voltage is removed. Typically it is fed from an output overvoltage signal as received via an opto-coupler, or an overload fault signal from the down-stream isolation/regulation stage. An internal weak pullup resistor (nominally 35 kΩ) is present and an external resistor – typically 4.7 kΩ – can be used in more noise-sensitive layout environments.

Pin 9 – BIASSNS: This pin is used to sense the PFC stage bias rail (normally in the 8-V to 12-V range to drive the PFC power MOSFET) during start-up to allow control of the external start-up fet.

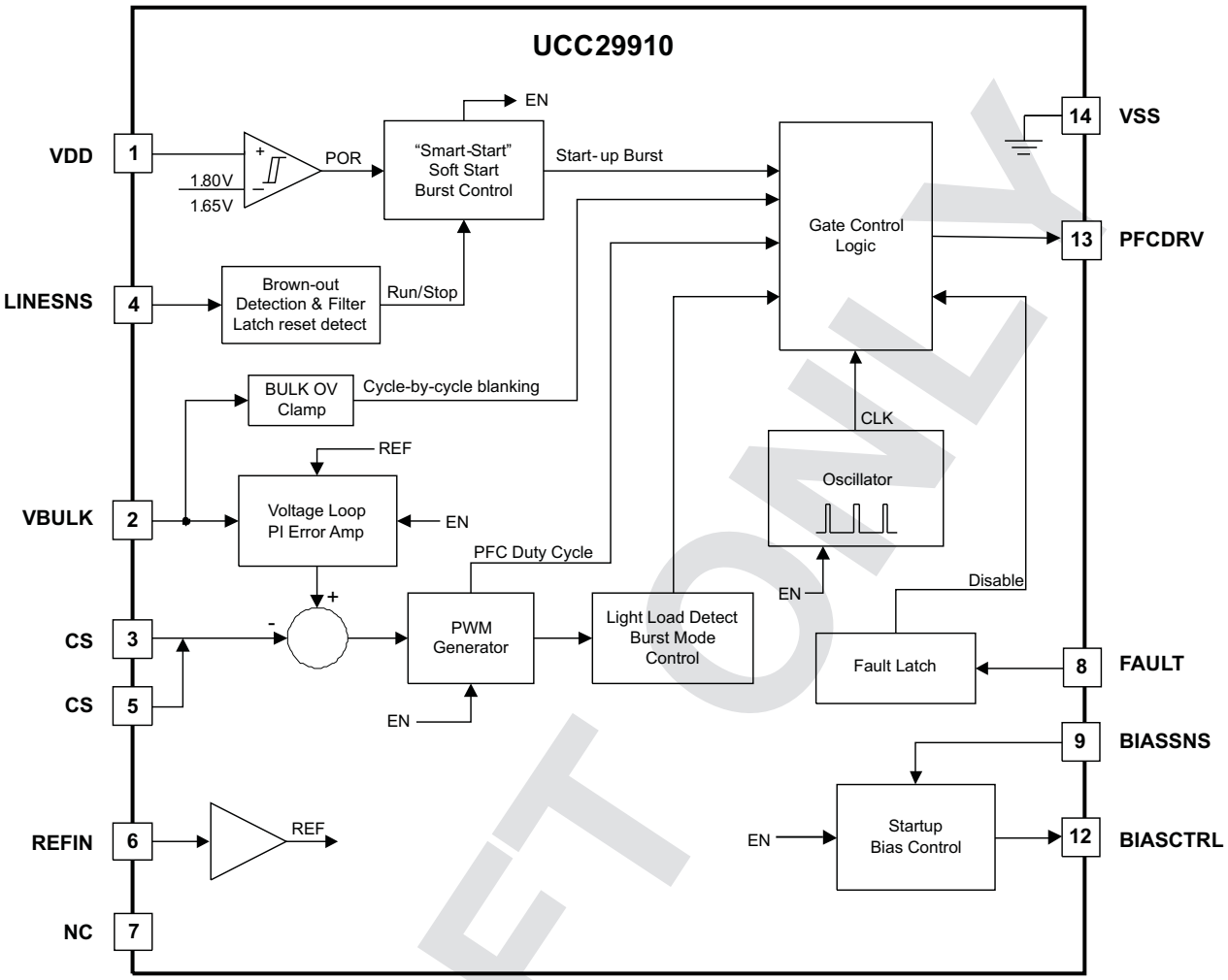
Pin 10 – VDD: This pin must be pulled high in normal operation, typically with 47 kΩ to VDD.

Pin 11 – NC: This pin is for internal use only, and must be normally left open.

Pin 13 – PFCDRV: This pin is used to drive the low-side PFC FET indirectly. This pin should be connected to a level-shifting gate driver to provide the required drive signal amplitude for typical high voltage power FET's. For this drive signal, D_{MAX} is limited to 90% duty cycle.

Pin 14 – GND: This pin is the common ground connection for the device.

UCC29910 Functional Block Diagram



APPLICATION INFORMATION

This controller is designed to control Buck PFC stages and is particularly suited to AC/DC applications in the power range from 65 W to 130 W. A fully characterised reference design using the UCC29910 PFC controller and the UCC29900 Integral Cycle Controller is available on request. The design is for a 90-W PSU intended for laptop adapter applications. It comprises a Buck PFC front end using the UCC29910 to convert line power to a nominal 84 V_{DC}. A UCC29900 controls the conversion of this bulk voltage to a nominal 19.25-V output using a half bridge output power stage. The paragraphs following give some details on how the UCC29910 is used. Additional guidelines for both the UCC29910 and UCC29900 are available on request.

Buck PFC Power Stage

The PFC stage converts the incoming rectified line voltage to a DC voltage on the output capacitors, power transfer happening during the times when the line voltage is greater than the output voltage. The resulting conduction angle is a function of both the incoming line and output voltages. The output voltage is optimally set to 84 V_{DC} which is low enough to allow conduction angles sufficient to achieve a PF (Power Factor) of at least 0.9 over an input voltage range from 90 V_{AC} to 264 V_{AC}. A high efficiency second stage can then down-convert to a nominal output of 19.25 V using a transformer with a simple 4:1 turns ratio, or to any other desired output voltage. The basic Buck PFC power stage is shown in Figure 1. The incoming AC line is fed through a rectifier and filter stages, not shown here. The resulting unipolar voltage (V_{HV}) is then fed into the power stage. The MOSFET is switched at a constant 100 kHz and the freewheeling diode function is provided by D1. The output voltage is developed across the two large capacitors, C2 and C21.

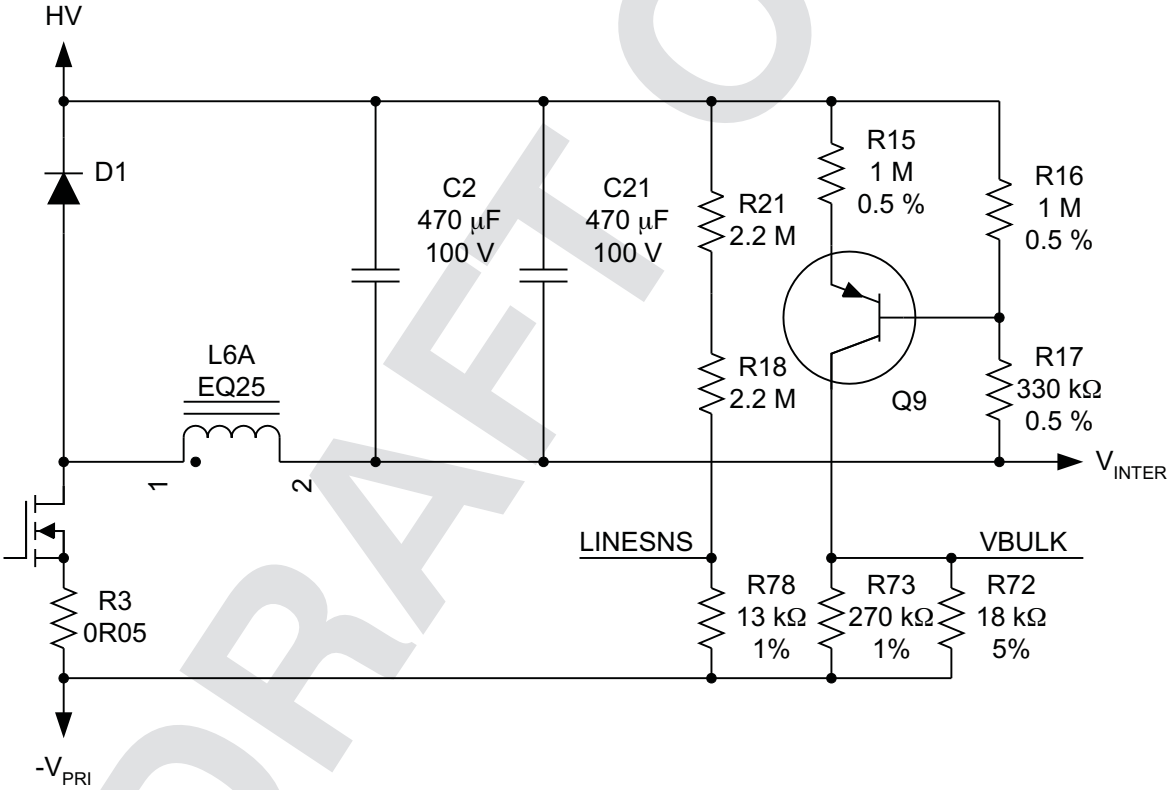


Figure 1. Buck Power Stage (simplified)

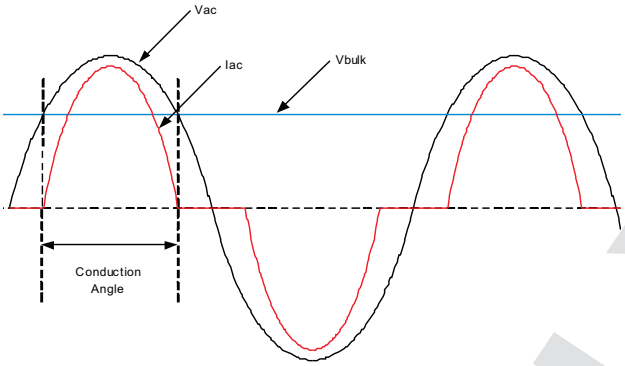


Figure 2. Illustrative Line Current and Voltage

The Buck converter operates off a rectified sinusoid, there are periodic dead times when the input voltage is lower than the output. During these times no power can be transferred to the output and the input current is nominally zero. Figure 1 shows the line current, I_{AC}, falling to zero when V_{AC} is less than V_{BULK}. The associated conduction angle increases as the RMS line voltage increases and the current waveform changes from low line to high line. The input current is therefore 'skewed' a little towards the beginning of the conduction cycle because V_{BULK} is at its lowest value at this time so conduction starts at a lower voltage than it finishes. This effect may be seen in Figure 3 and Figure 4. These waveforms are taken from a 90-W buck PFC reference design, both meet the harmonics requirements set out in EN61000-3-2 and their PF is greater than 90%.

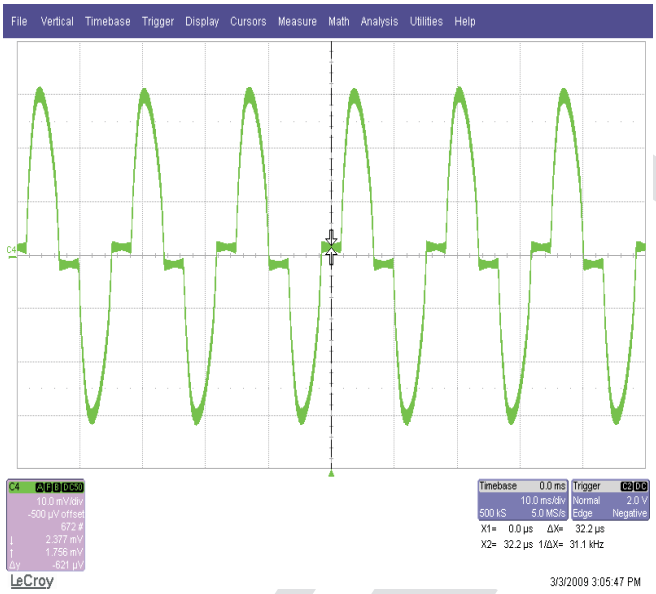


Figure 3. Input Current,
(115 V, 60 Hz, full load, 0.5 A/div)

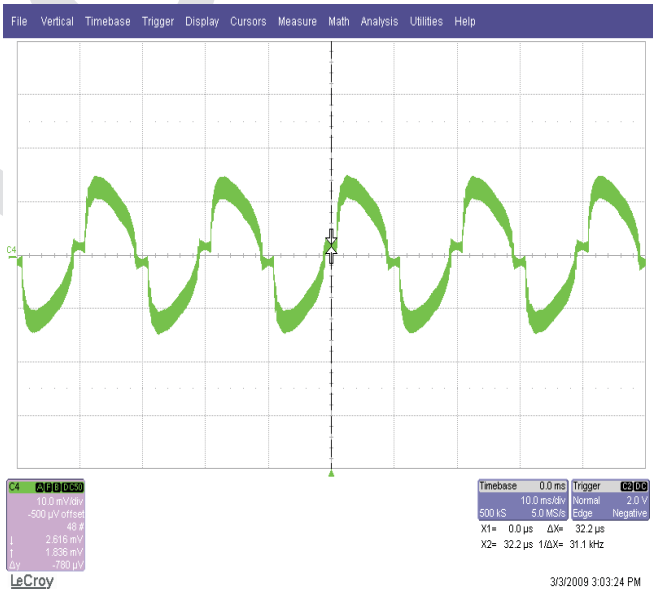


Figure 4. Input Current,
(230 V, 50 Hz, full load, 0.5 A/div)

PFC Inductor

The PFC choke is typically designed for an inductance value that ensures DCM operation at high line (i.e. >160Vac), right up to full peak load. With an appropriate value of inductance, operation at low line should then result in CCM operation over most of the conduction angle at full load. The inductance required is given by:

$$L_{PFC} = \frac{1}{2 \times f_{SW} \times I_{IN(pk)}} \left(V_{IN(pk)} - V_{BULK}\right) \left(\frac{V_{BULK}}{V_{IN(pk)}}\right)^2 \quad (1)$$

where:

$$I_{IN(pk)} = \frac{P_{IN(avg)} \times \pi}{2 \times V_{IN(pk)}} \times \frac{\left(1 - \sin\theta_{START}\right)}{\int_{\pi\theta_{START}}^{\pi/2} \left[\sin^2\left(\theta - \sin\theta \times \sin\theta_{START}\right)\right] d\theta} \quad (2)$$

And π is the stage conversion efficiency, θ_{START} is the phase angle at which conduction starts, ie where the instantaneous line voltage equals the bulk voltage. For a 100-W converter with an 84-V_{BULK} DC output we evaluate the equation at 160 V as follows.

$$L_{PFC} = \frac{1}{2 \times 100E^3 \times 1.033} \left(\sqrt{2} \times 160 - 84\right) \left(\frac{84}{\sqrt{2} \times 160}\right)^2 = 94.9\,\mu H \quad (3)$$

Compared to the Boost PFC, much smaller values of PFC inductance can typically be used in the Buck, because the voltage differential that needs to be supported across the choke is lower. Practical inductance values that have been used in various designs have ranged from ~150 µH at 50 W, to ~80 µH to 100 µH at 90 W to 150 W, down to ~50 µH to 60 µH for 300 W to 400 W power levels.

Bulk Capacitor Choice

The value of bulk capacitance required is dictated by requirements on the allowable ripple voltage and hold-up time. Where hold-up time is not the main factor, then the capacitors should be sized for approximately 12% pk-to-pk ripple as follows:

$$C_{BUS} = \frac{P_{LOAD} \times \theta_{cond\_\%}}{V_{BUS} \times \Delta V_{BUS(\%)} \times 2 \times f_{AC}} \quad (4)$$

For a typical 90-W adapter using Buck PFC, the required bus capacitance for ±6% maximum ripple at 90 V_{AC}/50 Hz (12% total ripple) and at 84^2 V_{DC} bus, assuming 96.5% efficiency of the second stage, would be:

$$C_{BUS} = \frac{\frac{90}{0.965} \times 0.57}{84^2 \times 0.12 \times 2 \times 50} = 628\,\mu F \quad (5)$$

where:

- **P_{LOAD}:** load power drawn (usually by the second regulation/isolation stage)
- **C_{BUS}:** bus capacitance
- **$\theta_{COND\_\%}$:** conduction angle at AC line of interest (as decimal percentage of total cycle, e.g. 50% conduction angle expressed as 0.5)
- **f_{AC}:** AC line frequency

The capacitance required to achieve a specific hold up time may be calculated as follows:

$$C_{BUS} = \frac{T_{HOLDUP} \times 2 \times P_{LOAD}}{\left(V_{BUS(min)}^{\ 2} - V_{BUS(min\_reg)}^{\ 2}\right)} \quad (6)$$

For example, in order to achieve 3-ms holdup, with nominal bus voltage of 84 V_{DC}, ±5% maximum bus ripple, and 70 V_{DC} minimum bus regulation level for the second stage, the required bus capacitance would be calculated as follows for a 90-W load, assuming 96.5% second stage efficiency:

$$C_{BUS} = \frac{0.003 \times 2 \times \frac{90}{0.965}}{\left((84 \times 0.95)^2 - 70^2\right)} = 381\mu F \quad (7)$$

Startup with External FET

Conventional start-up schemes utilising either resistive or enhancement mode MOSFET feeds incur line dependent static power losses. To avoid these power losses and to obtain an optimum turn-on time an external depletion mode FET may be used Figure 5 and Figure 6. The HV node is connected to the rectified incoming line. Q12 is a depletion mode FET which will start charging C45 as soon as VHV has exceeded its threshold voltage which is nominally 2 V. Initially U1 is inactive and Q6 is turned off. The V_{DD_3V} rail will begin to increase as U10 starts to conduct. The POR (Power On Reset) sequence of U1 will begin once this rail gets to about 1.7 V and will execute while the V_{DD_3V} rail is being established. The BIASCTRL pin will go high when BIASSNS reaches the $V_{B(max)}$ level. With the given values for R84 and R85 and assuming the REFIN pin is at 1.5 V this occurs when V_{CCA} reaches 12 V.

At this time, U1 begins to pulse the PFCDRV pin, which starts the process of charging the bulk capacitors at the output of the Buck PFC power stage. The current required to do this is drawn from C45, which starts to discharge. If the voltage at the BIASSNS pin falls below $V_{B(min)}$ then PFC switching is disabled and Q12 is turned on to re-charge C45. With the given component values the $V_{B(min)}$ level corresponds to 6 V on C45. The user can change this level if they wish, depending on the characteristics of any alternative components used.

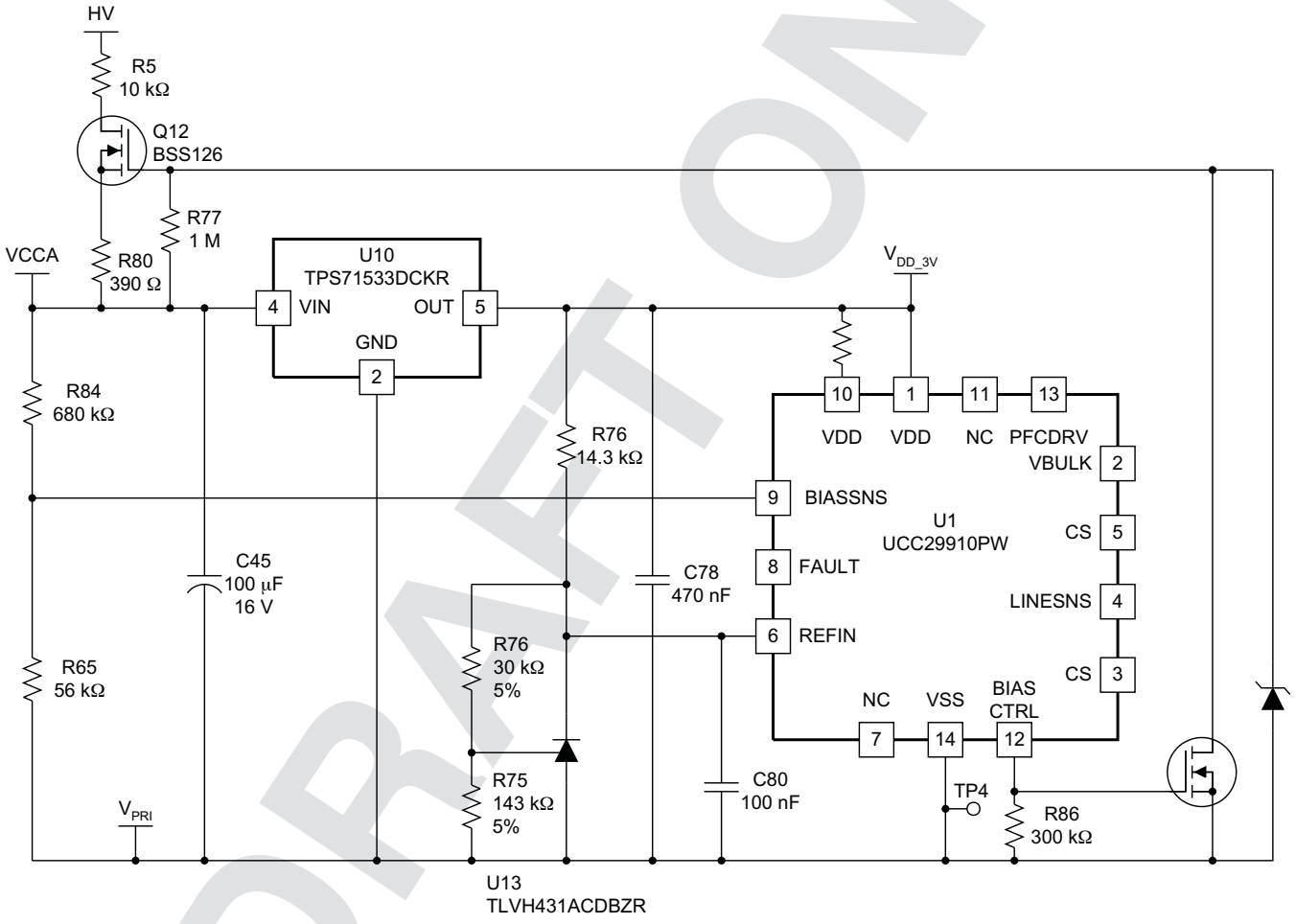


Figure 5. Simplified Schematic

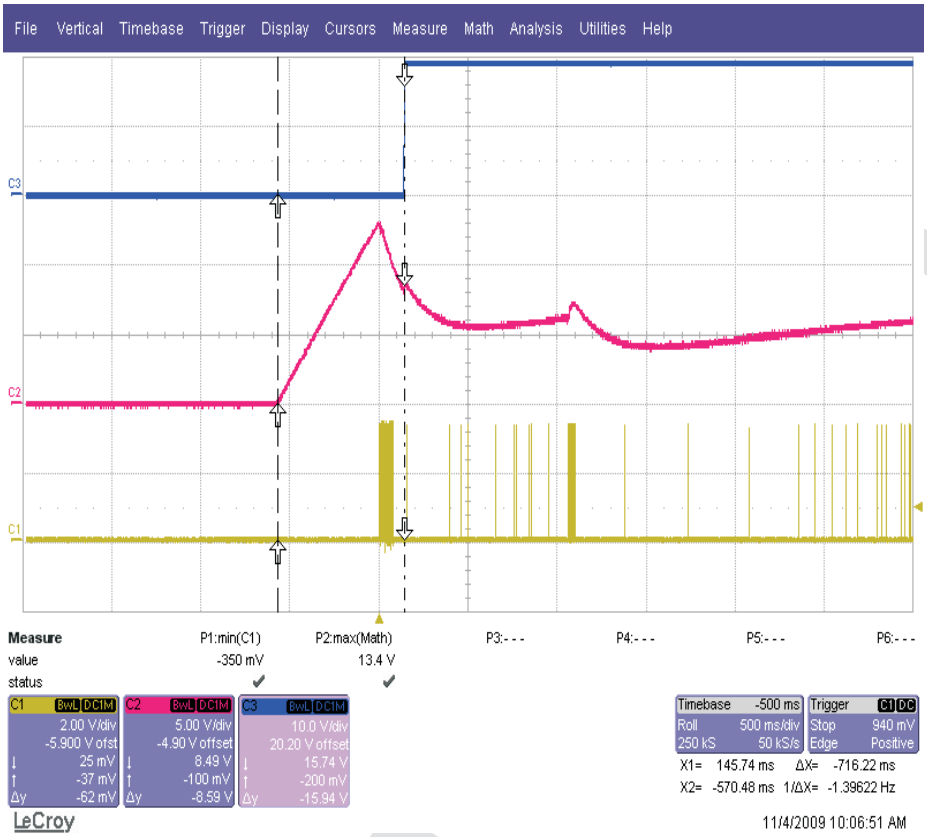


Figure 6. Start-Up Sequence Waveforms (Ch1 (Y), PFCDRV; Ch2 (R), V_{CCA}; Ch3 (B), DUT V_O)

V_{BULK} Ramp-Up

Once V_{CCA} has reached 12 V and Q12 has been turned off, the PFCDRV output of U1 becomes active and begins driving the main power MOSFET. The aim is to increase V_{BULK}, the voltage across C2 and C21, as rapidly as possible and this is done by transferring the maximum amount of energy possible during each pulse set. The UCC29910 requires that the inductor be designed to have a Volt-sec product withstand rating of 600 Vμs. In fact any inductor suitable for application in a Buck PFC stage will already meet this requirement in order to carry the full load currents involved without saturating, therefore the Volt-sec rating will not result in any additional constraints on the choke design. It is more convenient to think in terms of applied Volt-sec product rather than the peak inductor current.

The UCC29910 generates a series of pulses to the switching MOSFET which apply a constant Volt-sec product to the inductor during the on and off intervals. This ensures that the inductor current is ramped up as high as possible while the MOSFET is on and then decays to zero during the off time. In fact,T_{OFF} is extended to 110% of nominal which provides margin to ensure the inductor current ramps back to zero. The UCC29910 measures the instantaneous line voltage, (VHV in Figure 1) and the output voltage (HV-Vinter in Figure 1). The voltage applied to the inductor when Q1 is on is then found by subtracting these two values. It then calculates an appropriate T_{ON} corresponding to a 600 V x μs product. Toff is calculated in a similar fashion except that the inductor voltage during the off time is the voltage on the capacitors C2 and C21 (V_{BULK}) plus the forward voltage drop in D1 which is assumed to be 0.6 V. Inductor current is controlled on a cycle-by-cycle basis by constraining the T_{ON} and T_{OFF} values so that the inductor Volt-sec product is never exceeded. The initial T_{OFF} pulses are typically 1.1-ms long because the bulk capacitor voltage is still very low. As V_{BULK} is established, the current ramp-down rate will increase and the required T_{OFF} will reduce very rapidly and therefore the pulse sets can be moved much closer together as V_{BULK} rises. In addition, as V_{BULK} rises, the voltage across the PFC choke during T_{ON} will drop, so the on-time is adjusted to maintain a constant PFC choke volt-secs product.

During ramp-up the UCC29910 monitors V_{BIAS} and if the voltage at the BIASSNS pin falls below $V_{B(min)}$ the ramp-up operation is terminated and the BIASCTRL pin goes low. In the reference design, with the component values shown the minimum bias voltage will be approximately 6 V. When BIALCTRL goes low, Q12 is turned on again and C45 will begin charging back up towards 12 V. The ramp-up phase is then re-started. A maximum of 10 such restarts is allowed before the UCC29910 goes into a latched shutdown mode. Line power cycling is necessary for recovery from this mode.

Typically, the capacitor voltage increases monotonically until the voltage at the VBULK pin reaches VNM. In the circuit of Figure 1 this corresponds to a V_{BULK} across C2 and C21 of 85 V.

This approach allows the fastest possible startup time

Startup Fet Control

In order to save standby power at no load, once the start-up phase is complete, and Vbulk is being regulated (either by the Normal Mode voltage regulation loop, or the SmartBurst light load mode), the BIASCTRL pin is driven high. This is used to turn the start-up fet off which eliminates the power loss in the startup current path.

The gate drive V_{CCA} rail is periodically monitored while in SmartBurst mode. If the V_{CCA} rail is found to have dropped to a level where PFC fet drive capability is compromised, then the startup fet is turned back on to recharge the drive V_{CCA} rail. In this way, the V_{CCA} rail is controlled between 6 V and 7 V.

PFC Drive

A power MOSFET driver will normally be required to convert the PFCDRV output from the UCC29910 to the current and voltage levels typically needed.

CS Pin

The two CS pins must be connected to the same node and it is not possible to leave one floating. The CS pins are used to sense average inductor current during the line cycle and as such the UCC29910 does not provide cycle-by-cycle inductor current limiting. An external circuit is needed if this type of protection is required.

Transient Response and V_{BULK} Regulation

When the UCC29910 is regulating in Normal Mode, V_{BULK} will be regulated at a nominal 84 V_{DC}. An AC ripple at twice line frequency will be superimposed on this as the PFC stage drives current into the bulk capacitors. The amplitude of this ripple will be a function of line frequency, capacitance value and load current. Due to the necessary low control loop bandwidth V_{BULK} will reduce in response to a step load increase. If the load step is large enough to cause V_{BULK} to reduce to less than 79.5 V the loop response is temporarily speeded up until V_{BULK} has been increased back up to 83.5 V at which point the original loop response is restored.

As load current reduces the UCC29910 will continue to regulate V_{BULK} at a nominal 84 V. It will do this by reducing the PWMDRV waveform duty cycle except that any pulses which are commanded to be less than D_{MIN} will be masked and not delivered to the PWMDRV output. The proportion of cycles thus dropped is counted over a 10-ms window and if it exceeds 10% the UCC29910 changes its operating mode to SmartBurst mode.

SmartBurst Mode

At a sufficiently light load on the PFC stage the UCC29910 controller enters SmartBurst mode. In this mode it enters a low power consumption mode to minimise wasted power and improve light load efficiency. Every 1 ms (approximately) the UCC29910 samples V_{LINE} and V_{BULK}. If V_{BULK} is still within a target window of 88 V to 87 V no action is taken. After a sufficient number of samples, the bus voltage will eventually be found to have fallen outside the acceptable ripple window. In this case, a burst of pulses are output at the PFCDRV pin which drive the PFC FET and recharge the PFC bus voltage. The most efficient transfer of power during burst mode is achieved by minimising the number of switching events, thus minimising switching and gate drive losses. The line voltage sample is used in this case to select the maximum safe duty cycle for the PFCDRV pulses while keeping the inductor current discontinuous. Additionally, the pulse duty cycle is ramped over a set of 10 pulses from D_{MIN} to its final value. At the end of the burst, the pulse duty cycle is ramped back down. This avoids the sudden application of long PFC FET on-times which may excite input filter resonances and cause unwanted audio noise generation.

At the lower end of the SmartBurst load range, to avoid bus voltage “pumping” (and possible OVP), V_{BULK} is monitored. The SmartBurst pulse train is terminated if V_{BULK} reaches the peak value of the ripple window or if it exceeds 1.2 ms in length. There is a 5 ms minimum time between the start of successive SmartBurst pulse trains.

The max burst length and minimum burst repetition interval ensure that as load is increased, at some point the burst rate will become insufficient to raise V_{BULK}. Once V_{BULK} has fallen below the minimum burst mode regulation window, then the controller reverts to normal regulation mode.

Revision History

Changes from Original (Deccember 2009) to Revision A **Page**

- Added New DESCRIPTION 1
- Changed 1.0 ms to 1.2 ms 3
- Added 20 kΩ 3
- Changed 100 kΩ to 35 kΩ 3
- Added 50 kΩ 3
- Added Power Factor (PF) 5
- Changed 35 kΩ 5
- Changed UCC29910 Functional Block Diagram 6
- Added rectified 7
- Added The basic Buck PFC power stage is shown in Figure 1. The incoming AC line is fed through a rectifier and filter stages, not shown here. The resulting unipolar voltage (V_{HV}) is then fed into the power stage. The MOSFET is switched at a constant 100 kHz and the freewheeling diode function is provided by D1. The output voltage is developed across the two large capacitors, C2 and C21. 7
- Added The Buck converter operates off a rectified sinusoid, there are periodic dead times when the input voltage is lower than the output. During these times no power can be transferred to the output and the input current is nominally zero. Figure 1 shows the line current, I_{AC}, falling to zero when V_{AC} is less than V_{BULK}. The associated conduction angle increases as the RMS line voltage increases and the current waveform changes from low line to high line. 8
- Added therefore 8
- Deleted V_{BUS} to V_{BULK} 8
- Changed Equation 1 9
- Added is the stage conversion efficiency, ... 9
- Changed 80-V_{BUS} to 84-V_{BULK} 9
- Changed Equation 3 9
- Changed 80 V_{DC} to 84 V_{DC} 10
- Changed Equation 5 10
- Changed 80 V_{DC} to 84 V_{DC} 10
- Changed Equation 7 10
- Deleted Section: Bulk Capacitor Protection Network 11
- Deleted Figure, Buck PFC Bus Overvoltage Protection Crowbar 11
- Deleted Figure, Typical Sidactor VI Characteristic 11
- Changed Ch1 (Y), PFCDRV. 2 V/div Ch2 (R), V_{CCA}. 5 V/div Ch3 (B), DUT V_O, 10 V/div Horiz, 500 ms/div to Start-Up Sequence Waveforms (Ch1 (Y), PFCDRV; Ch2 (R), V_{CCA}; Ch3 (B), DUT V_O) 12