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Understanding and Using Power MOSFET Reliability Data

by Steve Clemente and Ken Teasdale

Abstract

It could reasonably be argued that a design is not complete until its long term performance is known. Design engineers will only be able to calculate it, to the extent that they are, in turn, supplied with reliability information on the devices they are using. This information has previously not been generally available for discrete power semiconductors and only recently power MOSFET manufacturers have begun to publish data that defines the reliability of their products.

This section will attempt to explain the mysteries surrounding manufacturers' power MOSFET reliability data, and will show how this data is derived, what it means, and how it can be used. Actual practical examples will be presented which demonstrate how the manufacturers' data can be used to design for in-circuit reliability of power MOSFETs.

Introduction

As quality and reliability (Q&R) are perceived more and more as a key feature of a successful electronic product, the task of the design engineer becomes more complex.

The circuit designer's attitude typically was that his function was to design the simplest and most economical circuit to do the job, with the components available. He assumed that the components he chose would be adequate and the QPL (if he happened to work for a large company) relieved him of any responsibility on the subject. Those who wanted to tackle the problem found that reliability information was basically unavailable and this made the task of calculating the system reliability a frustrating exercise. This is probably the chief reason why the vast majority of engineers have chosen to ignore the problem or relegate it to a well defined group of specialized people whose results he basically mistrusted.

Over the last few years things have been slowly changing. On the one hand, a number of developments have provided a better understanding of failure behavior of components as well as equipment. On the other hand, components manufacturers have realized that the cheapest way to offer products which — in the long term — will be the most cost effective and have the greatest longevity in the marketplace, is to spare no expense to optimize Q & R through rigorous quality control and long term reliability test programs. An important outcome is the publication by the semiconductor manufacturer of user-oriented data that quantifies failure rates under actual application conditions.

Hopefully this paper will induce some engineers to step from a tridimensional world of design constraints and functional specs into a four dimensional one where performance is looked at over a specified time span.

Power MOSFET Reliability

The conceptual steps to generate reliability information on a device are the following:

(a) Establish — or search for — the dominant failure mechanisms. To do this, the reliability engineer draws from a number of sources like established knowledge on that particular manufacturing technology, literature and his own intuition. Experience and intuition will help him to establish the testing priorities by which he will determine the failure mechanisms.

(b) Run accelerated stress tests aimed at activating the specific failure mechanism being tested for. This is a long, expensive and painful process. To be meaningful it must be done for a very large number of device hours, at elevated temperature, with expensive equipment and on an adequate number of part numbers.

(c) Establish, if possible, a "meaningful" mathematical model for the hazard function and determine its parameters. A model is "meaningful" to the extent that it has a physical underpinning. The availability of such a function can be of great help in understanding the nature of the failure mechanism. As we will see, such a good model is seldom available.

(d) Compute and present the reliability estimates for the different failure mechanisms in a form that can be readily used by design or component engineers.

At this point the work of the reliability engineer is only apparently complete: the key task he still has to accomplish is to relate his results back to R & D or Production Engineering, as appropriate, so that the process can be improved in light of his findings.

In general, failure modes fall into two broad categories — those related to defects within the silicon die itself, and those related to the packaging of the die. The failure mechanisms identified to date for HEXFETs within each of these categories, and the tests that are used to activate them, are discussed in the following sections.

Work is continuing to identify other acceleration factors that would apply, for instance, to drain or gate current, drain voltage, power, etc.

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Die Defects

These may be one of two kinds: field distortion defects, or oxide defects. Failure mechanisms such as electromigration or microcracking of aluminum conductors, slow trapping, surface charge or polarization, though potential problems with MOSFETs have not been detected in HEXFETs yet.

Field Distortion

The presence of polar molecules, such as water and ionic contaminants from the atmosphere, on top of the passivation surface and along the edge of the die, will distort the electric field when a high voltage is applied to the MOSFET, giving increased local leakage current and possible eventual thermal runaway. Failures occur in the random and wearout region, and can be accelerated by high temperature reverse bias burn-in.

In this test, the device is 'reverse biased' by applying voltage between the drain and source — typically 80% of the rated drain-to-source breakdown voltage — with the gate and source grounded (Figure 1). The tests is run at elevated temperature — typically 150°C — and the test runs for several thousand hours. As of June 1987, a total of 13,487 devices had accumulated over 1.9 billion device hours. Section 1.3 of "Reliability Program and Test Results" (also Ref. 1) relates the test results.
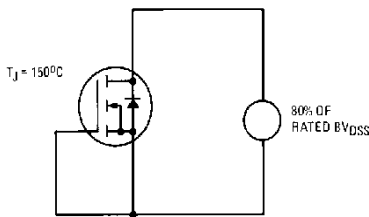

Fig. 1 — High Temperature Reverse Bias Test

For failures in the random region (failure rate substantially constant) the exponential model provides a good approximation:

$$\lambda = Ae^{-\frac{E}{KT}} \quad (1)$$

where λ is the failure rate, E is the activation energy, K is Boltzmann's constant, T is absolute temperature and A is a scaling factor. The activation energy in the above expression is determined by repeating the tests at two different temperatures and solving for E

in the expression for the ratio:

$$\frac{\lambda_{T_1}}{\lambda_{T_2}} = \exp\left[-\frac{E}{K} -\left(\frac{1}{T_1} - \frac{1}{T_2}\right)\right] (2)$$

Once E is known, A can be calculated from (1) in correspondence of a known failure rate and known temperature.

To predict the actual failure rate associated with this failure mechanism under a specific set of operating conditions the design engineer would use the expression (1) together with the appropriate parameter. In doing so he would be implicitly disregarding the fact that these figures are statistical in nature and are valid within some "confidence level" that is a function of the amount of data that has been collected. The plot in Figure 2 presents that same information with the appropriate confidence level.
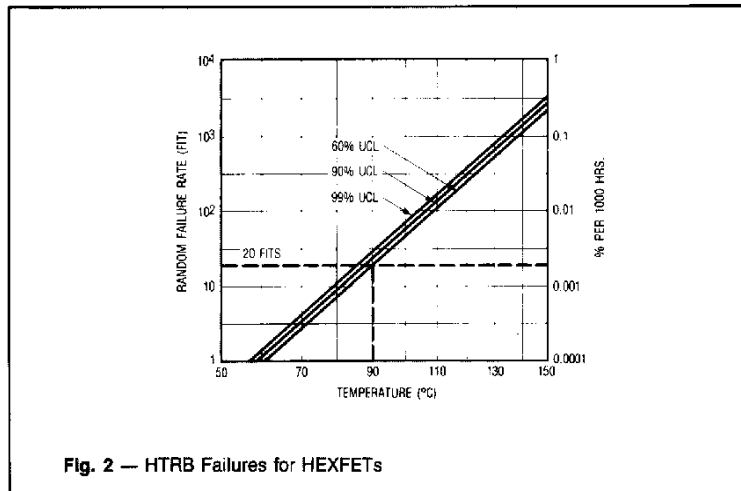

Fig. 2 — HTRB Failures for HEXFETs

It may be worth pointing out that device burn-in will not reduce the failure rate due to field distortion for two reasons:

(1) These failures occur in the random region, which is typical of strong population. No trace was found of a "weak" population that could be weeded out by burn-in.
(2) The failure rates are such that any reasonable burn-in (168 hours) will not have any noticeable effect.

Oxide Defects

Micro-defects in the devices's gate-oxide layer cause random failures, at a very low rate, in the infant and random regions. These defects lead to failures in the form of a gate-to-source short-circuit. They can be activated by high-temperature gate-stress burn-in testing (Figure 3).

In this test, a forward bias voltage is applied between gate and source, while drain and source are connected to ground. The test is run at elevated
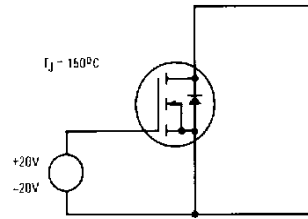

Fig. 3 — Gate Stress Test

temperature. As of June 1987, 3856 devices on long-term gate stress test accumulated over 4.7 million device-hours. Test results are shown in Section 1.3 of "Reliability Program and Test Results" (also Ref. 1).

For the failures, D. L. Crook (Reference 2) proposes an acceleration expression made up of two components:

$$\frac{\lambda_1}{\lambda_2} = \exp\left[-\frac{E_A}{K} -\left(\frac{1}{T_2} - \frac{1}{T_1}\right)\right]$$

$$\times \exp\left[-\frac{(E_2 - E_1)}{E_c}\right] \quad (3)$$

The first being a thermal acceleration factor according to the Arrhenius model, the second a voltage dependent factor, with $E_2 - E_1$ the electric field differential between the two test conditions and E_C an electric field constant,

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equivalent to the activation energy. To determine these constants the test was run at two different temperatures (100 and 205°C) and two different gate voltages (28 and 30V). The electric field constant came out to be 6.5 10⁶ V/m which is very close to the value of 6.2 mentioned in Reference 2.

The Expression 3 or Figure 4 can be used interchangeably to predict the actual failure rate as a function of gate voltage. This does disregard the statistical nature of the data and, in doing so, we will be assuming that the results obtained from a given population are 100% applicable to the entire population. Confidence levels for these results will be calculated later on.

The data from the thermal acceleration portion of the experiment are shown in Figure 5 together with their linear regressions. The fact that these two lines intersect indicates that there is not a good basis for the application of the Arrhenius model to the results in their present form. After some searching, it was found that his "aberrant" behavior was due to more than one failure mechanism in the test population. A closer scrutiny of the data presented in Figure 5 showed that the data points could be divided into two groups, those below 8% and those above 10% accumulated fails. Linear regression applied independently to both failures yielded parallel lines thereby confirming the validity of the assumption (Figures 6 and 7). The resulting parameters for the lognormal distribution are shown in Table I.

The significant difference between the two activation energies underscores the distinction between the two failure mechanisms, one for a weaker population and one for a stronger population. This implied that the first failures were caused by both failure mechanisms while the failures over 10% were only due to the lower activation.

Table I

Population	Leg	Temperature T (°C)	σ	μ	Activation Energy Ea (J)
< 8% of Accumulated Failures	3	100	1.7	8.4	.65 10⁻¹⁹
	4	205	1.7	5.7	
> 10% of Accumulated Failures	3	100	4.6	16.3	.19 10⁻¹⁹
	4	205	4.6	15.7	

To purge the first fails from the second failure mechanisms we write the acceleration factor for the two combined:

$$\exp\left[\frac{E_t}{K}\left(\frac{1}{T_2} - \frac{1}{T_1}\right)\right]$$

$$= \exp\left[\frac{E_1}{K}\left(\frac{1}{T_2} - \frac{1}{T_1}\right)\right]$$

$$\times \exp\left[\frac{E_2}{K}\left(\frac{1}{T_2} - \frac{1}{T_1}\right)\right]$$

where E_t and E_1 are known (.65 10⁻¹⁹ and .19 10⁻¹⁰ respectively) while $E_1 = E_t - E_2 = .46$ 10⁻¹⁹ joules which is in close agreement with the .3eV published in Reference 2. The final result of the above evaluation is presented in Figure 8 in a form that can be directly utilized by design engineers.

Such a clear-cut distinction between the stronger and the weaker component of the population could conceivably make burn-in a most effective tool to weed out the weaker component.

However, a quick glance at Figure 4 will show that a standard gate burn-in test (150°C, $V_{GS} = 80\%$ of max. rated) will take 10¹⁰ second to weed out a tiny 1% of the population, i.e. some 3200 years! This amounts to saying that burn-in, under those conditions, is a waste of time and money and it should be strongly questioned, unless it is mandated by powers that are beyond our control. The linear regression line for 100°C (Figure 7) shows virtually no distortion from the higher activation energy failure mechanism we would like to weed out. If that failure mechanism hardly makes its presence felt at 100°C, which is a fairly high operating temperature for all but the most demanding applications, why bother weeding it out? Whenever, on the other hand, burn-in is mandated, the possibility of using voltages and temperatures above those normally used should be seriously considered. With reasonable values like $T_J = 175°C$ and $V_{GS} = 28V$ the acceleration factor with respect to the 20V line of Figure 4 is 1.34×10^6 which means that in 48 hours (1.728×10^5 secs) more than 12% of the devices would fail, devices that, as we pointed out before, might not have failed in a practical application.

Packaging Defects

The main problems of the silicon interfaces are the following:

(A) Die attach fatigue that is normally caused by the temperature differential between the die and the header and by the different thermal
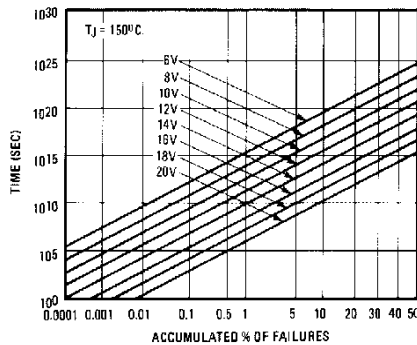

Fig. 4 — Projected Log Normal Accumulated Failures as a Function of Gate Voltage
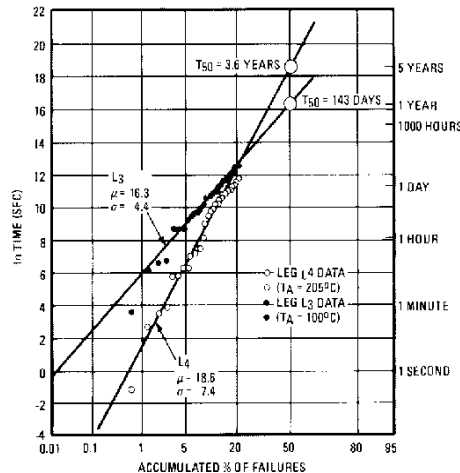

Fig. 5 — Data Points From The Thermal Acceleration Portion of the Gate Stress Test

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expansion coefficients of silicon and the header material. This shows up as cracking or separation of the die or voiding the die attach, resulting in degraded on-resistance and/or thermal resistance, and eventual thermal runaway. These failures largely occur in the wearout region. The susceptibility of a given die attach to thermal fatigue is normally ascertained with a power cycling test (Figure 9). In this test, drain current is supplied until the case temperature rises a given amount — typically 70°C. Power is then shut down and cooling fans force the temperature back to ambient. The cycle is repeated until significant degradation starts to occur. Each cycle typically takes about two to six minutes.

(B) Wire bond fatigue. This program is similar to the previous one and shows up as a separated wire bond.

It can also be tested by power cycling the parts although simpler but less effective tests are sometimes used (temperature cycling, without any power being applied).

(C) Metal corrosion. When the die is packaged in a non-hermetic package it is subject to a deterioration process that will be described later. The standard test to accelerate this failure mode it 85/85; 85°C and 85% relative humidity. We found this test to give only a superficial indication of meaningful operating conditions in so far as it disregards the applied bias that is normally present in a circuit. The test circuit we have used (Figure 10) includes a bias voltage as an accelerating factor.

Power Cycling Tests

Since the results of these tests are comprehensive of the two failure modes

A and B, the search for a model would not be appropriate.

Test results to this date (June, 1987) established two key points:
— The dependency of the power cycling capability on die size, package and bonding wire size;
— the adequacy of the Arrhenius model to provide acceleration factors that are consistent with the test result.

Further evaluation is required to fully qualify all dice and all packages. Tests at different power levels would also be required to obtain a larger number of die attach failures. This involves a substantial amount of work that is being carried out now.

In light of the above, the cumulative failure shown in Figures 11 and 12 should be taken as in indication of device capability more than actual design parameters. The activation energies appear to be $0.59 \ 10^{-19}$ joules
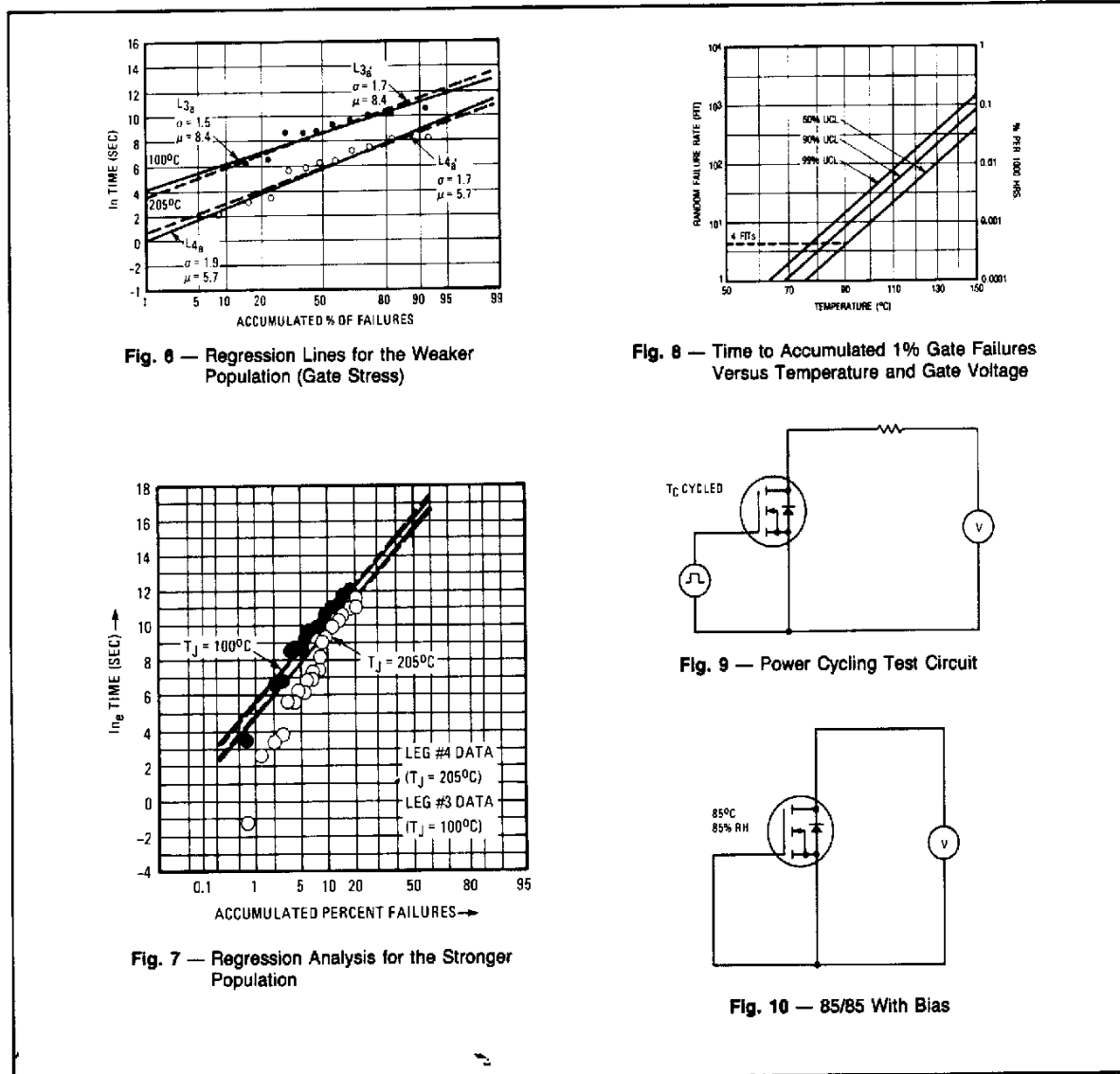

Fig. 6 — Regression Lines for the Weaker Population (Gate Stress)

Fig. 8 — Time to Accumulated 1% Gate Failures Versus Temperature and Gate Voltage

Fig. 7 — Regression Analysis for the Stronger Population


Fig. 9 — Power Cycling Test Circuit

Fig. 10 — 85/85 With Bias

for the IRF330 and 0.464 10^{-19} for the IRF350. Here too, device/equipment burn-in will not improve the reliability of the devices because this type of failure is characteristic of the wearout region.

Metal Corrosion with Bias Acceleration

Under the environmental stress conditions of humidity/temperature/bias, it is expected that one of two failure modes will normally predominate: 1) excess leakage currents under reverse bias will increase to the point of causing a parametric failure of I_{DSS} or, 2) corrosion of the internal metallization will result in a parametric shift in the on-resistance. $R_{DS(on)}$, eventually resulting in an open circuit condition. The cause of both of these phenomena is the ingression of water into the plastic package from the ambient atmosphere to the chip surface, forming external surface leakage paths. This can lead to excessive drain current and eventually parametric failure.

The application of reverse bias under blocking conditions ($V_G = V_S$) can result in cathodic corrosion of the source bond pad. As the corrosion proceeds, the aluminum source pad slowly dissolves causing intermittent continuity between the source wire and the top metallization of the chip. Eventually, the continuity goes altogether and the device presents an open circuit. The cathodic corrosion process is electrochemical in nature and is governed by the following equations (a and b) as described by van de Ven and Koelmans (Reference 3):

(a) $e^- + H_2O \rightarrow OH^- + \frac{1}{2} H_2$

(b) $OH^- + Al + H_2O \rightarrow AlO_2^- + 3/2 H_2 \rightarrow$
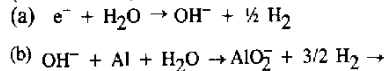
Electronic current, externally leaking from the source metallization to the drain, reacts with water according to the first equation, liberating hydrogen gas and creating hydroxyl radicals in the immediate neighborhood of the aluminum source pad. The hydroxyl radicals then reacts with the aluminum, in the presence of water, to form a soluble oxide of aluminum as in the second equation. The rate at which this process proceeds under 85°C/85% RH conditions is regulated by the amount of surface leakage current and by availability of water. The water must not only be present on the aluminum bond pad, but also on the sides of the chip, forming a conductive leakage path.

Once water is present on the chip, the electronic current available to take part in the corrosion will depend on the amount of applied bias. To evaluate this dependance various applied drain potentials were used on several groups of HEXFETs as described previously.

From the test result the acceleration factor due to the applied bias is shown in Figure 13. The resulting set of lines allow the projection of cumulative failures in time for any particular applied bias on a HEX-3 device in a TO-220 package in 85°C/85% RH conditions. The reader might notice that under these conditions, if the applied bias is substantial, plastic devices would not last too long. It might be argued, though, that the 85/85 conditions are unduly severe and do not reflect a realistic operating condition.

The results obtained to this date (June 1987) seem to confirm the accelertion factor reported in Reference 4:

$$AF = \left(\frac{RH_2}{RH_1} \right)^n exp \left[\frac{E_a}{k} \left(\frac{1}{T_1} - \frac{1}{T_2} \right) \right]$$

With:

RH = relative humidity (1 is lower, 2 is higher)

T = absolute temperature (1 is lower, 2 is higher)

E_a = experimental thermal activation energy

k = Boltzman constant
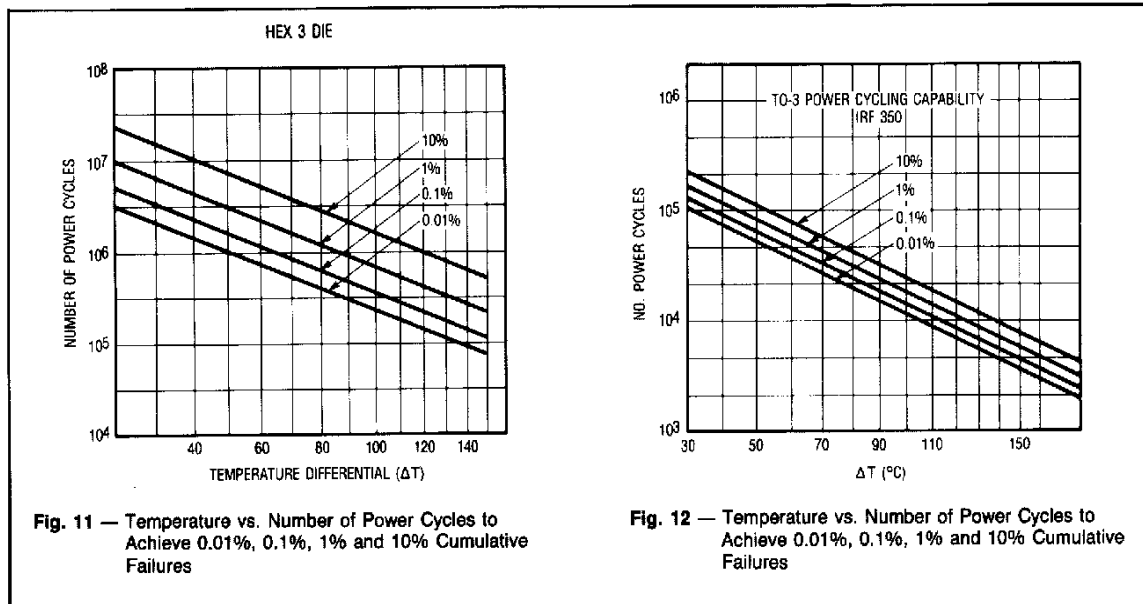
n = experimental humidity power parameter

E_a is in the order of 0.8eV and n is estimated to be 2.7

Here too, it may be worth pointing out that device or equipment burn-in would not accomplish anything since the failure mechanism is associated to device wearout.

Using the Failure Data To Calculate Circuit Reliability

In those applications where the devices would be subjected to a dominant stress that happens to be one of those we tested for, the reliability information supplied in our Reliability Report could provide a fairly straight forward answer. Two examples are shown in the next section. If, on the other hand, there is no dominant stress calculations have to take in account all factors as shown in the section entitled

"The Effects of Combined Stresses."

Fig. 11 — Temperature vs. Number of Power Cycles to Achieve 0.01%, 0.1%, 1% and 10% Cumulative Failures

Fig. 12 — Temperature vs. Number of Power Cycles to Achieve 0.01%, 0.1%, 1% and 10% Cumulative Failures

Dominant Stress

The following examples illustrate how the failure-rate data can be used by the designer to calculate incircuit reliability.

Example 1 — 250W Switching Power Supply

A high-rel power supply is to be designed that will provide a continuous output of 250W to a dedicated load, 24 hours per day. A HEXFET and heat-sink are to be selected that will keep HEXFET-related power supply failure rate to just 0.1% over a 5 year period. The maximum applied gate voltage is 12V, (meaning that gate failure rates are so low that they can be ignored). The principal failure mechanism will be governed by temperature and failure rates are quantified in Ref. 1. Maximum ambient temperature is 45°C.

Number of operating
hours in 5 years   = 43,800

Number of device operating hours per 1000 power supplies in 5 years (.1% of device failure permitted)   = 8.76×10^7

Permitted failures
per 10^9 hours   = 11.4 FITs

From the
HEXFET's FIT's
curve:
Max. permitted T_J
(Ref. 1)   84°C

Assuming a half bridge circuit operating from 220V minus 15% (low line) and an efficiency of only 80%, the rectifier current is 1.2A and a peak current in each device is 2.7A at a duty cycle of 45%. With these assumption, the following two alternatives are possible.

(a) The IRF430. The junction to sink thermal resistance is 1.8 deg. C/W and the maximum $R_{DS}(on)$ is 2.4 ohms at T_J = 84°C. Figure 14(a)

(b) The IRF440, which is a larger HEXFET die in the same TO-3 package. This has a maximum $R_{DS}(on)$ of 1.36 ohms at T_J = 84°C, and a junction to sink thermal resistance of 1.1 deg. C/W. Figure 14(b)

(a) IRF430
Conduction losses = $2.7^2 \times 2.4$
$\times 0.45$
= 7.8W
Temperature rise,
junction-to-ambient = 84 − 45
= 39°C
Thermal resistance,
junction-to-ambient = 39/7.8
= 5°C/W
Thermal resistance,
sink-ambient   = 5 − 1.8
= 3.2°C/W
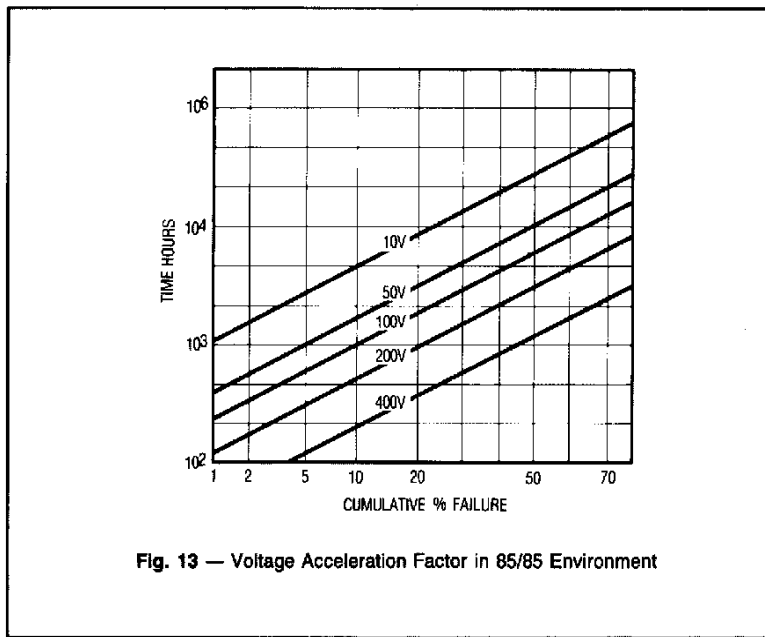

Fig. 13 — Voltage Acceleration Factor in 85/85 Environment

(b) IRF440
Conduction losses = 2.7×1.36
= 4.46W
Thermal resistance,
junction-ambient = 39/4.46
= 8.7°C/W
Thermal resistance,
sink-ambient   = 8.7 − 1.1
= 7.6°C/W

Example 2: Failure rates in relation to gate voltage

One of the major features of power HEXFETs is that they can handle very high peaks of current. The fundamental design limitations on the peak current handling capability are junction heating and maximum gate voltage.

The HEXFET is a "linear" device, and greater the peak current, the greater the gate drive voltage needed to ensure that the device is "fully enhanced." Figure 4 shows that increasing gate voltage produces increasing failure rates, particularly at gate voltage about 16V or so. Therefore, operation at very high peak current, while being operationally practical, will have an effect on long-term reliability, in as much as high peak drain current of necessity requires relatively high peak gate voltage.

The effect will be most significant for devices with relatively low drain-source voltage rating. This is because low voltage devices have low on-resistance with correspondingly high peak current handling capability, and need more gate drive voltage to achieve their high peak current ratings. To take an example (Figure 15) an IRF330, rated 400V, is fully enhanced at rated peak current of 22A with just 12V gate voltage. The IRF130, rated 100V, needs virtually 20V gate voltage for full enhancement at its rated peak current of 56A.

To see how operation with high peak currents impacts the reliability let's take, as an example, a buck converter operating from a 48V bus with a nominal output current of 7A. Reliability requirements are the same as those seen in the previous example and the following conditions also apply.

Device mounted on heatsink
with total $R_{th}J\text{-}A$ = 4°C/W

Maximum ambient
temperature   = 45°C

Maximum average
power dissipation = $7^2 \times .18 \times$
1.75
= 15.4W

Maximum junction
temperature   = 15.4 × 4 +
45 = 106.7°C

Notice that since the buck converter has only one device, twice as many FITs are permitted in this application as opposed to the previous one and the operating conditions indicated above satisfy the reliability requirements (Figure 1.1.1 of Ref. 1). Because of delays in the current sensing loop, the minimum duty cycle under short circuit conditions is 4% with a peak current of 40A. Under these conditions, maximum junction temperature is not to exceed 150°C. It follows that:

Max. power that
can be dissipated
$(\Delta T/R_{th})$ = (150 − 45)/4
= 26.25W

Max. allowable $R_{DS}(on)$
@ 150°C   = $P/(I^2pk \ *D.C.)$
= 26.25/ $(40^2 \times$
.04)
= .41 ohm

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Max. allowable $R_{DS(on)}$
@ 25°C   = .23 ohm

Figure 16 shows the relationship between drain current, on-resistance, and gate voltage at T_J = 25°C. Table II shows the maximum achievable peak drain current for a given gate voltage with the specified limitation of .23 ohm. It appears that, with some margin, a gate voltage of 18V will satisfy the peak current requirements and the gate drive circuit has to be designed to provide that voltage on a continuous basis. For these conditions (107°C and V_{GS} = 18V) we find, (Ref. 1) that it takes a few days to accumulate a .1% of failures so that the reliability criteria are definitely not met and a bigger device has to be considered. Going through the same procedure for an IRF142, we find that the peak current requirements are satisfied with a gate voltage of less than 12V, so that all conditions would be met.

The Effects of Combined Stresses

In an ideal design there should not be a dominant stress, nor should there be a dominant failure mechanism in a given device. The consequences of such a statement are far reaching: It implies that the device manufacturer should be well versed with the applications for his devices and keeps them in mind when he designs them. It also implies that the design engineer is intimately familiar with the device and chooses its operation point to get the most out of it.

Of course this is far from being a real condition and the previous examples are more typical of what occurs in practice. For the sake of completeness, though, we shall touch briefly on the effects of combined stresses.
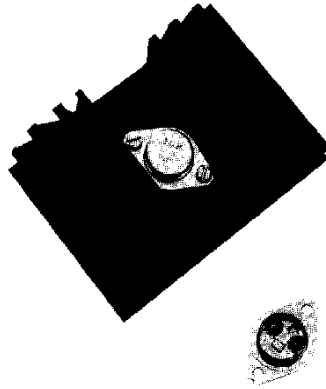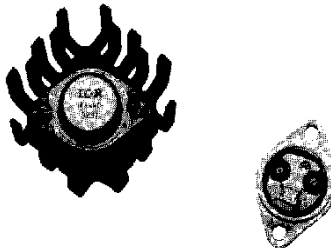

Figure 14(a): IRF430 on a "large heatsink

Figure 14(b): IRF440 on a "small" heatsink

Figure 14: Reliability trade-offs. These HEX-FET/heatsink combinations are for a high-rel 250W switching power supply with a calculated HEXFET related failure rate of just 0.1% over 5 years continuous operation. The same reliability can be achieved with the "small" HEXFET and "large" heatsink in (a) or with the "large" HEXFET and "small" heatsink in (b).

A group of devices operating at 125°C with 16V on the gate will experience a constant failure rate of approximately .5 10^{-6} device failures/our due to field distortion and it will accumulate 1% of failure in approximately 5 10^9 secs due to gate stress (10 failures in 5 10^9 seconds, i.e. 7.2 10^{-9} devices/hour). On a 1000 unit sample, over a five year period, (42,720 hours) there will be:

21.36 failures due to field distortion
 .31 failures due to gate stress

By raising the gate voltage to 17V the gate stress failure would go to 2.4 10^{-7} device failures per hour and the corresponding gate failures for that stress would be 10.25, which is comparable to the number of field distortion failures.

These failures are summable to the extent that their number is small compared to the total population otherwise they should be corrected to take into consideration the fact that the population decreases as failures occur and that, once a device has failed, it cannot fail again.

Table II

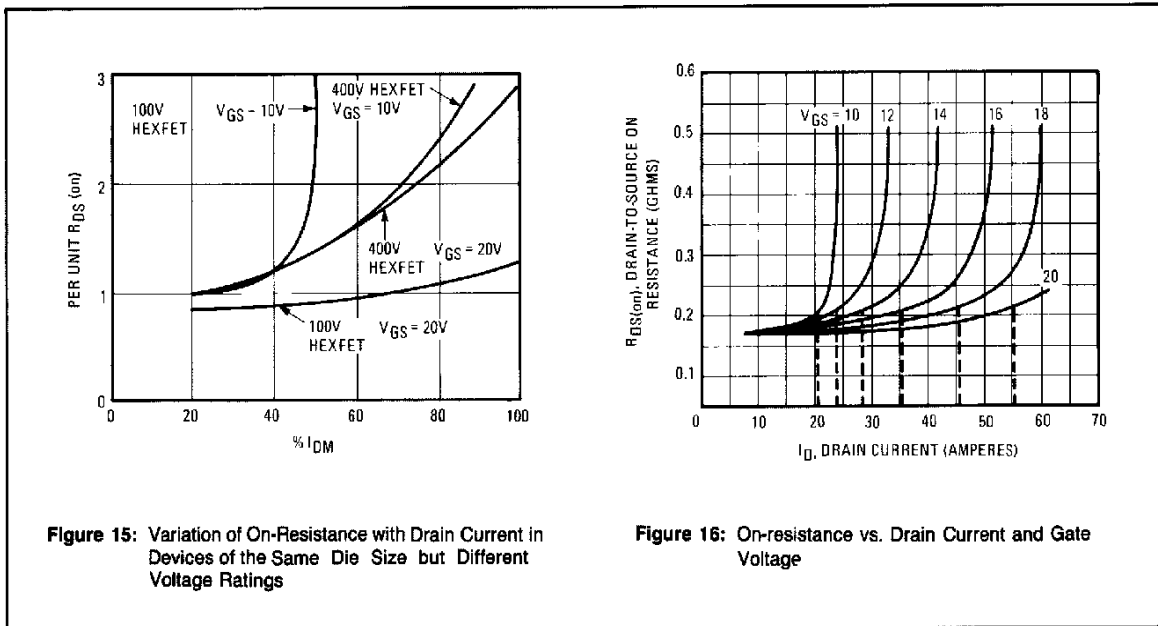| V_{GS} V	Peak Current (A)
20	55
18	45.5
16	35.5
14	28.5
12	24.0
10	20.5

Figure 15: Variation of On-Resistance with Drain Current in Devices of the Same Die Size but Different Voltage Ratings

Figure 16: On-resistance vs. Drain Current and Gate Voltage

Cost Considerations

It may be appropriate, at this point to clarify the terminology a bit by defining quality and reliability:
— Quality is a measure of the relative amount of defective parts at the time of shipment. Statistical sampling techniques are normally employed to measure quality directly (AOQL = actual outgoing quality level, or PPM) or indirectly (AQL = acceptance quality level).
— Reliability measures the capability of a device to perform as specified over a period of time, as we have seen in the previous section.

The tools available to **components manufacturers** to achieve the objective of a higher quality and more reliable device are basically the following:
— incoming material, process and assembly monitoring
— lot certification
— outgoing quality control
— long term reliability programs

Equipment manufacturers, on other hand, have been following one or more of the following procedures:
— incoming inspection
— device and/or equipment burn-in
— device/vendor qualification
— design auditing to established procedures

It is easily realized that the items listed above make up a very expensive shopping list and, as every engineer knows, the concern for quality and reliability has to be tempered by the economical considerations dictated by the competitive environment the product will face.

Unfortunately substantial costs are also incurred in renouncing Q & R.

Components of poor quality will require board reworking or scrapping. Poor reliability will increase warranty repairs, down time, and customer dissatisfaction.

The only rational way of solving this dilemma is to look at Q & R as a capital investment and determine its payback. In order to do this its costs have to be quantified.

If we subscribe to the traditional notion that to improve Q & R action should be intensified on the items listed above we would find that beyond a certain level the costs become very high and do not provide commensurate results. Interestingly enough, of the two most expensive procedures, incoming inspection becomes detrimental once the AOQL goes below .04% because of the additional handling of the parts, while device burn-in, as shown in the previous section, serves no purpose if good long term reliability information is available. In other words, a component manufacturer that can supply parts to a very low AOQL and has appropriately researched their long term reliability will be able to save the customer a significant amount of money in incoming inspection (Ship to Stock), board reworking, scrap, and burn-in.

Vendor qualification and design auditing procedures would still be left in place, but with a different emphasis.

Since the equipment manufacturer is now relying on data supplied by the vendor it should periodically check on how they are generated and that the lot qualification procedures are adhered to. Furthermore he must provide accurate and timely feedback on in-plant and field failures to correct any potential

problem before it develops. He may also want to consult with Application Engineeering in setting up proper design auditing procedures. It will be appreciated that the costs associated with vendor qualification and auditing procedures are negligible compared to a high quality incoming inspection and device or equipment burn-ins.

Conclusion

User-oriented failure rate data for MOSFETs is a new design tool available to the user. They enable MOSFET reliability performance to be calculated and optimized at the design stage. The data presented show that HEXFETs, applied within their ratings, exhibit extremely low failure rates. This, coupled with a very low AOQL figure substantially reduces the cost of building quality and reliability into a product.

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