AN1338

Grid-Connected Solar Microinverter Reference Design Using a dsPIC® Digital Signal Controller

Author: *Mohammad Kamil*
Microchip Technology Inc.

INTRODUCTION

As the world is more and more concerned with fossil fuel exhaustion and environmental problems caused by conventional power generation, renewable resources are becoming a focal point of the environmental movement, both politically and economically. Such renewable resources includes photovoltaic (PV) and wind generation systems.

Using renewable resources on a large scale is a cost problem and in most cases, more research is needed to make their use cost-effective. PV systems, also termed solar microinverters, have gained greater visibility during the past several years as a convenient and promising renewable energy source. These energy systems have several advantages compared to other forms of renewable power, such as wind energy.

The main drawbacks of PV energy are the high cost of manufacturing silicon solar panels and the low conversion efficiency. With the newer techniques of manufacturing crystalline panels and efficient power converter design, it is possible to make a PV project cost-effective.

The conversion of the output voltage from a solar panel into usable DC or AC voltage must be done at its Maximum Power Point, or MPP. MPP is the PV output voltage at which the PV module delivers maximum energy to load.

SPECIFICATIONS, DEMANDS, AND STANDARDS OF A SOLAR-POWERED SYSTEM

Interfacing a solar microinverter module with the power grid involves two major tasks. One is to ensure that the solar microinverter module is operated at the Maximum Power Point (MPP). The second is to inject a sinusoidal current into the grid. Since the inverter is connected to the grid, the standards given by the utility companies must be obeyed. The EN61000-3-2, IEEE1547 standards, and the U.S. National Electrical Code (NEC) 690, are worth considering. These standards deal with issues like power quality, detection of islanding operation, grounding, and so on.

These inverters must be able to detect an islanding situation, and take appropriate action in order to prevent bodily harm and damage to equipment connected to the grid. Islanding is the continued operation of the inverter when the grid has been removed intentionally, by accident, or by damage. In other words, if the grid has been removed from the inverter; the inverter should then stop attempts to supply power to the grid or energize the grid.

The most common solar technologies today are the monocrystalline and multicrystalline silicon modules. A PV cell can be modeled as shown in Figure 1, and its electrical characteristics are shown in Figure 2. The MPP voltage range for these PV modules is normally defined in the range from 27V to 45V, at a power generation of approximate 200W, and their open-circuit voltage is below 45V.

FIGURE 1: SIMPLIFIED MODEL OF A PV CELL

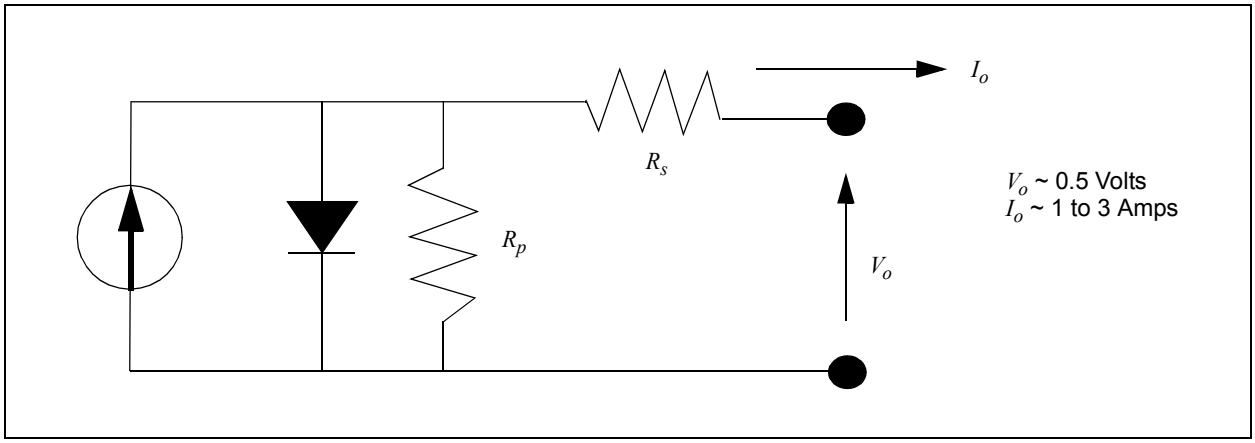
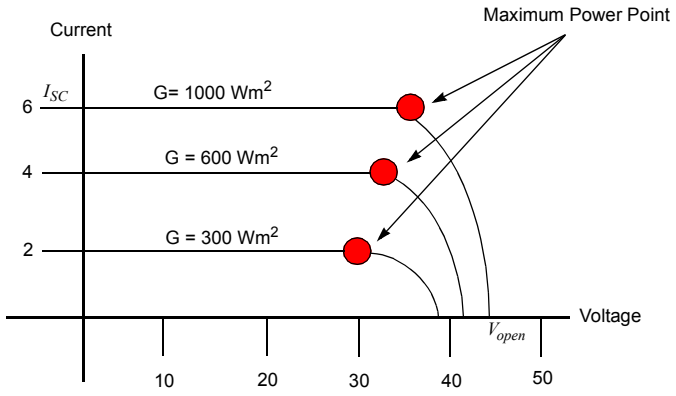


FIGURE 2: PV MODULE ELECTRICAL CHARACTERISTIC



I-V versus illumination (36 cell string)

Solar microinverters must guarantee that the PV module is operated at the MPP, to capture maximum energy from the PV module. This is accomplished by the maximum power point control loop known as the Maximum Power Point Tracker (MPPT). It also involves PV output voltage ripple at the terminals of the PV module being sufficiently small, in order to operate around the MPP without too much variation in PV current.

ELECTRICAL CHARACTERISTICS OF SILICON PV CELLS

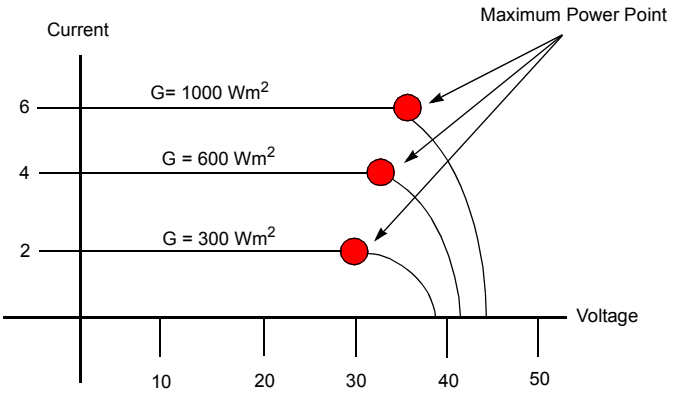
PV cells are semiconductor devices, with electrical characteristics similar to a diode. However, a PV cell is a source of electricity, rather than an electrical load (a diode), and operates as a current source when light energy, such as sunlight, makes contact with it.

A PV cell will behave differently depending on the size of the PV panel or type of load connected to it and the intensity of sunlight (illumination). This behavior is called the PV cell characteristics.

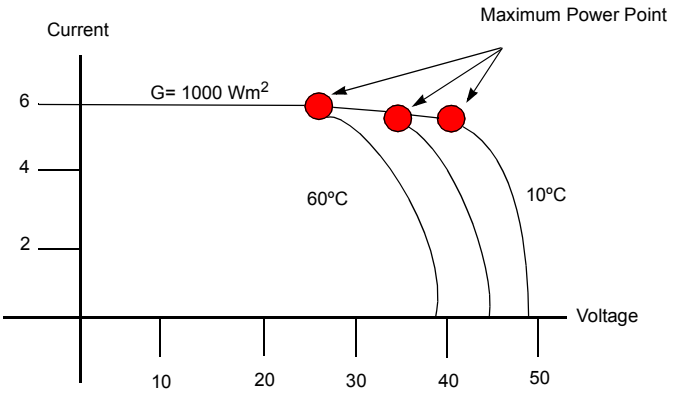
The characteristics of a PV cell are described by the current and voltage levels when different loads are connected. When the cell is exposed to sunlight and is not connected to any load, there is no current flowing and the voltage across the PV cell reaches its maximum. This is called an open circuit (V_{open}) voltage. When a load is connected to the PV cell, current flows through the circuit and the voltage drops. The current is maximum when the two terminals are directly connected with each other and the voltage is zero. The current in this case is called a short circuit (I_{SC}) current, as shown in Figure 2. Comparisons can be made to the electrical characteristics of different PV cells as these measurements are made at standard test conditions (STC), which are defined as a light intensity of 1000 W/m2 and a temperature of 25°C.

The light intensity as well as temperature affects the PV cell characteristics. Current is directly proportional to light intensity. Voltage also changes with fluctuating light levels, but the change in the voltage is less. Voltage is more affected by changes in the temperature of the PV cell than the current. An increase in cell temperature decreases the voltage and increases the current by a very small amount. How these influences affect an I-V curve is illustrated in Figure 3 and Figure 4. It can be seen that changing (decreasing) the light intensity has a much greater effect than changing (increasing) the temperature. This is true for all commonly used PV materials. The important result of these two effects is that the power of a PV cell decreases when light intensity decreases and/or temperature increases.

FIGURE 3: PV MODULE ELECTRICAL CHARACTERISTICS WITH LIGHT INTENSITY AND TEMPERATURE



I-V versus illumination (36 cell string)



I-V versus temperature (36 cell string)

Maximum Power Point (MPP)

A solar cell may operate over a wide range of voltages (V) and currents (I). By continuously increasing the resistive load on an irradiated cell from zero (a *short circuit*) to a very high value (an *open circuit*), the MPP can be determined (the point that maximizes V x I); that is, the load for which the cell can deliver maximum electrical power at that level of irradiation. (The output power is zero in both the short circuit and open circuit extremes).

A high quality, monocrystalline silicon solar cell, at 25°C cell temperature, may produce 0.60 volts open-circuit (V_{OC}). The cell temperature in full sunlight, even with 25°C air temperature, will probably be close to 45°C, reducing the open-circuit voltage to 0.55 volts per cell. The voltage drops modestly with this type of cell, until the short-circuit current is approached (I_{SC}).

Maximum power (with 45°C cell temperature) is typically produced with 75% to 80% of the open-circuit voltage (0.43 volts in this case), and 90% of the short-circuit current. This output can be up to 70% of the V_{OC} x I_{SC} product. The short-circuit current (I_{SC}) from a cell is nearly proportional to the illumination, while the open-circuit voltage (V_{OC}) may drop only 10% with an 80% drop in illumination. Lower quality cells have a more rapid drop in voltage with increasing current and could produce only 1/2 V_{OC} at 1/2 I_{SC}. The usable power output could thus drop from 70% of the V_{OC} x I_{SC} product to 50% or even as little as 25%.

The maximum power harvesting is accomplished with an MPP tracker (MPPT). It also involves PV output voltage ripple at the terminals of a PV module being sufficiently small, in order to operate around the MPP without too much fluctuation. Analysis of the circuit in Figure 1 shows that there is a relationship between the amplitude of the voltage ripple and the utilization ratio, as expressed in Equation 1 and Equation 2.

EQUATION 1:

$$\hat{U} = \sqrt{\frac{(k_{PV}-1)\cdot 2\cdot P_{MPP}}{3\cdot \alpha \cdot U_{MPP}+\beta}}$$

Where $\hat{U}$ is the amplitude of the voltage ripple, P_{MPP} and U_{MPP} are the power and voltage at the MPP, α and β are the coefficients describing a second-order Taylor approximation of the current, and the utilization ratio is given as the average generated power divided by the theoretical MPP power.

EQUATION 2:

$$\hat{U} = 2\cdot \sqrt{\frac{(k_{PV}-1)\cdot P_{MPP}}{\left(\frac{d^2P_{PV}}{dU_{PV}^2}\right)}}$$

The coefficients are computed, as shown in Equation 3 through Equation 7.

EQUATION 3:

$$i_{PV} = \alpha \cdot U_{PV}^2 + \beta \cdot u_{PV} + \Upsilon$$

EQUATION 4:

$$u_{PV} = U_{MPP} + \hat{u} \cdot Sin(\omega \cdot t)$$

EQUATION 5:

$$\alpha = 0.5 \cdot \frac{d^2 I_{MPP}}{dU_{MPP}^2}$$

EQUATION 6:

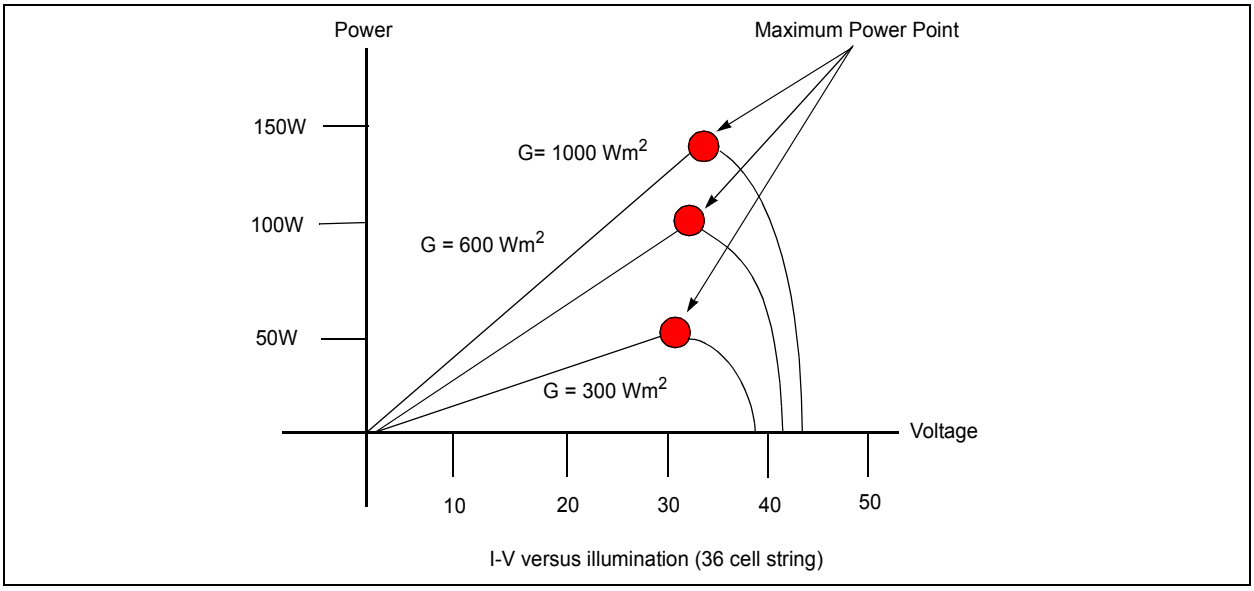
$$\beta = \frac{dI_{MPP}}{dU_{MPP}} - 2\cdot \alpha \cdot U_{MPP}$$

EQUATION 7:

$$\Upsilon = \alpha \cdot U_{MPP}^2 - \frac{dI_{MPP}}{dU_{MPP}} \cdot U_{MPP} + I_{MPP}$$

Calculations show that the amplitude of the ripple voltage should be below 8.5% of the MPP voltage in order to reach a utilization ratio of 98%. For example, a PV module with an MPP voltage of 35V should not be exposed to a voltage ripple of more than 3.0V (amplitude) in order to maintain a utilization ratio of 98%. As seen in the previous section, the power injected into the grid follows a sinusoidal wave, raised to the second power, for which reason the inverter must contain a power decoupling device.

FIGURE 4: PV MODULE ELECTRICAL CHARACTERISTICS MAXIMUM POWER POINT

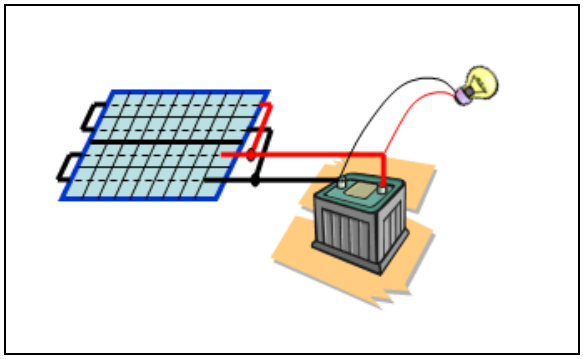


SOLAR POWER SYSTEM EVOLUTION

PV cells have been used in many applications to generate electricity. A few of these are briefly discussed in this section.

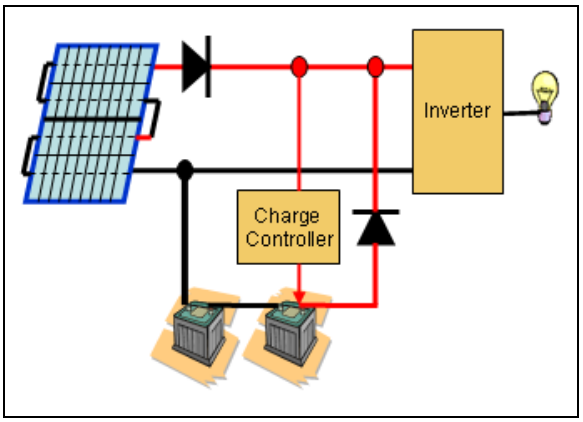
Log Cabin System – A simple 12 volt DC system provides lighting for isolated cabins. Low wattage (<100W) solar panels are connected directly to a battery. The battery is connected to lamps and other 12 volt DC appliances as shown in Figure 5. The battery life is compromised by unregulated current charging. Available appliances are limited for 12 volt DC power, because wire resistance limits power to a few hundred watts. This system is not connected to AC power lines and is considered to be “off the grid”.

FIGURE 5: LOG CABIN SYSTEM



Country Home System – Larger panels providing 24-96 volts are connected to an inverter to yield 120/240 V_{AC} to operate standard lighting and appliances as shown in Figure 6. Battery life is improved with a regulated charging module. The higher DC voltages support moderate power levels. This system is not connected to AC power lines and is considered to be “off the grid”.

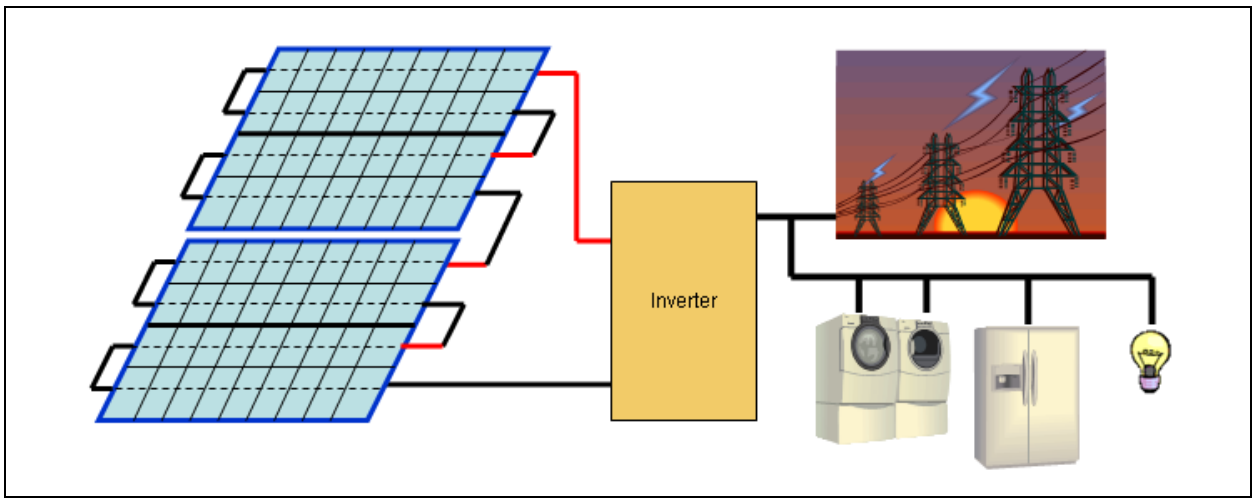
FIGURE 6: COUNTRY HOME SYSTEM



Urban Home System – Larger panels providing 200-400 volts are connected to an inverter to yield 120/240 V_{AC} at medium power levels (2-10kW). This system is connected to AC power lines (i.e., connected to the grid) as shown in Figure 7. The customer sells power to the power company during the day and buys power from the power company during the night. The grid-connected approach eliminates expensive and short-lived batteries.

A couple of issues exist with this system. One, the inverter has potential as a single point of failure; and two, non-optimal power harvesting from the solar panels, especially in partial shading conditions.

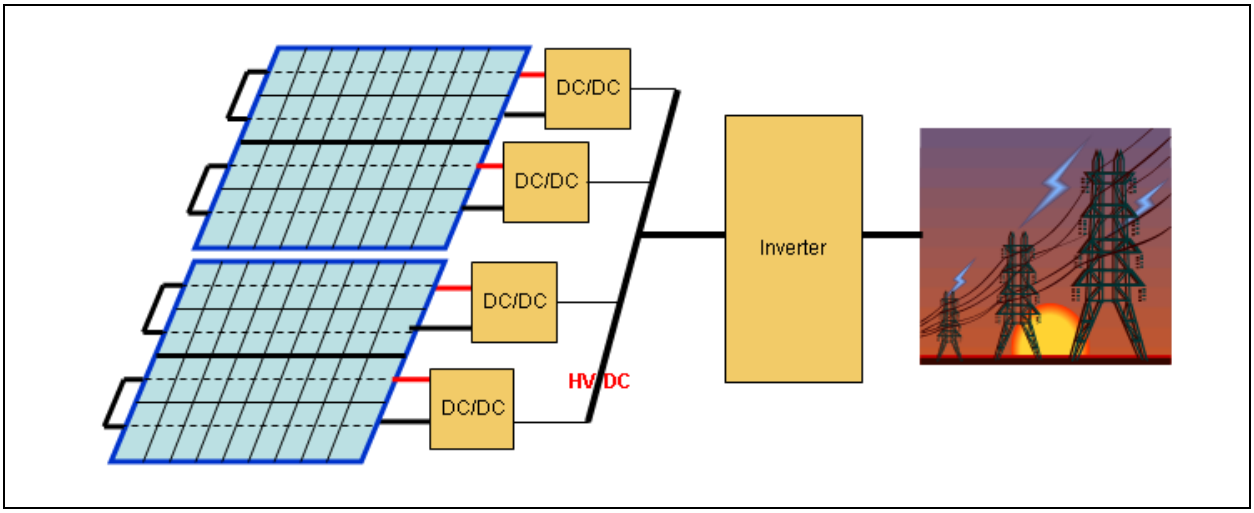
FIGURE 7: URBAN HOME SYSTEM



Single Inverter With Multiple DC/DC Converters – The use of DC/DC converters per string provide enhanced power harvesting from solar panels as shown in Figure 8. The DC/DC converters may be separate modules or reside within the inverter module.

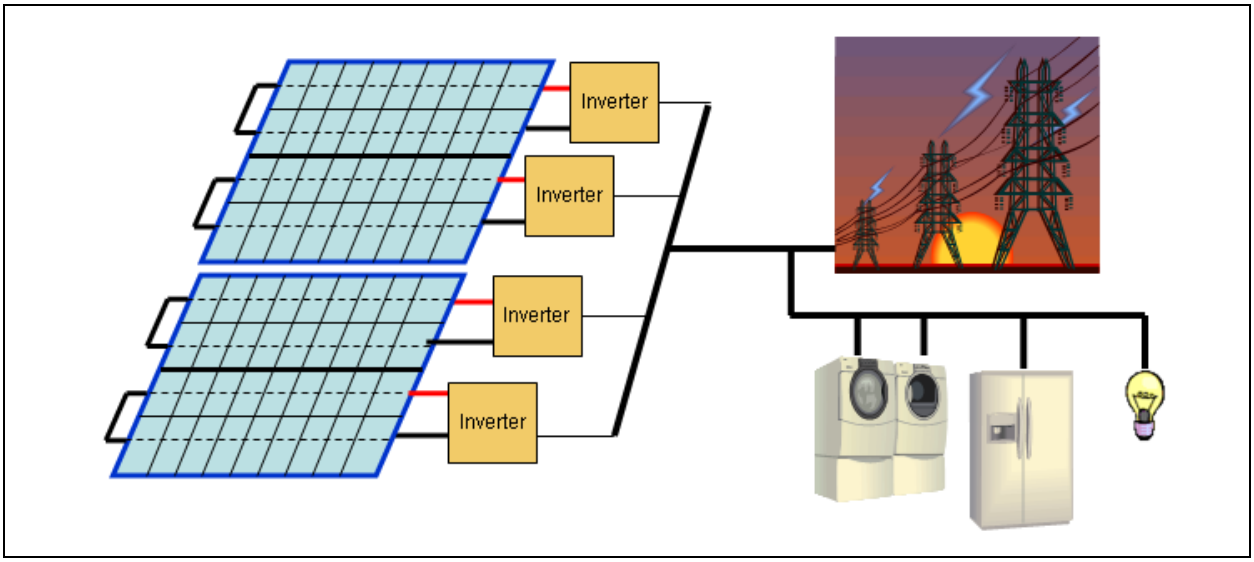
This method is still susceptible to single-point-failure of the inverter, and involves the distribution of high voltage DC power – a potentially dangerous situation because direct current power fusing is difficult to achieve.

FIGURE 8: SINGLE INVERTER WITH MULTIPLE DC/DC



Urban Home System With String Inverters - Panels providing 200-400 volts are connected to multiple inverters to yield 120/240 V_{AC} at medium power levels (2-10kW). The inverters are connected to the grid as shown in Figure 9. Use of multiple inverters provides enhanced power harvesting from solar panels and also provides enhanced system reliability.

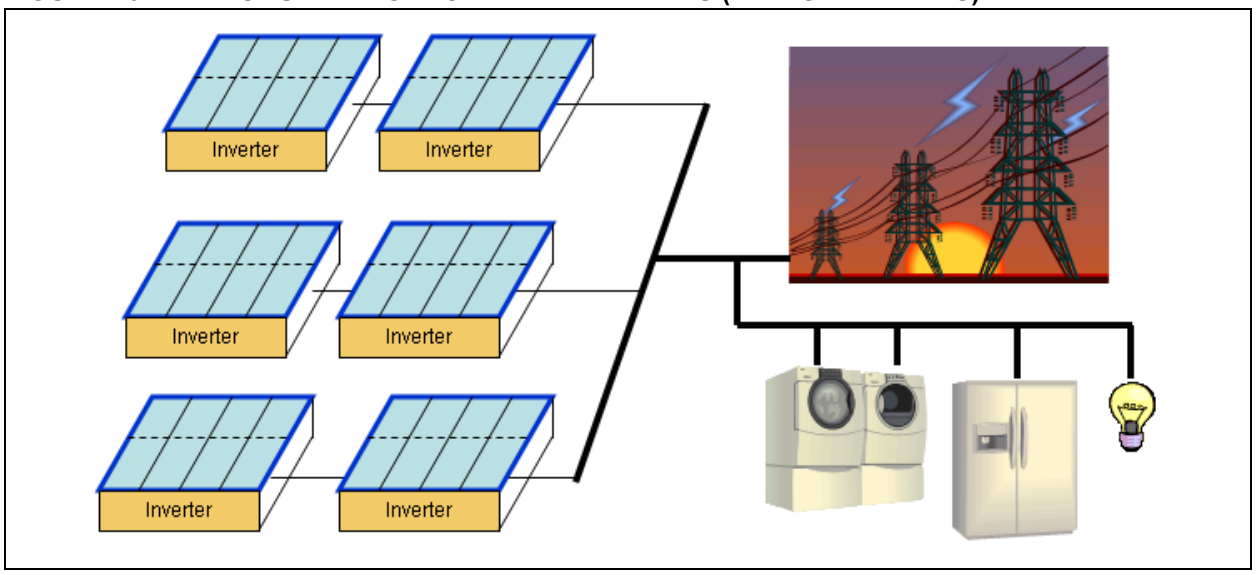
FIGURE 9: URBAN HOME SYSTEM WITH STRING INVERTERS



Module Incorporated Inverters – Each solar panel module incorporates its own inverter. Module-incorporated inverters are also known as microinverters. A microinverter system is shown in Figure 10.

The incorporation of inverters into the solar panels greatly reduces installation labor costs, improves safety, and maximizes the solar energy harvest.

FIGURE 10: MODULE INCORPORATED INVERTERS (MICROINVERTERS)



Why a Microinverter?

- Moving from centralized inverters to distributed inverters optimizes the energy harvest.
- Incorporating converters into the solar panel modules reduces installation costs.
- Improves system reliability from 5 to 20 years by reducing converter temperatures and removing fans.
- Replacing hard-switching techniques with soft-switching ii mp roves efficiency and reduces heat dissipation.
- Standardized designs (hardware and software) improve reliability and reduce costs – from cottage industry to mass production.
- Eliminates electrolytic capacitors (due to high failure rate) – designs require higher voltages to reduce current, which allows use of lower capacitance non-electrolytic capacitors.
- Converters that are tied to the grid eliminate the need for batteries in many applications. Batteries are very expensive, require maintenance, and are short-lived.
- Microinverters tend to be lower powered (only a few hundred watts), which tends to lower internal temperatures and improve reliability.
- Microinverter solar systems require many inverters to handle a specific power level – driving up production quantities, which reduces cost

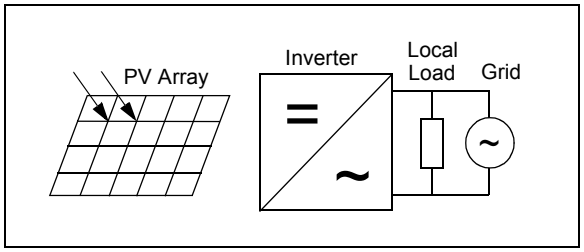
Solar Microinverter Requirements

- Maximum Power Point Tracking (MPPT) algorithm is required to optimize the power harvest from solar panels
- System efficiency > 94% (as high as possible)
- Wide DC input voltage range
- Cost < $0.50 per watt (production quantity)
- Safety: Fault detection and anti-islanding
- AC quality, Total Harmonic Distortion (THD) <5%: meets IEEE 519 standard

GRID-CONNECTED SOLAR MICROINVERTER SYSTEM

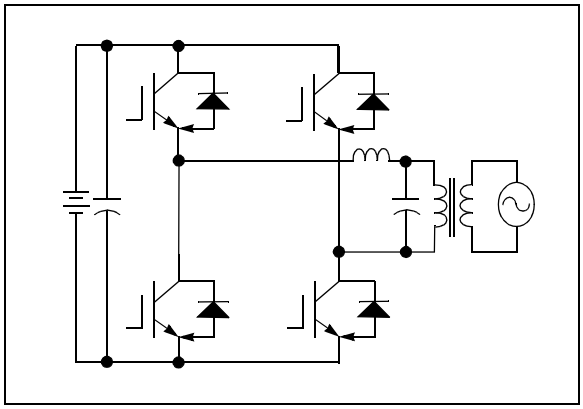
A general structure of a grid-connected solar microinverter system is shown in Figure 11.

FIGURE 11: GRID-CONNECTED SOLAR MICROINVERTER SYSTEM



A buck-derived full-bridge inverter shown in Figure 12 is used in grid-connected solar microinverter systems. This configuration does not have the flexibility of handling a wide range of input PV voltage, and requires heavy line frequency step-up transformers.

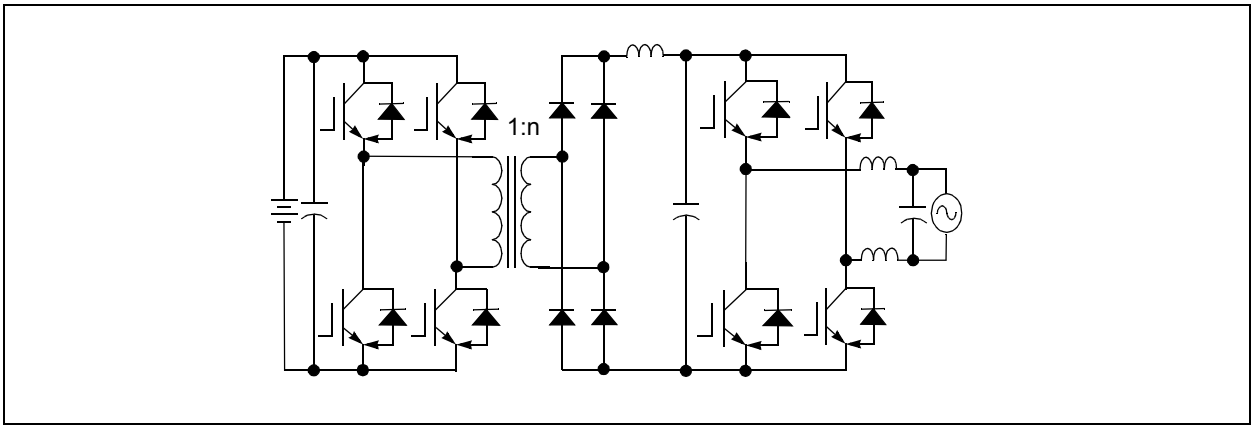
FIGURE 12: SINGLE-STAGE FULL-BRIDGE INVERTER



To accommodate a large input voltage range, the two-stage topology is generally used, as shown in Figure 13.

The first stages of the inverter system boost the low voltage of the PV panel to high voltage DC with or without isolation. The topology used in the first stage can be simple boost, push-pull or full-bridge. The second stage of the converter produces sinusoidal output voltage and current in synchronization with the grid voltage. The general topology used for this stage is full-bridge and half-bridge. The two-stage topology makes the system costly and complicated, especially for a single PV panel system. To make the system simple, the high efficiency and reduced cost single-stage topology is used.

FIGURE 13: TWO-STAGE TOPOLOGY FOR SOLAR MICROINVERTER SYSTEM



GRID-CONNECTED SOLAR MICROINVERTER REFERENCE DESIGN

The reference design in this application note describes a single-stage grid-connected solar (PV) microinverter. A simple flyback converter is used to achieve sinusoidal output voltage and current that is in phase and in synch with the grid. This microinverter has been designed to connect any PV module having maximum power rated up to 220 watt with input voltage range of 25 V_{DC} to 45 V_{DC}, and a maximum open circuit voltage of 55V.

The specifications of the reference designs are as follows.

110V Solar Microinverter System

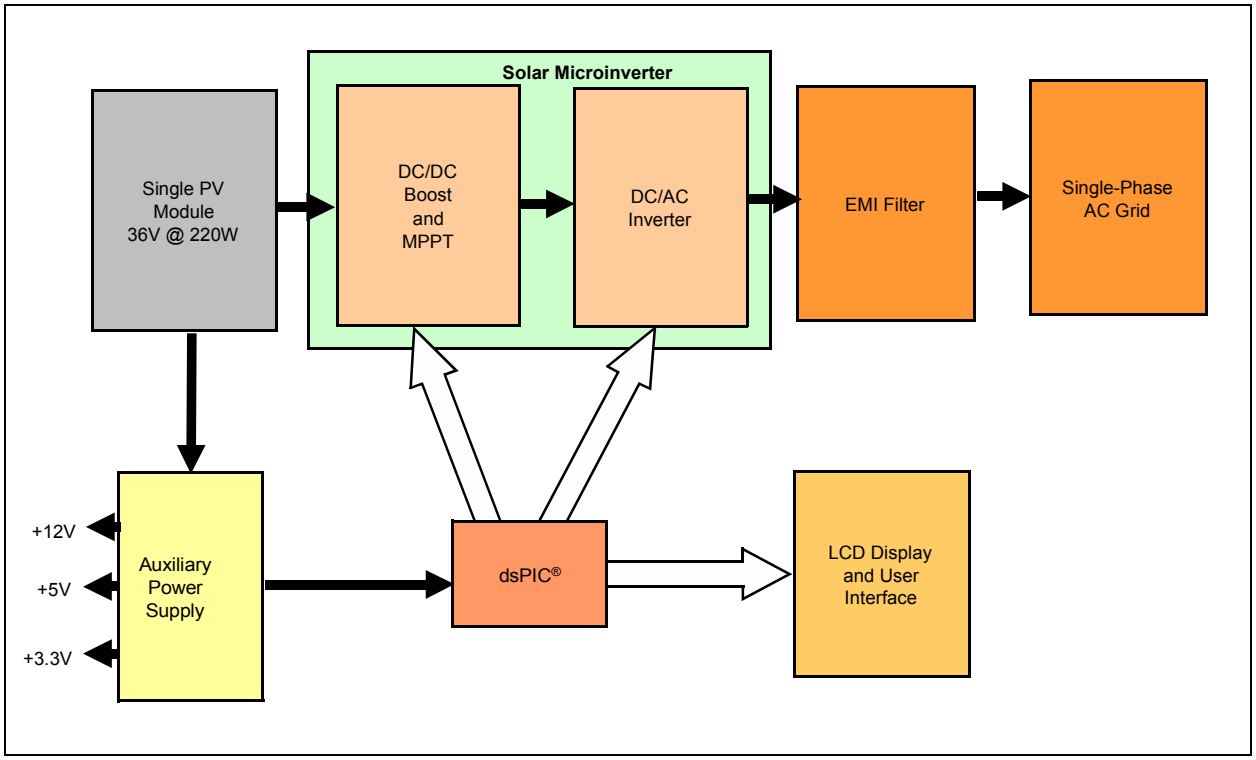
- Maximum output power = 185 watt
- Nominal output voltage = 110V
- Nominal output current = 1.7A
- Output voltage range = 90 V_{AC}-140 V_{AC}
- Output frequency nominal frequency = 60 Hz
- Output frequency range = 57 Hz-63 Hz
- Power factor = >0.95
- Total harmonic distortion = <2%

230V Solar Microinverter System

- Maximum output power = 185 watt
- Nominal output voltage = 230V
- Nominal output current = 0.8A
- Output voltage range = 180 V_{AC}-264 V_{AC}
- Output frequency nominal frequency = 50 Hz
- Output frequency range = 47 Hz-53 Hz
- Power factor = >0.95
- Total harmonic distortion = <5%
- Efficiency
  - Peak efficiency = 95%
  - Maximum Power Point tracking = 99.5%
  - Minimum efficiency>0.8

A block diagram of the grid-connected solar microinverter reference design is shown in Figure 14.

FIGURE 14: SOLAR MICROINVERTER REFERENCE DESIGN BLOCK DIAGRAM



The PV panel output is converted to sinusoidal output current and voltage in phase with the grid. An EMI/EMC[1] filter is used to suppress the EMI/EMC noise and provide impedance between inverter output and the grid. The auxiliary power for the controller and all feedback circuitry is derived from the PV panel voltage. A single Microchip dsPIC33F 'GS' series device (dsPIC33FJ16GS504) is used to control power flow from the PV panel to the grid. The dsPIC DSC also executes the MPPT algorithm, fault control, and optional digital communication routines.

A key requirement of the grid-connected solar microinverter is high efficiency over a wide range of input voltage and input power since these variables are defined in very wide ranges as functions of solar irradiation and ambient temperature. Furthermore, the inverter must be highly reliable (long operational lifetime) since most PV module manufacturers offer a warranty of 25 years on 80% of initial efficiency. The electrolytic capacitor used for power decoupling between the PV module and the single-phase grid is the main limiting component inside the inverter. The operational lifetime of electrolytic capacitors provided by most manufacturers varies from 5000 hours to 10000 hours.

The life span of the electrolytic capacitor is determined by Equation 8.

EQUATION 8:

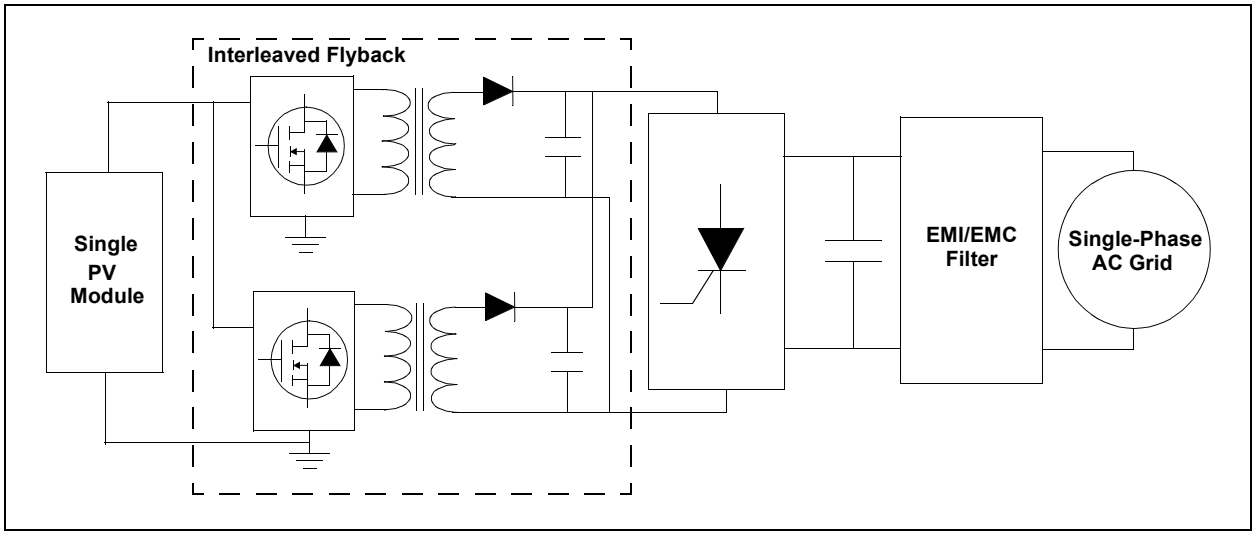
$$L_{hrs} = L_{hrsto} \cdot 2^{\left(\frac{(t_0 - t_h)}{\Delta t}\right)}$$

L_{hrs} is operational lifetime, L_{hrsto} is operational lifetime at temperature, t_0, t_h is the hotspot temperature and Δt is temperature rise, which reduces the lifetime by a factor of two. The ripple current in the electrolytic capacitor produces heat, which causes a rise in temperature. The ratio of operating ripple current RMS to rated ripple current RMS also affects the life of the capacitor.

The Grid-Connected Solar Microinverter Reference Design uses an interleaved flyback converter, as shown in Figure 15.

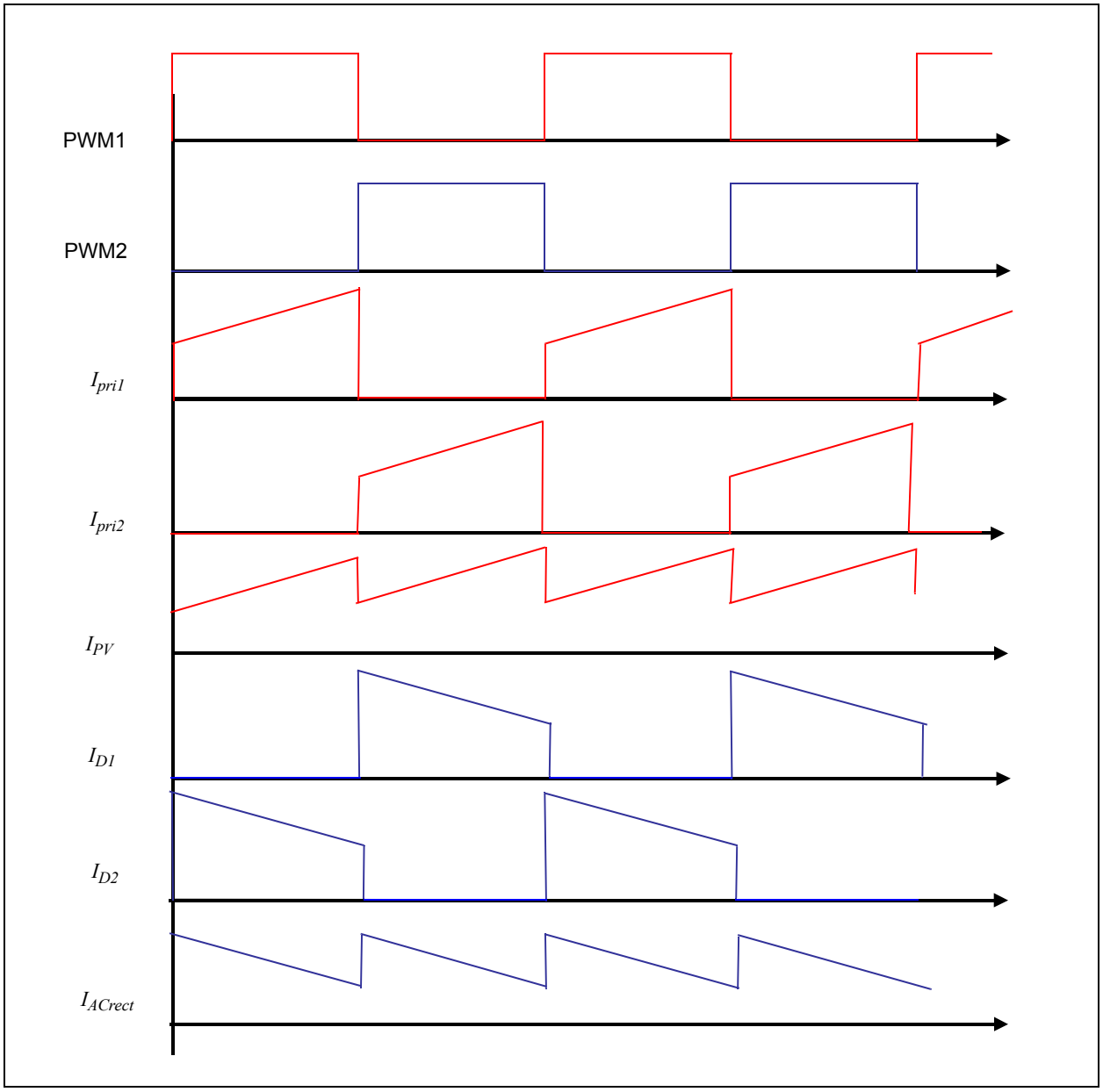
1. Electromagnetic interference = EMI
   Electromagnetic capability = EMC

FIGURE 15: INTERLEAVED FLYBACK CONVERTER BLOCK DIAGRAM



The interleaved flyback converter reduces the ripple current RMS through the input bulk electrolytic capacitor, which increases the life of the capacitor. Output current ripple also reduces by interleaving action resulting in low output current THD. The input and output current waveform of the interleaved Flyback converter at 50% duty cycle operation of the flyback MOSFET is shown in Figure 16.

FIGURE 16: CURRENT AND VOLTAGE WAVEFORM OF INTERLEAVED FLYBACK CONVERTER



Listing of I/O Signals for Each Block, Type of Signal, and Expected Signal Levels

The block diagram in Figure 17 illustrates measurement of the grid voltage required for Phase-Locked Loop (PLL), output current control, and system islanding. The inverter output voltage measurement is required for synchronization inverter output to grid voltage and system islanding.

The grid current is measured to make sure the inverter supplies the sinusoidal current in phase with the grid. PV voltage and flyback MOSFET current is measured for MPP detection. In addition, two MOSFET currents are measured for load balancing of both converters.

FIGURE 17: SOLAR MICROINVERTER RESOURCES DIAGRAM

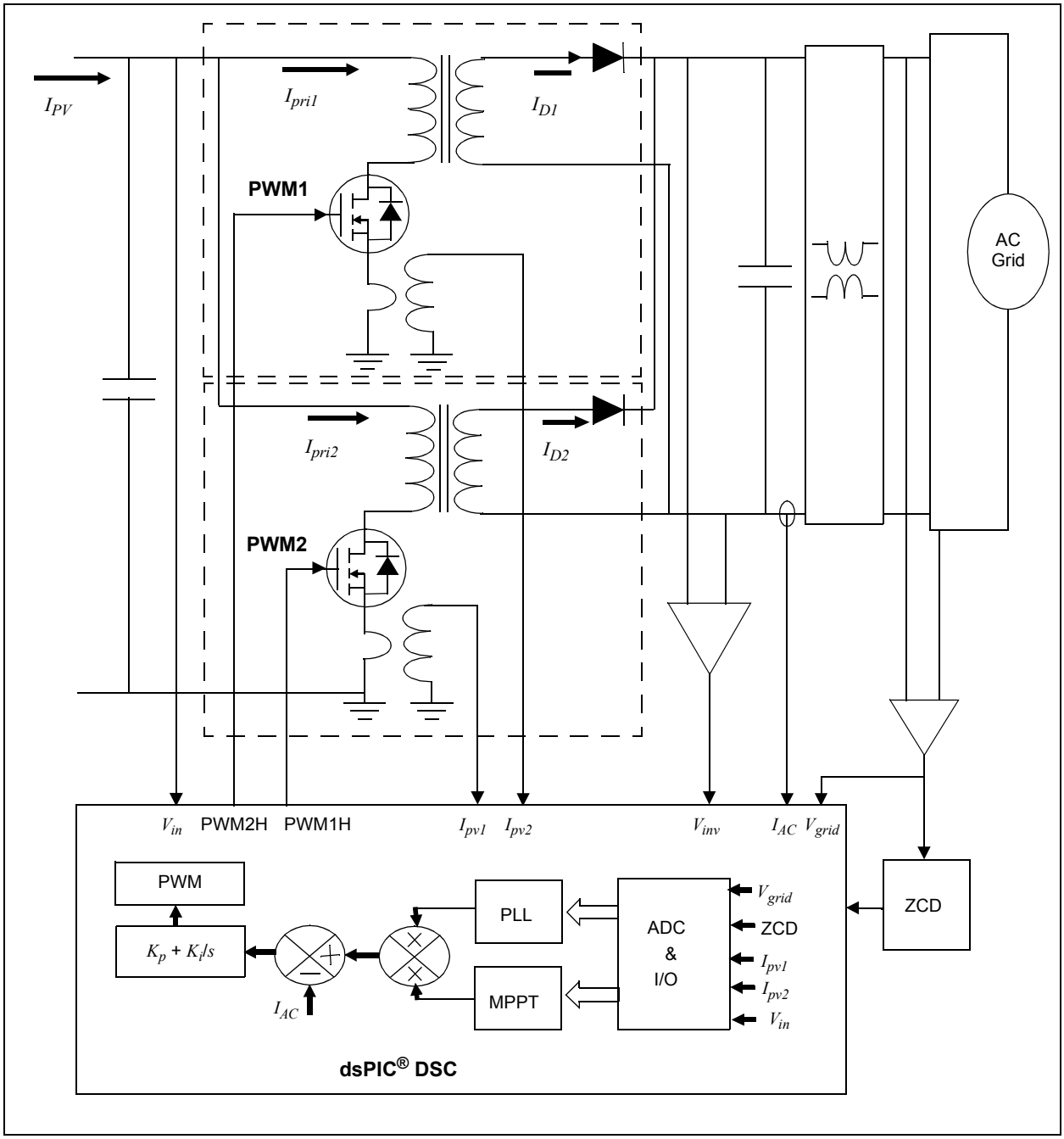


Table 1 provides the resources required for a digital solar microinverter design.

TABLE 1: REQUIRED RESOURCES FOR DIGITAL SOLAR MICROINVERTER DESIGN

Signal Name	Type of Signal	dsPIC DSC Resources	Expected Signal Level
V_{pv}	Analog	AN1	0-2.4V
I_{pv1}	Analog	AN0	0-2.0V
I_{pv2}	Analog	AN2	0-2.0V
V_{inv}	Analog	AN3	0-3.3V
V_{grid}	Analog	AN4	0-3.3V
I_{AC}	Analog	AN5	0-3.3V
Flyback MOSFET Gate Drive	Digital	PWM1H, PWM2H	—
Flyback Active Clamp MOSFET Gate Drive	Digital	PWM1L, PWM2L	—
Vac_Zero_Cross	Zero-Crossing Detect, Digital	RB15	—

Microinverter Circuit Operation

The DC input from the PV module is fed to the flyback primary. A modulated high-frequency sine PWM is used for the flyback MOSFET to generate the rectified sine output voltage/current across the flyback output capacitor. The two flyback converters are operated 180 degrees out of phase to accomplish interleaving operation. The flyback topology operates in two modes.

- **Mode 1:** When the flyback MOSFETs (Q7/Q8) turn ON, energy is stored on the primary of the flyback transformers (TX5/TX6). The diodes (D1/D2) are in a blocking state, as voltage applied across the diode is reverse-biased from the transformer secondary winding. During this time, the flyback transformer behaves like an inductor and the primary current (I_{pri1}/I_{pri2}) of the transformers (TX5/TX6) rises linearly as shown in Figure 16. Load current is supplied by the output capacitor.
- **Mode 2:** When the flyback MOSFET turns OFF, the voltage applied across the primary winding is reversed, producing the secondary winding's voltage, which forward biases the output diodes (D1/D2). The stored energy in the primary is transferred to the secondary, which charges the output capacitor and supplies current to the load. During this time, output voltage is applied directly across the transformer secondary winding and subsequently the diode current decreases linearly, as shown in Figure 16.

The snubber circuitry diodes (D18/D17), capacitors (C19, and C15/C11, C12) and active clamp circuitry MOSFET (Q2/Q1) and capacitors (C13, C14/C9, C19) are used to clamp the flyback primary MOSFETs (Q7/Q8) voltage to a safe value. When the MOSFETs turn OFF, voltage applied across the drain to source (V_{ds}) will be a summation of input voltage, clamp voltage across, and leakage spikes voltage due to transformer leakage inductance.

A modulated sine PWM generates modulated sine primary MOSFET current, producing the diode secondary diode current, as shown in Figure 18. The average of the sine modulated secondary diode current produces a rectified sine voltage/current across the output capacitor.

An SCR full-bridge is used to unfold rectified output voltage/current to sinusoidal voltage/current. Therefore, the SCR is switched at line frequency. The output of the inverter is synchronized with the grid by digital PLL. The MPPT controls the magnitude/rms of the output current. The shape of the output current is controlled by current control loop. Sine modulated PWM operation of the flyback MOSFETs transfers the packet of energy to the inverter output capacitor. I_{pri1} is the flyback1 converter MOSFET current and I_{sec1} is the flyback1 output diode current.

The secondary diode current (I_{sec1}) is filtered by the flyback output capacitor and produces sinusoidal output voltage across the output capacitor.

Figure 19 shows the input solar microinverter voltage and PV inverter output voltage/current waveform before the SCR full-bridge. Figure 20 shows the solar microinverter output voltage/current waveform and its unfolded voltage/current waveform after the SCR full-bridge.

FIGURE 18: SINE-MODULATED PRIMARY MOSFET AND SECONDARY DIODE CURRENT

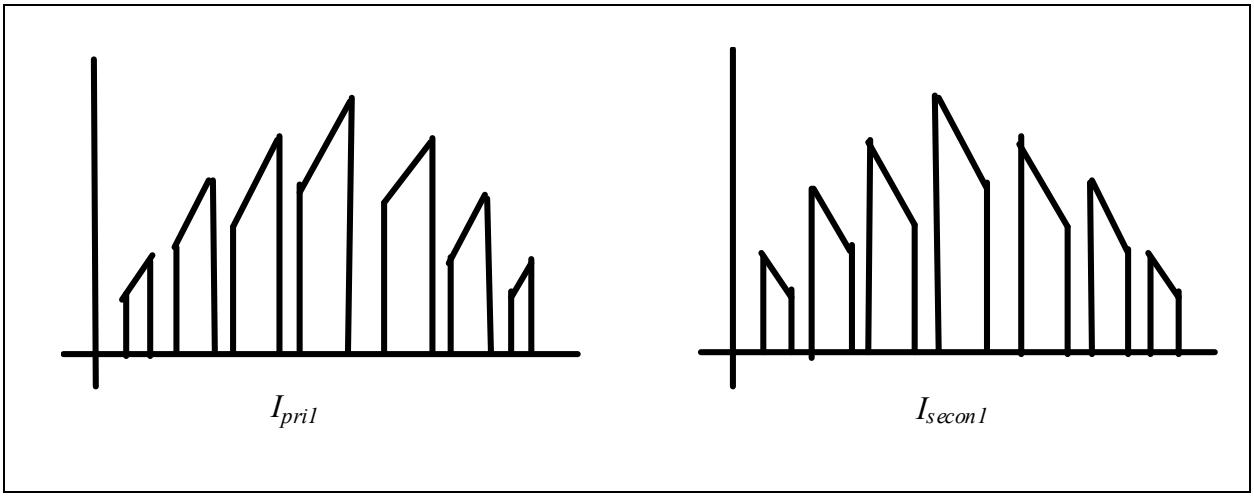


FIGURE 19: FLYBACK I/O VOLTAGE/CURRENT WAVEFORM

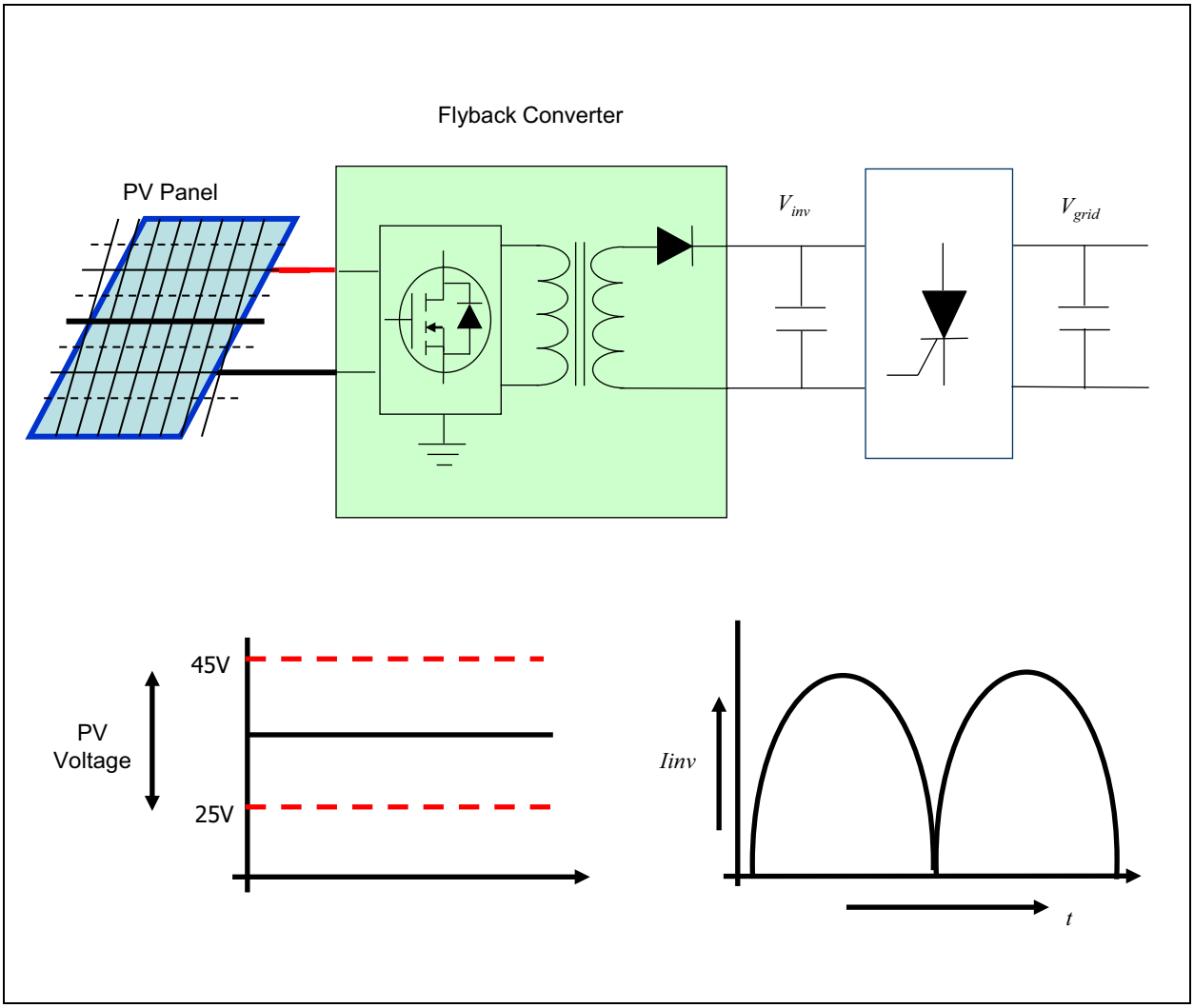
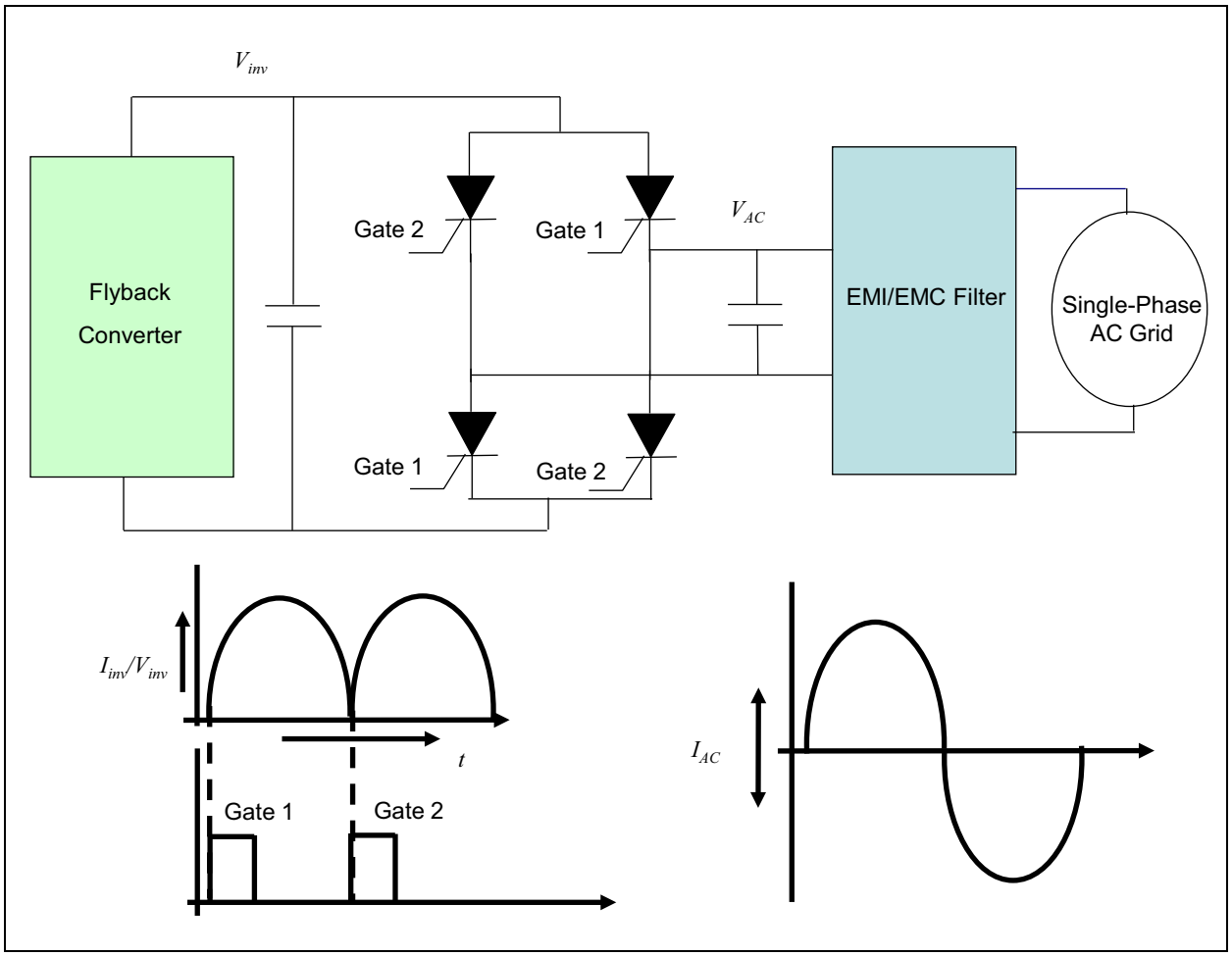


FIGURE 20: SCR BRIDGE I/O VOLTAGE/CURRENT WAVEFORM



The main specification of the grid-connected solar microinverter is that current must be drawn from the PV panel and delivered to the utility grid at unity power factor.

Consider the grid-connected microinverter of Figure 19 and Figure 20 where:

- V_{AC} is the fundamental component of the inverter output
- VL is the voltage drop across the link inductor (EMI inductor)
- V_{grid} is the utility grid voltage waveform

Assuming that the losses are negligible, it can be observed that $V_{AC} = V_{grid} + VL$, where all variables are vectors in the form of $v = V * e^{j*\varphi}$. Based on this, V_{AC} is then calculated, as shown in Equation 9.

EQUATION 9:

$$V_{AC} = V_{grid} + j \cdot \omega \cdot L \cdot I_{AC}$$

To achieve the unity Power Factor condition, the current waveform must be in phase from the utility voltage waveform. Figure 21 show how this waveform appears in vector form.

FIGURE 21: VECTOR WAVEFORM

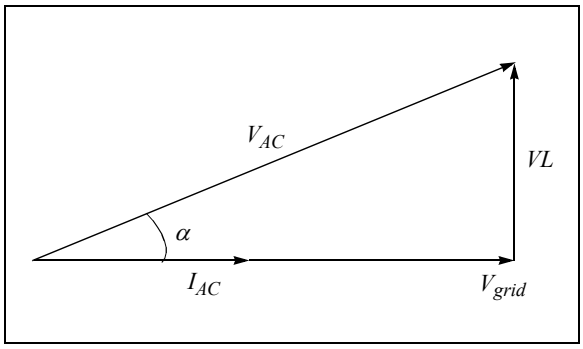
The key to controlling this operation is the inverter voltage variable, V_{AC}. From Equation 9, I_{AC} can be expressed, as shown in Equation 10.

EQUATION 10:

$$I_{AC} = \frac{V_{AC} - V_{grid}}{j \cdot \omega \cdot L}$$

Figure 22 shows I_{AC} when drawn as a phasor.

FIGURE 22: MAGNITUDE AND PHASE REQUIREMENT OF INVERTER OUTPUT VOLTAGE



The phasor in Figure 22 shows that the magnitude and direction of current flow (and therefore power flow), can be controlled by the phase shift α and the magnitude of the inverter output voltage waveform.

HARDWARE DESIGN

A flyback inverter needs to convert wide input PV panel voltage into rectified high-voltage AC. The instantaneous rectified output voltage should be greater than the instantaneous grid voltage to feed the sinusoidal current to infinite voltage source (i.e, the grid). The transformer turns ratio is utilized to boost the low DC voltage to high voltage. The design specifications used in the flyback inverter are as follows:

- Input voltage range: 25-45 V_{DC}
- Rectified output voltage peak range: 120-210V
- Continuous power: 190 watt
- Switching frequency: 172 kHz

The flyback converter should be able to boost the minimum available PV voltage (25 V_{DC}) to maximum peak grid voltage (210V). The converter is designed to operate at a maximum of 62% of the PWM duty cycle. The input and output voltage relationship on the flyback converter is expressed by Equation 11.

EQUATION 11:

$$V_{rectified} = \frac{V_{inmin} \cdot N \cdot Duty_{max}}{(1 - Duty_{max})}$$

Where,

$V_{rectified}$ = inverter output voltage

V_{inmin} = minimum input voltage

N = transformer turns ratio

$Duty_{max}$ = maximum duty cycle of the flyback MOSFET

For a V_{inmin} of 22 VDC and a $V_{rectified}$ of 210V with a maximum duty cycle of 0.62, the turns ratio of the transformer should be N ≈ 6.

Flyback MOSFET

When choosing the MOSFETs, the following must be considered:

- Maximum Breakdown Voltage
- Continuous Current
- Peak Current
- Package Thermal Performance

Maximum Breakdown Voltage

In Flyback configuration the maximum voltage applied across the MOSFET is expressed by Equation 12.

EQUATION 12:

$$V_{ds} = V_{in} + V_{reflected} + V_{leakage}$$

Where,

V_{ds} = voltage applied across the drain and source of the MOSFET

V_{in} = input voltage of 25-45 VDC

$V_{reflected}$ = output reflected voltage applied across the transformer primary when the output diode turns ON

$V_{leakage}$ = leakage spike voltage due to transformer leakage magnetizing inductance

The maximum output voltage will be equal to the peak of the maximum grid voltage, which is 210V. The maximum reflected voltage at the peak of maximum grid voltage is expressed by Equation 13.

EQUATION 13:

$$V_{reflected} = \frac{210}{6} = 35$$

Leakage voltage depends on leakage inductance of the transformer. The expected leakage voltage spike is 30V to 35V at full load condition. Therefore, the drain-to-source voltage across the MOSFET at V_{inmax} = 55V and maximum grid voltage is calculated, as shown in Equation 14.

EQUATION 14:

$$V_{ds} = 55 + 35 + 35 = 125V$$

Continuous Current

The MOSFETs should be able to handle maximum continuous and peak current during extreme conditions. As the flyback MOSFET duty is sine modulated its current will be sine profile. At V_{inmin}, the maximum input average current will be 9 amps. The maximum input current will be 9/$Duty_{max}$, which equals 14.5 amps. Therefore, the peak of the sine modulated input current will be 14.5 * 1.414 = 20.53 Amps. As input current rises linearly when the MOSFET turns ON, the MOSFET current will have peak-to-peak ripple current on top of its peak current. The maximum peak-to-peak current is chosen 20% of the input peak current. Therefore, the peak current across the MOSFET is expressed by Equation 15.

EQUATION 15:

$$I_{peakmax} = 20.53 + 20.53 \cdot \frac{0.2}{2}$$

In the interleaved flyback converter this current will be divided into two MOSFETs. Therefore, each MOSFET will have maximum peak current of ~11.5 Amps.

Package Thermal Performance

A MOSFET should be selected with low Rds(on) to reduce the conduction losses in the MOSFET. a MOSFET with an Rds(on) less then 20 mOHM is a good choice. The gate switching losses depend on the total gate charge of the MOSFET. Therefore, the MOSFET should have less then 100 nC for 172 kHz switching. Based on the above parameter, the IRFS4321 has been selected. The IRFS4321 has a maximum of 15 mOHM Rds(on) and 110 nC maximum total gate charge.

Flyback Transformer

The flyback transformer has been designed using a ferrite transformer. The transformer design is based on using the area product (W_aA_c) approach and is designed to meet the following conditions:

- Minimum input voltage: V_{imin} = 22V
- Maximum DC link voltage: V_o = 210V
- Maximum output power: P_{omax} = 200W
- Primary rms current: IP_{rms} = 10A
- Maximum duty cycle: D_{max} = 0.62
- Switching frequency: f = 172 kHz

The manufacturer's data sheet was used to help select the appropriate material for the desired application. For the given range of materials, frequency, core loss, and maximum flux density of the material should be considered. From the research data, 3C90 material from FERROXCUBE was selected. From core loss, maximum flux density can be calculated, as shown in Equation 16. The factors used in this equation are provided in Table 2.

EQUATION 16:

$$P_l = a \cdot f^c \cdot B_{max}^d$$

TABLE 2: FACTORS APPLIED TO THE CORE LOSS EQUATION

Material	Frequency (f)	a	c	d
R, 35G, N87, 3C90	f <100 kHz	0.074	1.43	2.85
	100 kHz ≤ f < 500 kHz	0.036	1.64	2.68
	f ≥ 500 kHz	0.014	1.84	2.28
P, 45G, N72, 3C85	f < 100 kHz	0.158	1.36	2.86
	100 kHz ≤ f < 500 kHz	0.0434	1.63	2.62
	f ≥ 500 kHz	7.36e-7	3.47	2.54
F, 25G, N41, 3C81	f < 10 kHz	0.790	1.06	2.85
	10 kHz ≤ f < 100 kHz	0.0717	1.72	2.66
	100 kHz ≤ f < 500 kHz	0.0573	1.66	2.68
	f ≥ 500 kHz	0.0126	1.88	2.29

Core loss density is normally selected at approximately 250 mW/cm^3. The calculated maximum flux density must be limited to less than half of b at saturation. This b level is chosen because the core will develop excessive temperature rise at this frequency when a flux density is close to saturation. Maximum flux density can now be calculated by Equation 17.

EQUATION 17:

$$B_{max} = \left(\frac{P_l}{a \cdot \left(\frac{f}{1000} \right)^c} \right)^{\frac{1}{d}} = \left(\frac{150}{0.036 \cdot \left(\frac{172000}{1000} \right)^{1.64}} \right)^{\frac{1}{2.68}} = 960G$$

To select the right size of the core, the area product of the core must be calculated using Equation 18. This equation is derived from the equation for flux linkage ($\psi = N * \phi$) and represents the power handling ability of the core. Therefore, each core has a number that is a product of its window area, W_a, and core cross-section area, A_c.

EQUATION 18:

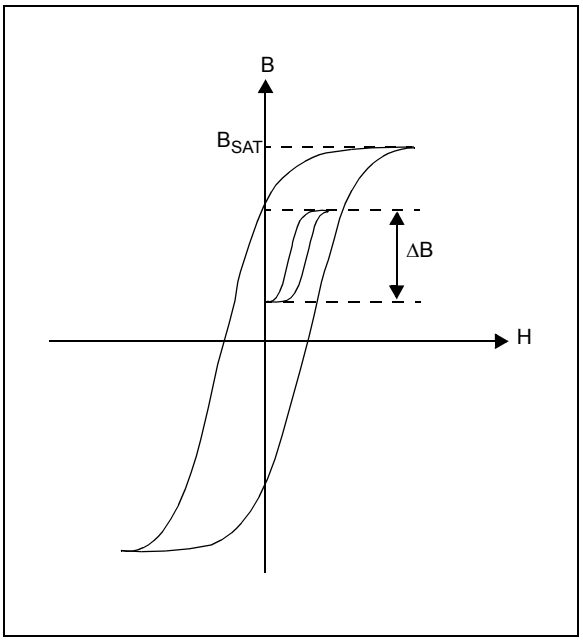
$$W_a A_c = \frac{10^8 \cdot P_{omax}}{K_t \cdot \Delta B \cdot f \cdot J}$$

ΔB in Equation 18 is equal to B_{max} core excitation as seen in Figure 23. Current density of a winding is estimated to be 400 A/cm^2 and maximum output power P_{omax} is 190W. Therefore, the calculated area product can be determined using Equation 19.

EQUATION 19:

$$W_a A_c = \frac{10^8 \cdot 195}{0.254 \cdot 960 \cdot 172000 \cdot 400} = 1.16cm^4$$

FIGURE 23: HYSTERESIS LOOP OF MAGNETIC CORE



The selected core must have area product larger than calculated. Next, the RM14 shape and size of a core was selected. A size larger than needed was selected due to the primary and secondary windings that fit to the winding area of that core.

The primary turns are calculated using Equation 20.

EQUATION 20:

$$N_p = \frac{10^8 \cdot V_{inmin} \cdot \left(\frac{1}{f} \right) \cdot D_{max}}{\Delta B \cdot A_c} = \frac{10^8 \cdot 22 \cdot \left(\frac{1}{172000} \right) \cdot 0.62}{960 \cdot 1.68} = 5$$

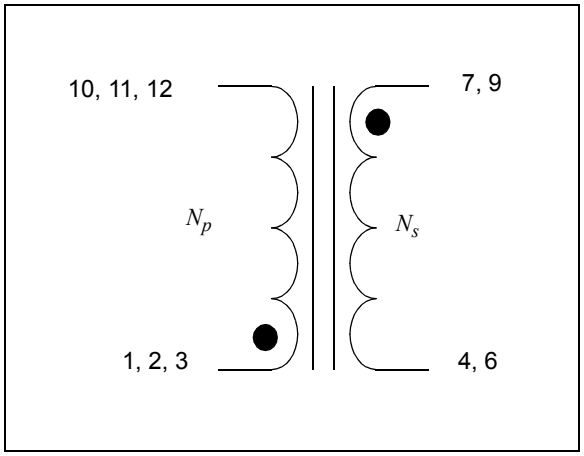
To maintain the design margin we have chosen the number of primary turns = 6, with the secondary number of turns, N_s, expressed by Equation 21.

EQUATION 21:

$$N_s = N_p \cdot N = 6 \cdot 6 = 36$$

As primary current is very high, copper foil is used to reduce copper loss. In addition, to have 4 kV isolation from primary to secondary, triple insulated wire is used for the secondary winding. The winding diagram of the transformer is shown in Figure 24.

FIGURE 24: TRANSFORMER ELECTRICAL AND MECHANICAL CONSTRUCTION



Output Rectifier Diode

A power diode requires a finite time to change from the blocking state to the conduction state and vice versa. The time required to change its state, and how the diode current and voltage change during the transition period affects the operation of circuitry. The shape of the waveform (voltage and current) and transition time depends on diode intrinsic properties. When selecting diodes the following should be considered:

- **Diode Breakdown Voltage**

  Transformer secondary voltage is calculated with $V_s = V_{inmax} * N_s/N_p$, at highest PV module voltage V_s = 55 * 6 = 330V, and maximum peak grid voltage V_s = 145 * 1.414 = 250V. Therefore, the maximum voltage applied across the output rectifier diode will be V_{br} = 330 + 205 = 535V, because of transformer leakage inductance, and diode internal inductance voltage spikes that appear on diodes when switching. Due to this, the calculated breakdown voltage is increased by 30% and should be more than 700V.

- Average Forward Current

  Average forward current per leg is easily calculated by Equation 22 from maximum output current at minimum gird voltage and continuous output power.

EQUATION 22:

$$I_{avg} = \frac{2 \cdot \sqrt{2} \cdot P_{output}}{\Pi \cdot V_{gridmin}} = \frac{537}{282} = 1.90$$

- Peak Forward Current

  Peak current is calculated in Equation 23 using the transformer current ratio and peak MOSFET current.

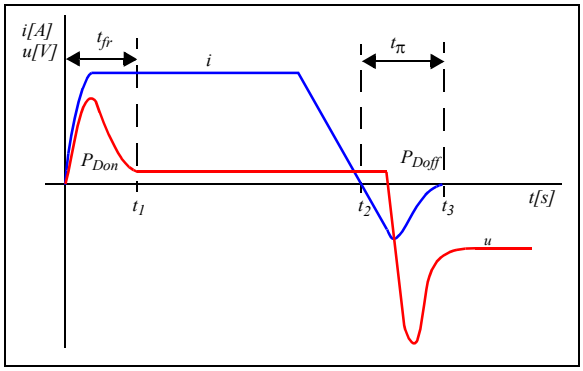
EQUATION 23:

$$I_{pD} = I_P \cdot \frac{N_1}{N_2} = 11.5 \cdot 0.167 = 1.9167$$

- Switching Characteristics

  Diode switching characteristics (see Figure 25) are determined by forward recovery time and reverse recovery time.

FIGURE 25: DIODE SWITCHING CHARACTERISTICS



The diode switching loss can be estimated using Equation 24.

EQUATION 24:

$$P_{swD} = Q_c \cdot V_{DC} \cdot f_{SW}$$

- Package Thermal Performance

  For diodes, the isolated TO-220-2 package is used. Continuous working junction temperature should not exceed 130°C. Typical thermal junction to heat sink resistance of junction isolated TO-220-2 package is $R_{\Theta t}$ = 3.5°C/W for maximum allowed power dissipation.

  Total power loss in both diodes is estimated by adding conduction losses and switching losses, as expressed by Equation 25.

EQUATION 25:

$$P_{tot} = P_{swD} + P_{fD} = 2W$$

The estimation shows that the power losses are within the set criteria.

Full-Bridge Thyristor

A thyristor is used in the full-bridge configuration to convert the inverter output voltage/current (rectified) to sinusoidal voltage/current. The maximum grid voltage of the SCR will be equal to the maximum grid voltage peak. Also, the average and peak current across the SCR will be equal to the grid current. The S8016N thyristor from Tecco Electronics was selected.

AUXILIARY POWER SUPPLY DESIGN

Design Specifications

The auxiliary power supply provides power, which is taken from the PV module input, to all of the on-board electronics.

The design specifications are:

- Input voltage: 15V-60V
- Output: 150 mA @ 3.3V, 200 mA @ 5V, 400 mA @ 12V

Because of a wide range of input voltage and power losses, a buck converter was used to generate 12V from the battery voltage. For 3.3V and 5V, linear regulators are used because of simplicity and price. All of the voltage regulators are connected in series; therefore, the 12V buck converter needs to deliver maximum 1A of current. For the buck converter, the LM5007 from National Semiconductor was used.

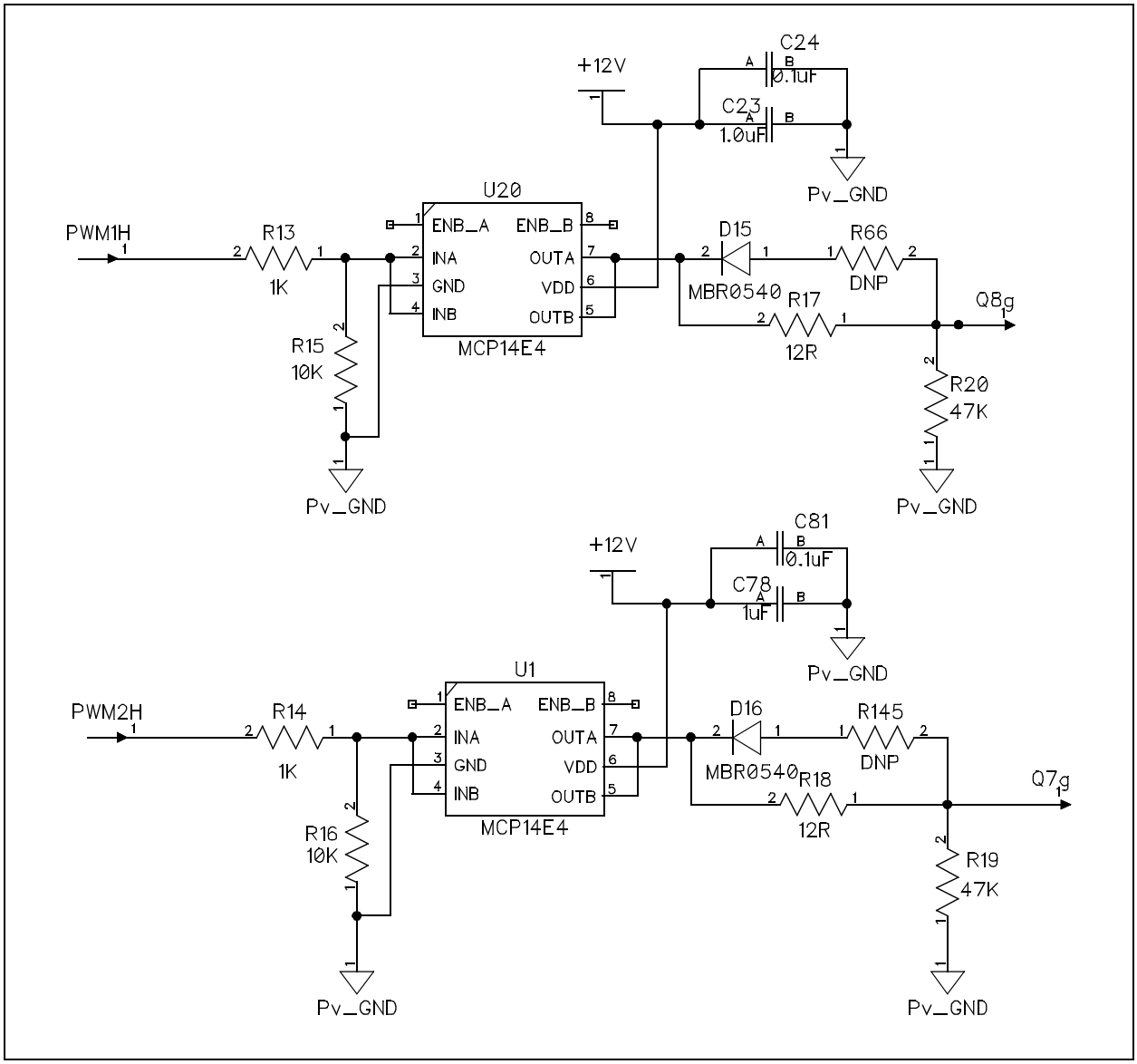
Signal Adaptation Block

The signal adaptation block consists of all of the electric circuitry (active and passive), which interfaces the dsPIC DSC to the power electronics circuitry, such as MOSFET gate signals**,** analog currents and voltages sense, filters, and voltage dividers.

Flyback MOSFET Gate Drive Signal

The Microchip driver, MCP14E4, drives the flyback MOSFET gate signals: Q7G and Q8G (see Figure 26). PWM1H and PWM2H are the PWM output ports of the dsPIC DSC device. A reverse diode is used across the gate drive resistor for fast MOSFET turn-off to reduce the turn-off switching loses.

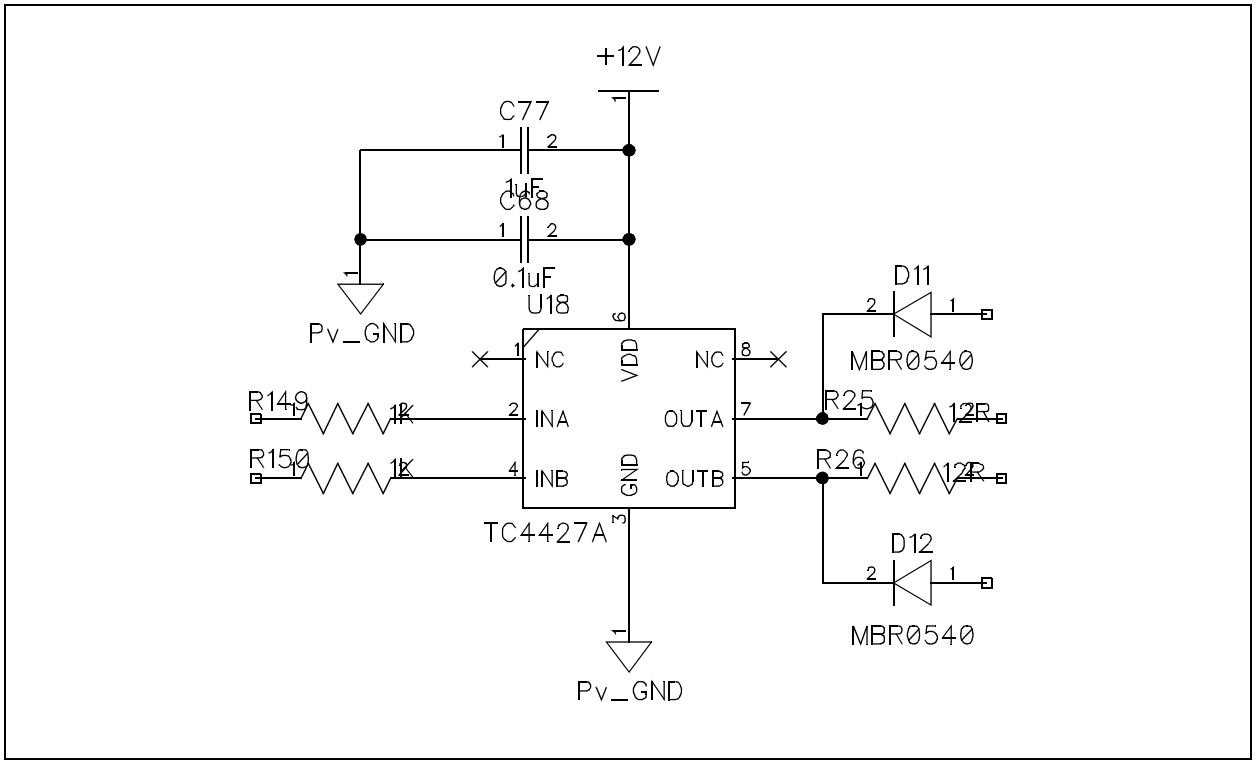
FIGURE 26: FLYBACK MOSFET GATE DRIVE



Active Clamp MOSFET Gate Drive Signal

The Microchip driver, TC4427, drives the active clamp MOSFETs gate signals: Q1G and Q2G (see Figure 27). PWM1L and PWM2L are the PWM output ports of the dsPIC DSC device. A reverse diode is used across the gate drive resistor for fast MOSFET turn-off to reduce the turn-off switching loses.

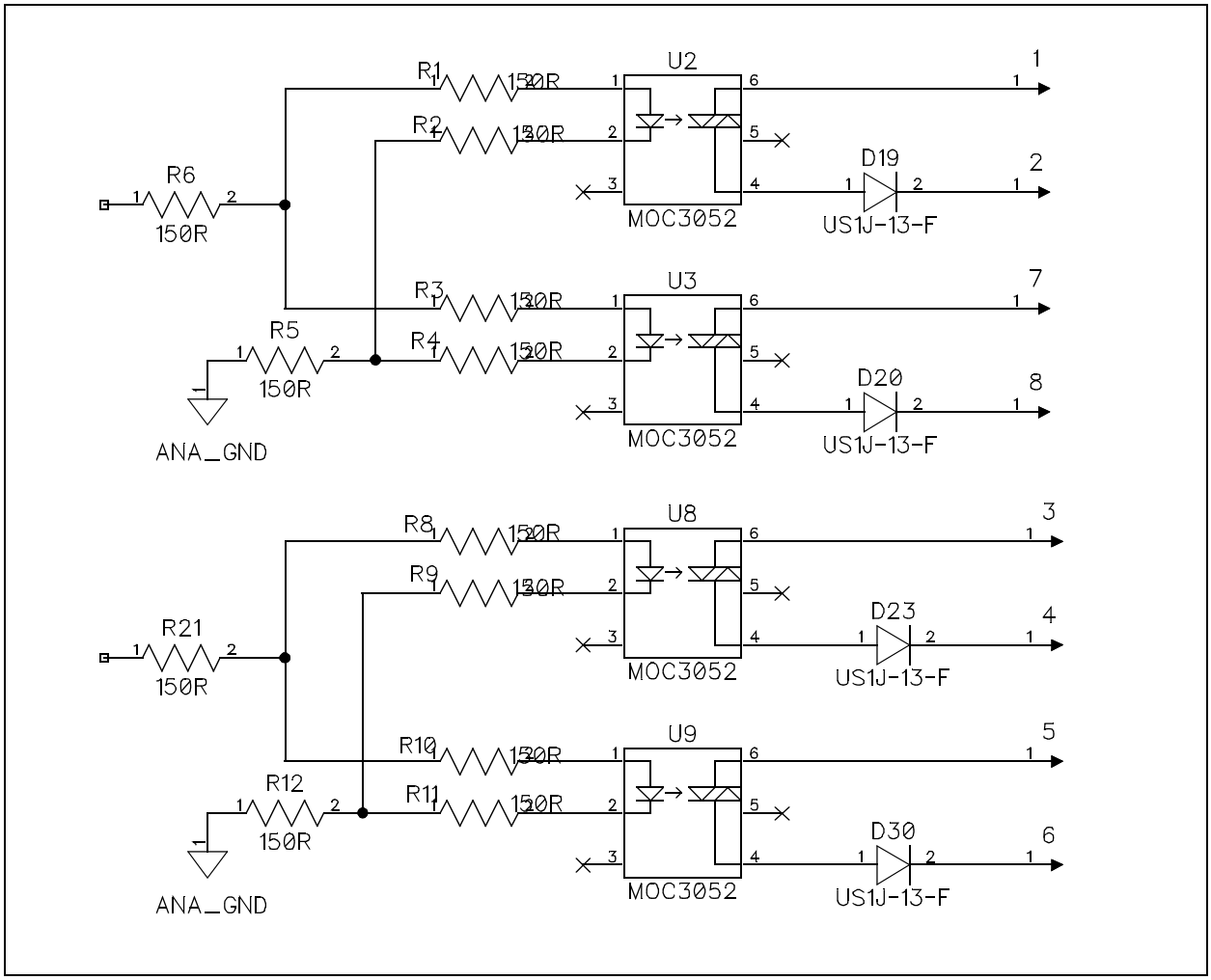
FIGURE 27: FLYBACK ACTIVE CLAMPED MOSFET GATE DRIVE



SCR Gate Drive Signal

The MOC3052 opto-coupler-based gate driver drives the SCR bridge diodes D3, D4, D5 and D6. The MOC3052 SCR driver drives the high-side as well as the low-side SCR with opto-isolation of the gate drive signal (see Figure 28). PWM3H and PWM3L are the PWM output ports of the dsPIC DSC device.

FIGURE 28: SCR GATE DRIVE



Current Measurement Techniques

- Hall Effect-based Linear Current Sensor IC
- Current Transformer (CT) Measurement

HALL EFFECT-BASED LINEAR CURRENT SENSOR IC

This method measures the inverter output current flowing into the grid. In this method, the current sensor IC is connected between the inverter output and the grid in one line.

A Hall effect-based linear current sensor from Allegro can measure current with 80 kHz bandwidth. It provides 2.1 kV isolation between the primary and the secondary. The output sensitivity of the selected current sensor is 180 mV/A. The output voltage of the current sensor is very small with an offset of 2.5V.

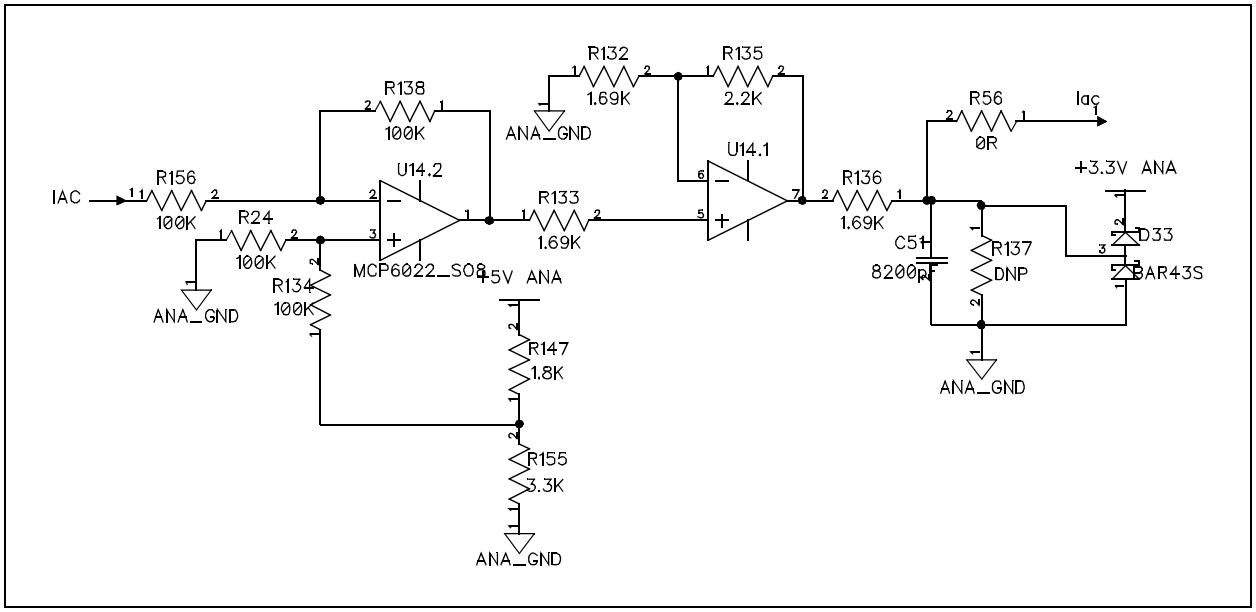
To optimize the available analog voltage range of dsPIC DSC, an offset of 3.235V is added to the output of the current sensor and then amplified by a non-inverting amplifier.

The current signal at the ADC pin of the dsPIC DSC will have an offset of 1.65V; therefore, it can effectively utilize the available analog voltage range for measurement.

Output of the current sensor is fed to the inverting pin of the Op amp, U14.2, and offset voltage is fed to the non-inverting pin of Op amp U14.2 Op amp U14.2 is used as a unity gain differential amplifier. The output of Op amp U14.2 is amplified by a non-inverting amplifier and is fed to the analog channel of the ADC.

The schematic is built around Microchip's MCP6022 rail-to-rail input/output Op amp, as shown in Figure 29, where I_{AC} designates the inverter output current fed to the grid.

FIGURE 29: AC CURRENT SENSE CIRCUIT

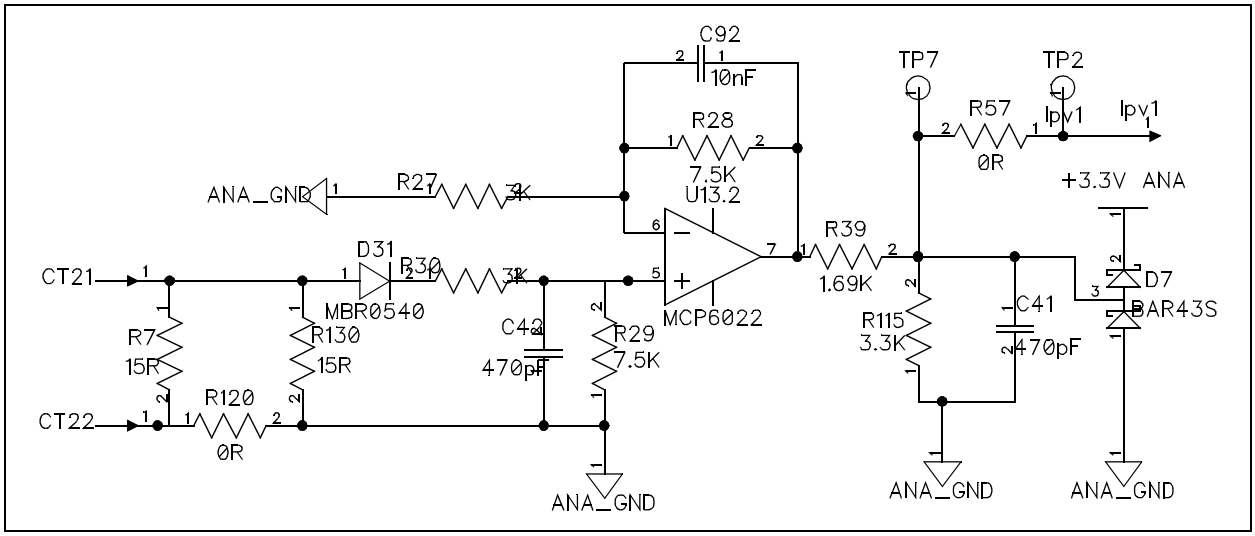


CURRENT TRANSFORMER (CT) MEASUREMENT

The CT measurement method uses a current transformer (CT) to measure the current. It is mounted at the lower side of the switching leg, between the MOSFET transistors and ground (see Figure 30). This method offers certain advantages, such as galvanic isolation and cost reduction. The CT measurement method is used to sense flyback MOSFET currents. Figure 30 shows the simplified schematic of the current measurement method.

The current, I_{pv1}, denotes the current flowing through one of the flyback converter MOSFET legs. The selection of the CT depends on the number of turns (N) of the secondary of the transformer and the external current sense resistor (RT) known as burden resistor. The parameters N and RT are chosen to minimize the resistive for sensing the current. Voltage across the burden resistor is then amplified enough to utilize the maximum dsPIC DSC voltage range of 0V to 3.3V.

FIGURE 30: CURRENT MEASUREMENT



Voltage Measurement Techniques

- Resistive Divisor Voltage Measurement
- Differential Amplifier With Voltage Offset
- Zero-crossing Detect Circuit

RESISTIVE DIVISOR VOLTAGE MEASUREMENT

The PV panel voltage required for the control algorithm is scaled using the voltage divisor shown in Figure 31.

The resistive divisor formed by R123 and R124 scales down the PV panel voltage to the ADC input voltage level, which is in the range of 0V to 3.3V.

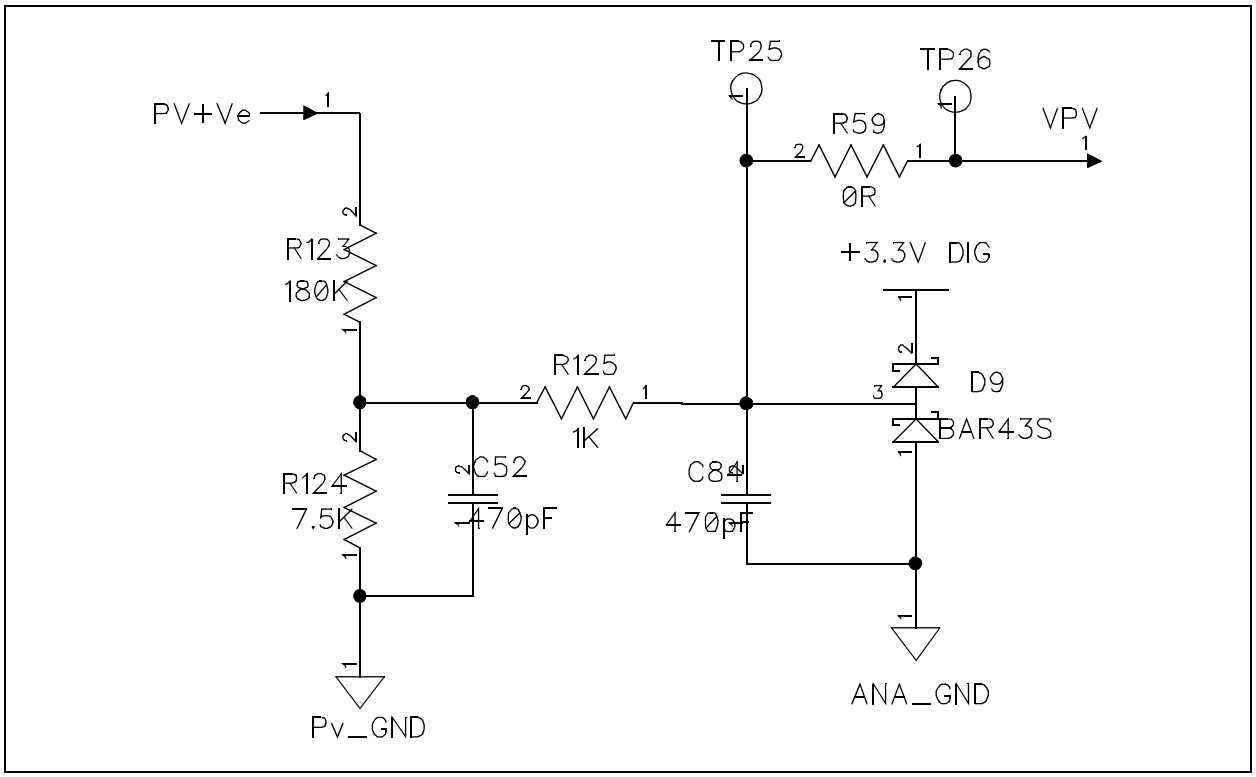
Equation 26 computes the gain of the voltage division.

EQUATION 26:

$$V_{ADC} = V_{PV} \cdot \frac{R124}{(R124 + R123)}$$

The capacitors, C52 and C84, are used for the signal filtering, but their presence in the circuit is not mandatory. Similarly, the presence of the diode D9 is not mandatory. This diode provides protection if the voltage provided to an analog pin of the dsPIC DSC exceeds 3.3V.

FIGURE 31: VOLTAGE DIVISOR

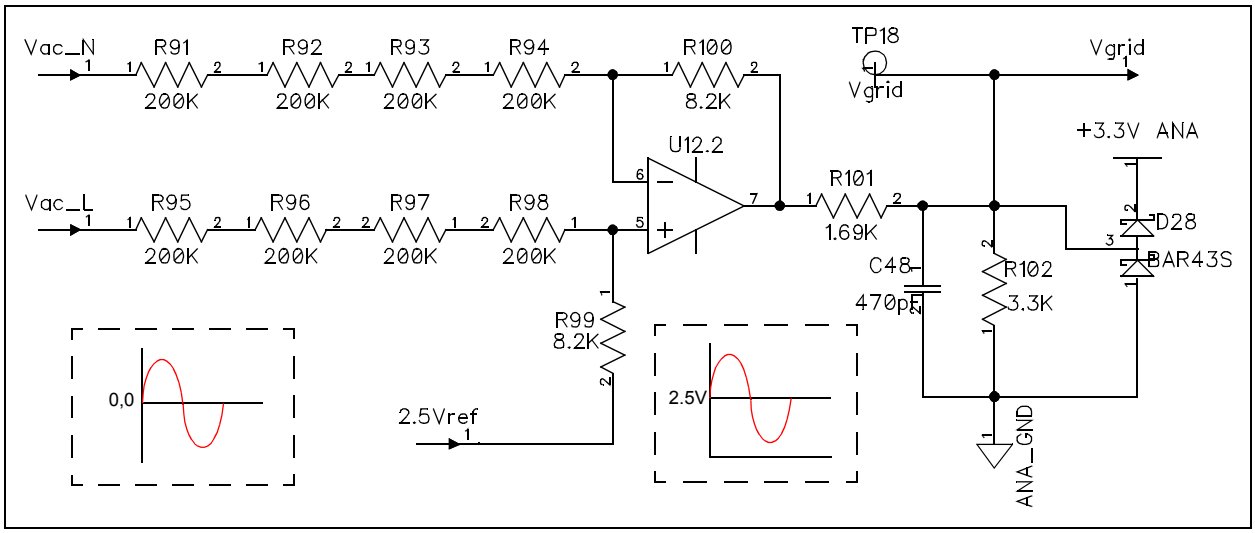


DIFFERENTIAL AMPLIFIER WITH VOLTAGE OFFSET

The inverter output voltage and grid voltage are AC in nature, and cannot sense through a resistive divider network, because the ADC module of the dsPIC DSC can only measure a voltage signal range from 0V to 3.3V. High-voltage AC signals are deamplified and a 2.5V offset is added using a differential amplifier as shown in Figure 32.

An offset of 2.5V makes the bidirectional AC sense voltage centered around this DC offset voltage. The resistor divider makes sure that the sense signal voltage varies from 0 to 3.3V with an offset of 1.65V at the analog pin of the dsPIC DSC, to effectively utilize the available voltage range of the ADC.

FIGURE 32: AC VOLTAGE SENSE



ZERO-CROSSING DETECT CIRCUIT

Inverter output should be in phase and in the same frequency as the grid voltage to feed current with a high power factor. Zero cross detect circuitry detects the grid voltage state and changes the dsPIC DSC port (Port B15) state accordingly.

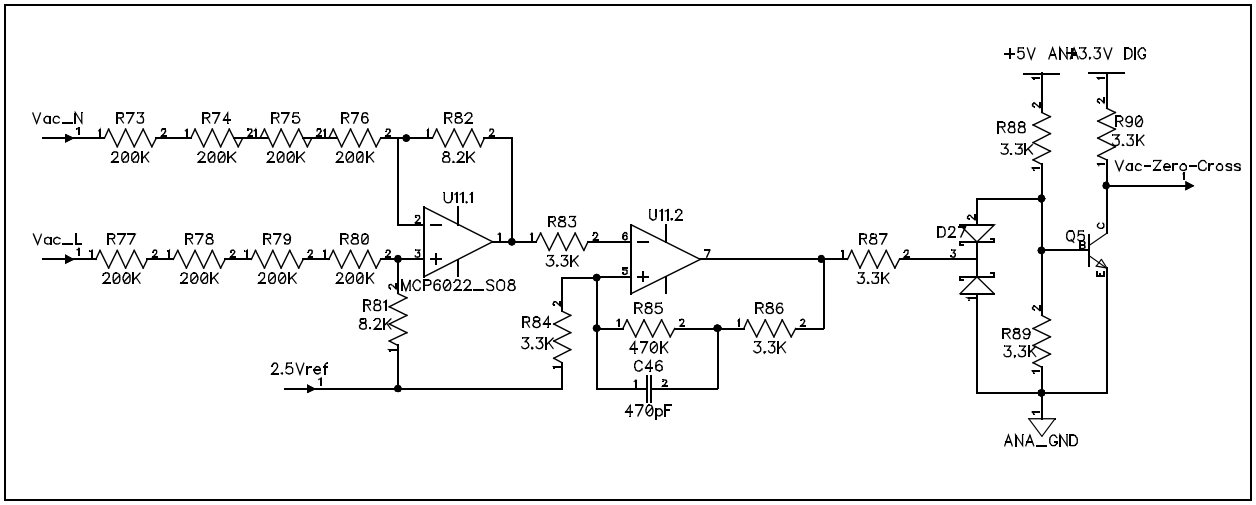
As the grid voltage state changes from negative to positive, it changes the state of PORTB15 from low-to-high and vice-versa.

High voltage AC signals (grid voltage) are deamplified and an offset of 2.5V is added using the differential amplifier U11.1. The output of the differential amplifier U11.1 is compared with the 2.5V reference by comparator U11.2. The comparator U11.2 output drives the transistor Q5 base, as shown in Figure 33.

To avoid false triggering of the comparator, a hysteresis band of ~10 mV is added

using R85, R86 and C46.

FIGURE 33: ZERO-CROSSING DETECT



SOFTWARE DESIGN

The Grid-Connected Solar Microinverter Reference Design is controlled by a single dsPIC DSC device, as shown in the system block diagram in Figure 34.

The dsPIC DSC device is the heart of the Solar Microinverter design and controls all critical operations of the system as well as the housekeeping operations. The functions of the dsPIC DSC can be broadly classified into the following categories:

- All power conversion algorithms
- Inverter state machine for the different modes of operation
- Maximum Power Point Tracking (MPPT)
- Digital Phase-Locked Loop (PLL)
- System islanding and Fault handling

The dsPIC DSC device offers intelligent power peripherals specifically designed for power conversion applications. These intelligent power peripherals include the High-Speed PWM, High-Speed 10-bit ADC, and High-Speed Analog Comparator modules. These peripheral modules include features that ease the control of any Switch Mode Power Supply with a high-resolution PWM, flexible ADC triggering, and comparator Fault handling. In addition to the intelligent power peripherals, the dsPIC DSC also provides built-in peripherals for digital communications including I^2C™, SPI and UART modules that can be used for power management and housekeeping functions.

A high-level diagram of the solar microinverter software structure is shown in Figure 35. As shown in this figure, the software is broadly partitioned into two parts:

- Solar Microinverter State Machine (includes power conversion routines)
- User Interface Software

FIGURE 34: GRID-CONNECTED SOLAR MICROINVERTER BLOCK DIAGRAM

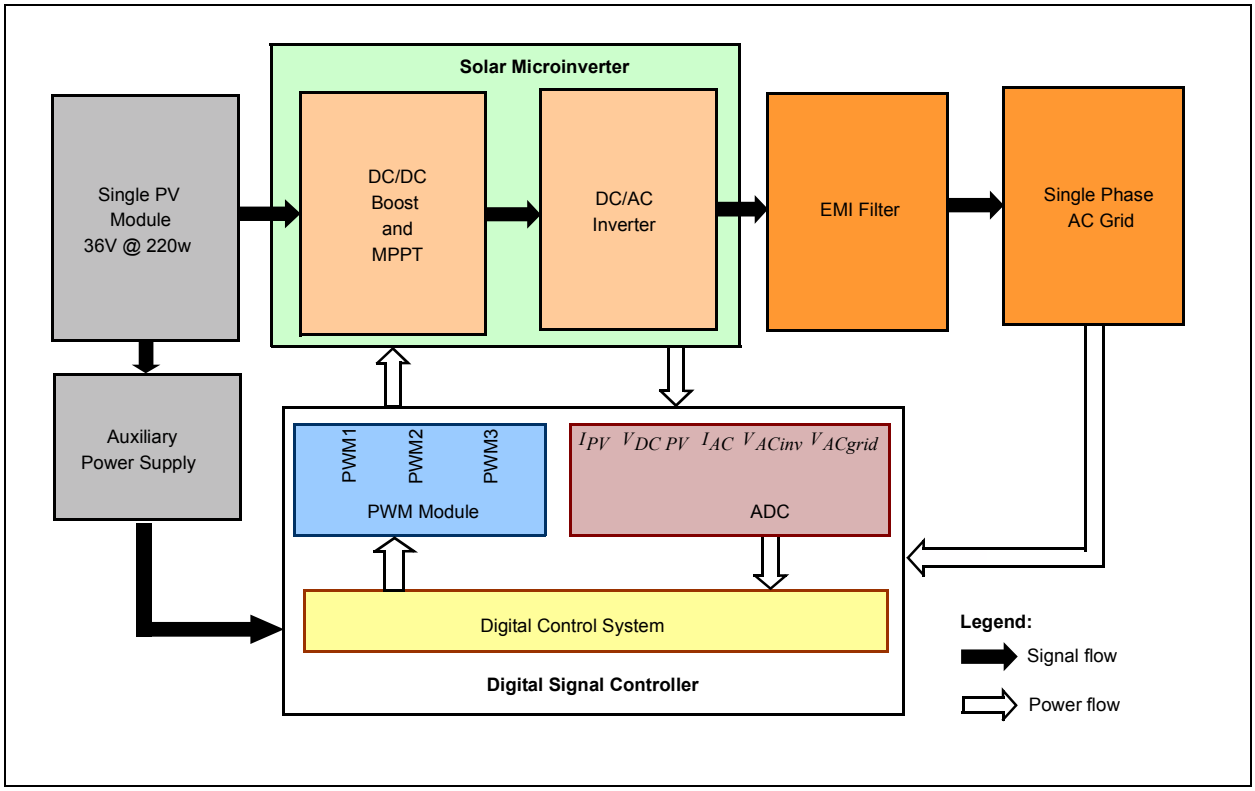
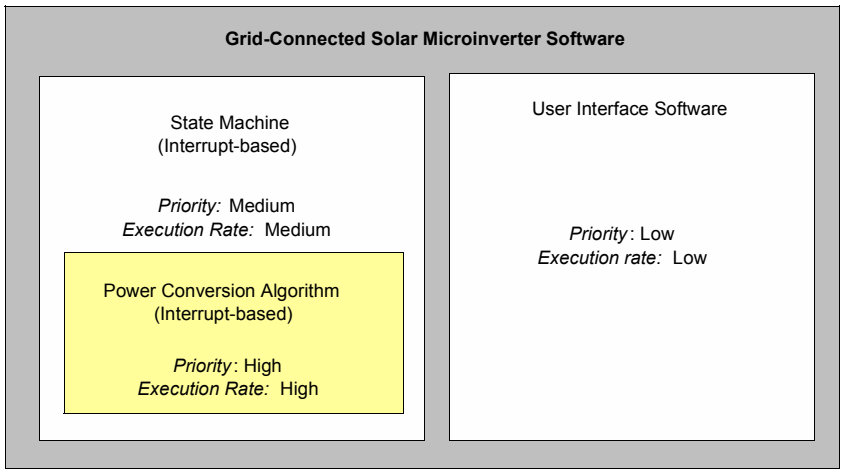


FIGURE 35: GRID-CONNECTED SOLAR MICROINVERTER SOFTWARE: HIGH-LEVEL PARTITIONS



The grid-connected solar microinverter software implements a state machine to determine the mode of operation for the system. The state machine is executed once every 100 µs inside a timer Interrupt Service Routine (ISR). The state machine configures the on-chip peripherals to execute the correct power conversion algorithms.

When the system first turns ON, it checks for all the input and output condition and Faults. If the input and output are within the specified range and there is no Fault, the system state machine switches the system to Start-up mode. It checks the system condition again at Start-up mode and initializes all the necessary variables and peripherals for normal mode operation and then switches to DAY_MODE operation. If the grid fails, the state machine switches the state of the system to the SYSTEM_ERROR mode operation and if the grid is healthy, but the PV panel voltage is not within the specified limit, the state machine switches the system to the NIGHT_MODE of operation.

System Initialization

When the solar microinverter is turned ON, the system goes into initialization routing and initializes all its peripherals, variables and constants. The state of the system will initialize with the system start-up state. The state machine first monitors all system variables and the input and output state. If any Faults are detected, it checks for:

- Grid voltage condition
- Grid frequency condition
- Inverter output AC current condition
- PV panel voltage condition
- Flyback MOSFET current condition

Modes of Operation

Each mode of operation for the reference design is described in the following sections.

Figure 36 shows the state diagram for the reference design.

SYSTEM_STARTUP

If any of the conditions previously described are not within the specified limit, the state machine will switch the system state to the SYSTEM_ERROR mode of operation.

If all conditions are within the specified limits, the state machine will first calculate the input PV voltage and the output grid voltage and its frequency before setting `systemStartFlag` to start the system in normal operation. It reinitializes all of the mandatory control loop variables to ensure reliable operation during initial switching of the PWMs. After initializing all mandatory control loop variables, the system state switches to DAY_MODE operation. During SYSTEM_STARTUP mode operation, the system continuously checks for all the conditions specified. If any of the these conditions fails it switches to the SYSTEM_ERROR mode of operation.

DAY_MODE

DAY_MODE is the normal mode of operation. During normal operation of the solar inverter, the state machine configures the system peripherals to execute the correct power conversion algorithms as determined by the system state. In this mode, the solar microinverter delivers the maximum available energy from the PV panel to the single-phase grid. The ADC peripheral of the device is triggered by the PWM to sample all of the analog feedback signals. The PLL generates sine current reference in phase and synchronizes with the grid voltage. The MPPT control loop calculates the magnitude of the current output current reference to

make sure the inverter system is feeding the maximum available energy from the PV module. If any of these condition are not met, the system state machine switches to the SYSTEM_ERROR state.

NIGHT_MODE

The system state switches NIGHT_MODE when there is not sufficient energy available from the connected PV panel (power <25W) or the PV panel voltage is not within the specified limit. In this mode of operation, the system stops feeding any energy to the grid and turns OFF all of the PWM switching and switches the ADC triggering option from PWM to Timer1, keeping the ADC trigger rate the same as it was in DAY_MODE operation. Therefore, all feedback signals are being continuously monitored and checked for all of the previously mentioned input and output conditions and faults in the system. The system switches to the SYSTEM_ERROR mode of operation, if there are any faults or the grid voltage moves away from the specified limit.

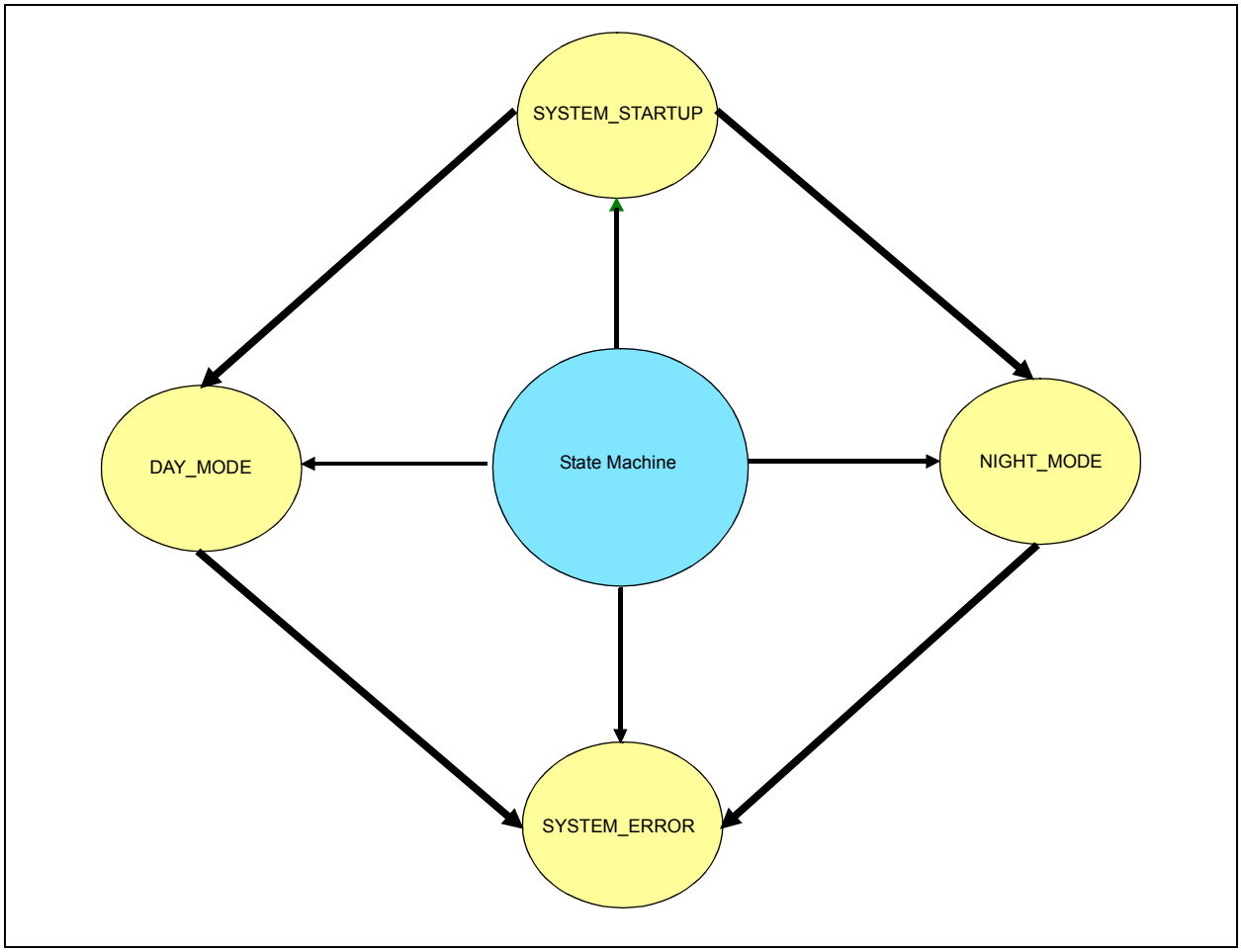
SYSTEM_ERROR

The system state switches to SYSTEM_ERROR mode if any of the following conditions occur:

- Grid undervoltage < ~90 V_{AC}
- Grid overvoltage > ~ 140 V_{AC}
- Grid frequency > 65 Hz or < 55 Hz
- Flyback MOSFET overcurrent
- Inverter output current peak > 3A

As soon as the system switches to the SYSTEM_ERROR state, it once again checks the conditions described previously to avoid any false SYSTEM_ERROR triggering. Once the system confirms that the error is true, it goes in safe operation mode. It then stops the PWM module and changes the ADC trigger source to Timer1. During the SYSTEM_ERROR mode of operation, the system state continuously checks the input and output voltage condition. If faults are removed, and the PV panel grid voltage, and grid voltage frequency are under the specified limit, the system switches to SYSTEM_STARTUP mode of operation to reliably turn the solar inverter ON and start feeding the available energy to grid.

FIGURE 36: STATE MACHINE BLOCK DIAGRAM



SINGLE-STAGE SINGLE CONVERTER LIMITATIONS

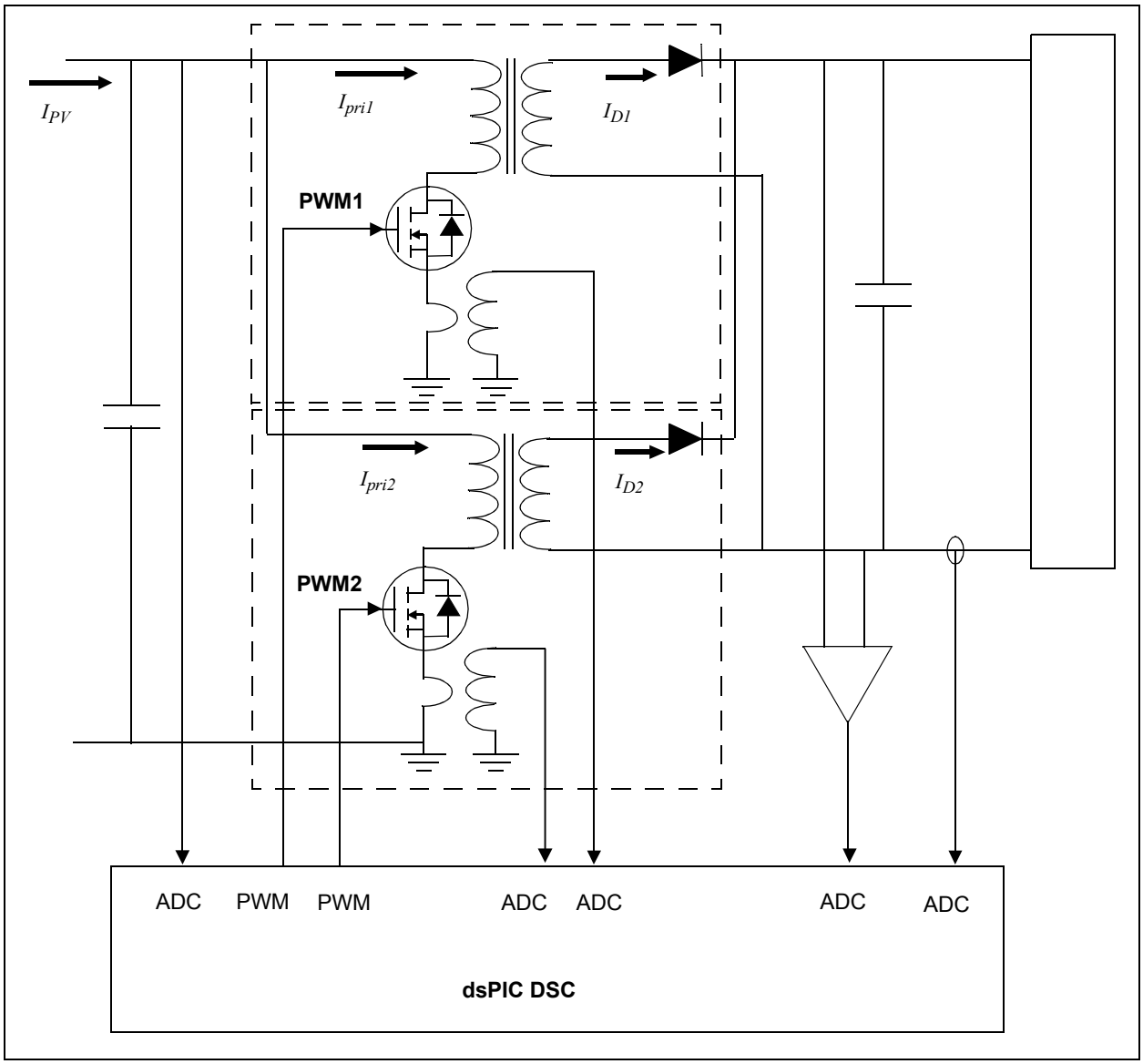
The following are the limitations of a single-stage single converter design when compared to a single-stage interleaved converter:

- Current ripple cancellation is not possible, thus a bigger input and output capacitor is required
- Large magnetics core
- Higher current rating of semiconductor devices

The interleaved converter can overcome these limitations. It contains two flyback converters, which are parallel coupled and are 180º out of phase with respect to each other, as shown in Figure 37.

At the input side, the total input current drawn from the PV panel equals the sum of the two Flyback MOSFET currents (I_{pv1} and I_{pv2}). Because the ripple currents through the two flyBack transformers/MOSFETs are out of phase, they cancel each other and reduce the total ripple current in the input side. At a duty cycle of 50%, the best cancellation of ripple currents is possible. At the output side, current through the output capacitor (IC) equals the sum of the two diode currents (I_{D1} and I_{D2}) minus the output current (I_{load}), as shown previously in Figure 16.

FIGURE 37: INTERLEAVED FLYBACK CIRCUITRY

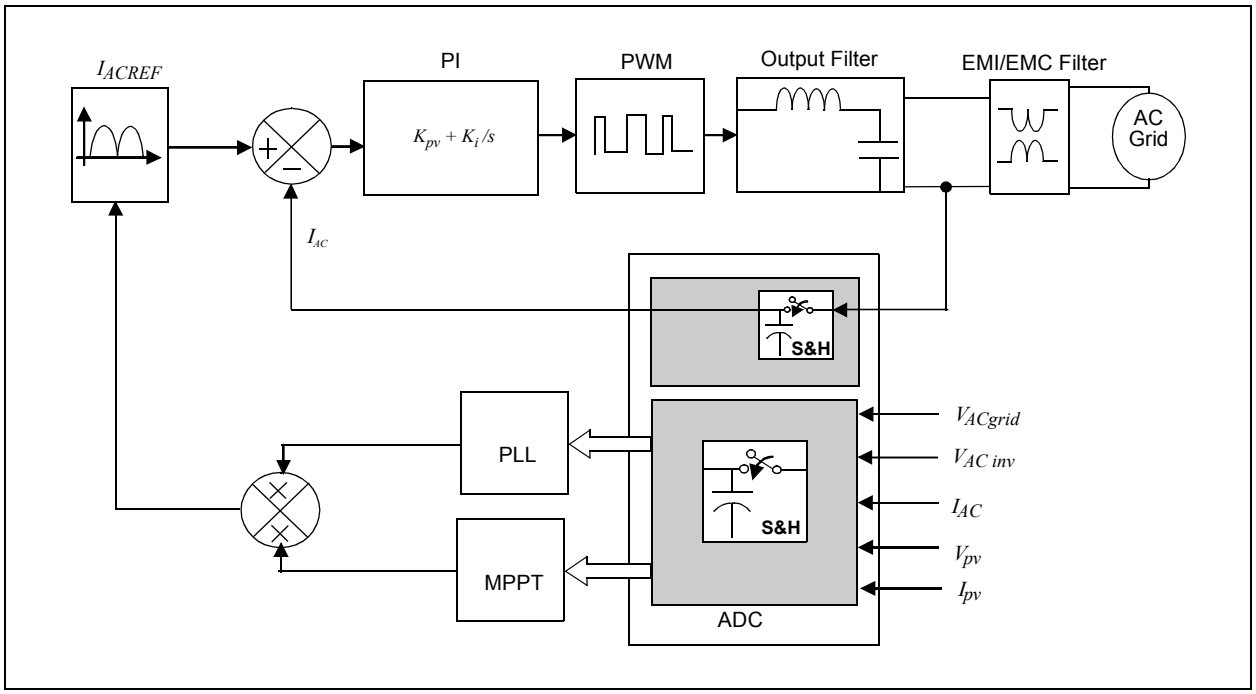


The solar microinverter system uses the average current mode control method to meet the system requirements. For the grid-connected microinverter system, this control method is used to generate sinusoidal output current. The control method operates in Continuous Conduction mode for most of the operating points of the converter. The operation is primarily based on the value of the load current at any point and the selection of magnetizing inductor of the flyback transformer. The various advantages offered by the average current mode control over other methods include:

- Suitable for operation at higher power levels
- Less ripple current in the flyback transformer, thus it's a MOSFET
- Reduces EMI filter requirements
- Less rms current will be seen by the transformer primary, thus it's a MOSFET
- Continuous Conduction mode operation is possible

To generate the sinusoidal shape for the output voltage/current, sinusoidal pattern is generated in software. The control system controls the subscribe ON time of the flyback MOSFET in order to generate the necessary shape of the output voltage/current. Figure 38 shows the block diagram of the digital average current mode control scheme.

FIGURE 38: CONTROL LOOP BLOCK DIAGRAM



Control Loops

The grid-connected solar microinverter control system includes the following control loops:

- Digital Phase-Locked Loop (PLL)
- MPPT Loop
- Current Control Loop
- Load Balance Control Loop

Digital Phase-Locked Loop (PLL)

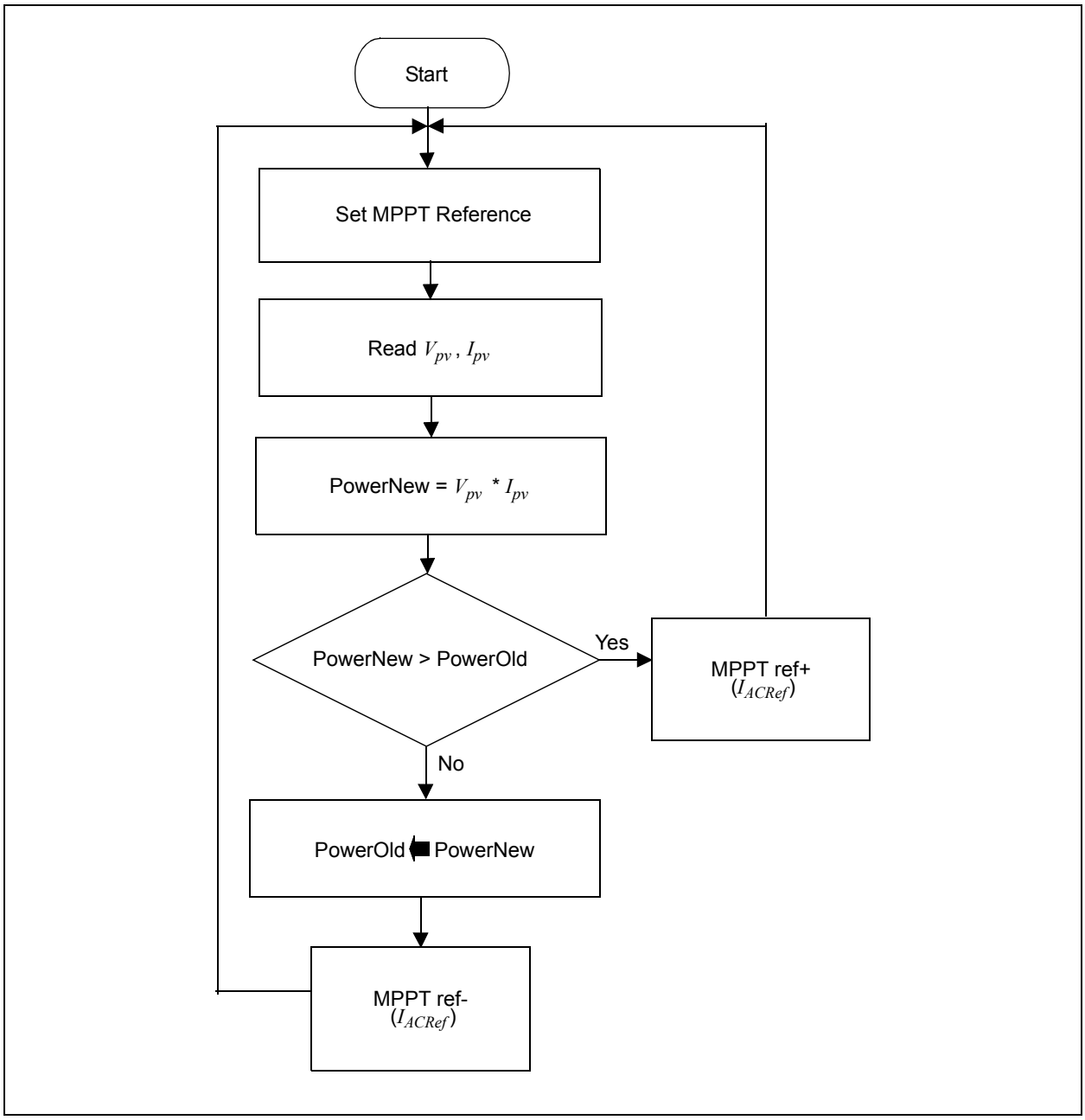
In systems connected to the grid, a critical component of the converter's control system is the PLL that generates the grid voltage's frequency and phase angle for the control to synchronize the output to the grid. the estimated frequency, ωe, and phase angle, θe, of the grid voltage by the PLL can be used not only for control and signal generation, through synthesis or transformations, but also in protection to detect when the converter has entered an islanded mode. As such, PLL systems that can synchronize to these grid parameters accurately and as quickly as possible are of vital importance; otherwise, inaccurate and potentially harmful control of power factor angle, harmonics, and the determination of system mode of operation can result. The grid-connected solar microinverter PLL has been implemented by hardware as well as software zero-crossing detect of grid voltage. Hardware zero-crossing detect is shown in Figure 33.

In software, grid voltage is sampled at every ADC trigger and the polarity of the grid voltage is stored in a register. In every sample grid voltage polarity has been checked. If there is change in grid voltage polarity, software sets the zero voltage detect flag. A period counter register stores the total number of interrupts that occur between two zero-crossing detections. The period counter register value then gives half of the period value of the grid voltage, as the time between the two interrupts is fixed in software and never changes. The period value determines the phase angle increments for sine table reference generation from the sine table. The sine table consists of 512 elements for generating 0-90 degrees of sine reference. As 90-180 degrees of sine waveform is a mirror image of 0 to 90 degrees. Therefore, 0-180 degree, half sine reference is generated in phase and is synchronized with the grid voltage.

MPPT Loop

Two algorithms are commonly used to track the MPPT: the Perturb and Observe (P&O) method and the Incremental Conductance (IncCond) method. The reference design uses the P&O method for MPPT. Figure 39 presents the control flow chart of the P&O algorithm. The MPP tracker operates by periodically incrementing or decrementing the solar array voltage. If a given perturbation leads to an increase (decrease) the output power of the PV, the subsequent perturbation is generated in the same (opposite) direction. In Figure 39, *Set MPPT reference* denotes the perturbation of the solar array voltage, and *MPPT ref+* and *MPPT ref-* represent the subsequent perturbation in the same or opposite direction, respectively. A set MPPT reference decides the peak value of sine reference current generated by the PLL.

FIGURE 39: MPPT CONTROL LOOP BLOCK DIAGRAM



As seen in Figure 3, a slight increase in PV output current after the MPPT point can lead to a decrease in PV output voltage of one-half, and thus, the PV output power. Therefore, the PV voltage is being continuously checked at every zero-crossing of the grid voltage and its value is compared with previous zero-crossing sample of the PV voltage. if the difference in PV is more than 40 mV, the MPPT algorithm reduces the output current reference magnitude, and the power drawn from the PV panel is maintained at an operating point closer to MPP of the PV characteristics curve.

Current Control Loop

The current control loop is a PI controller and is the heart of the control system. This loop corrects the errors between these two currents, which are the inputs to the current control loop:

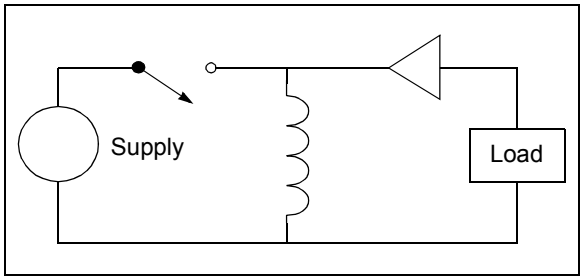
- Reference current signal (I_{ACREF})
- Input current (I_{AC})

The output of the current control loop is a control signal, which ensures that the input current (I_{AC}) follows the reference current (I_{ACREF}). The current control loop executes at a rate of 57 kHz and its bandwidth is 2500 Hz for a switching frequency of 172 kHz. The output of the current control loop decides the duty cycle (D) required for switching the MOSFETs.

Analysis of a Flyback Converter

A flyback converter's equivalent non-isolated circuit is like a buck-boost converter; therefore, for modeling purposes and to calculate control loop coefficients, a buck-boost converter will be used. A buck-boost converter, like the boost converter, is a highly nonlinear system. When the system is operated in Continuous Conduction mode, the relation between the duty ratio and output voltage and current is nonlinear. The challenge is to produce a sine wave current wave shape. A buck-boost converter circuit is shown in Figure 40.

FIGURE 40: BUCK-BOOST CONVERTER



The flyback transformer magnetizing inductance has been replaced by a buck-boost inductor. The switch is given a duty cycle, D. The goal is to drive a rectified sine wave through the load. The topology of the buck-boost produces an inverted output voltage. Therefore, the average current through the diode and load should look like an inverted rectified sine wave. The only current stiff element in the system is the inductor (transformer magnetizing inductance). The current in the inductor does not change instantaneously. The load current is given by Equation 27.

EQUATION 27:

$$I_{load} = I_L(1-D)$$

I_{load} represents I_{AC} in the flyback inverter system, I_L represents current though the magnetizing inductance of the flyback transformer, I_{L*} represents I_{ACref} and D represents the duty of the flyback MOSFET. G is the control loop compensator block coefficient K_p and K_i.

The fundamental equation of the inductor is expressed by Equation 28.

EQUATION 28:

$$V_x = sL\ I_L$$

To control the current, we can close the loop on current with the gain (G). That is, we apply a voltage proportional to current error as expressed by Equation 29.

EQUATION 29:

$$V_x = G(I_L^* - I_L)$$
$$G = \left(K_p + \frac{K_i}{s}\right)$$
$$V_x = G\frac{(I_{load}^* - I_{load})}{(1-D)}$$

From basic power electronic theory
$V_x = V_{in} * D - (1-D) * V_o$

The output voltage V_o is the inverted rectified voltage obtained by directly connecting the grid via a thyristor bridge to the output of the flyback circuit. Since we measure V_{in} and V_o, we can obtain D (in Equation 29), as shown in Equation 30.

EQUATION 30:

$$D' = G\frac{(I_{load}^* - I_{load})}{(1-D)(V_{in}+V_o)} + \frac{V_o}{(V_{in}+V_o)}$$

The input and output voltage relation of the buck-boost converter is expressed by Equation 31.

EQUATION 31:

$$(V_{in} + V_o) \cdot (1 - D) = V_{in}$$

From Equation 30 and Equation 31, the desired duty cycle can be calculated, as shown in Equation 32.

EQUATION 32:

$$D' = G\frac{(I^*_{load} - I_{load})}{V_{in}} + \frac{V_o}{V_{in} + V_o}$$

Where I^*_{load} is a rectified sinusoid.

The first term is the contribution of PI compensator. The bandwidth of the PI compensator is given by G/L rad/s

The second term is the decouple contribution. The goal of this term is to allow the current to follow the sine shape without a controller. The contribution of the controller is small over and above the contribution of the decouple term.

Load Balance Control Loop

The individual output voltage of each flyback converter may differ by a small value. This drift is possible because of differences in the internal characteristics of the MOSFETs, internal resistances of the transformer windings, capacitors and the diodes. Therefore, when the same duty cycle is applied to both of the MOSFETs, it may result in unequal sharing of the load between the two flyback converter stages. This necessitates the presence of a load balance control loop that balances the currents in the two flyback converter switches, which in turn results in the equal sharing of load between the two converters.

One of the inputs to the load balance control loop is the difference between the two MOSFET currents (I_{pv1}-I_{pv2}) of the two flyback converters. The other input, which acts as a reference to this control loop, is tied to zero. This control loop mainly corrects the difference between the MOSFET currents and brings it close to the reference input, which is zero. The output of the load balance control loop will be a duty correction term (ΔD), which is added to the main duty cycle, D, to get the duty cycle of the first boost converter, D_1. The ΔD term is subtracted from the main duty cycle, D, to determine the duty cycle of the second boost converter, D_2.

Load Balance Error Compensator

Similar to the current error compensator, the load balance compensator is also designed by normalizing the output to a range of -1 to +1. The proportional gain for the load balance compensator is derived using the small signal model of the flyback converter (see Equation 32).

Function Usage in Software

The numerical constants and variables are defined in Q15 format or 1.15 format. Because the selected dsPIC device is a 16-bit digital signal controller, if the gains or constants exceed the range of 16 bits in the intermediate calculations, they are appropriately prescaled to a different format during computation and the end result is again converted to the Q15 format by postscaling them.

Table 3 lists and describes the functions used in the software (see **Appendix A: "Source Code"** for additional information).

TABLE 3: FUNCTION USAGE IN SOFTWARE

Filename	Function Name	Description
Source Files		
PVInverter_main.c	Main()	Calls the function to configure the operating frequency of the device and auxiliary clock.
		Calls the functions for configuring I/O Ports, Timer, ADC and PWM modules.
		Calls the function for the state machine.
PVInverter_int.c	initClock()	Configures the operating frequency of the device.
	initPWM()	Configure the PWM module.
	initADC()	Configure the ADC module.
	initIOports()	Configure I/O ports.
	ioLock()	Open I/O port to configure.
	ioUnlock()	Close I/O port after configuration is done.
	initStateMachineTimer()	Configure Timer2 for system state machine.
PVinverter_isr.c	ADCP0Interrupt()	Read ADC value of all feedback signals.
		Check the faults condition.
		Executes the various control loop if faults doesn't exists.
		Disable the PWM output if faults exists.
PVInverter_isr.s	T2Interrupt()	Check PV voltage, Inverter output and Grid voltage condition.
		Disable PWM if any faults exists and switched SYSTEM_ERROR mode.
		Check for the system state.
PVInverter_Variable.c	—	Declaration and Initialization of all the global variables.
Header Files		
PVInverter_defines.h	—	Defines all the global function prototype and global parameters.
PVInverter_Variable.h	—	Includes the supporting file for PVInverter_Variable.c.
PVInverter_macro.h	—	Checks the polarity of the grid voltage and sets the zero-crossing detect flag.
Sinetable512.h	—	Sine table for current reference.
stdlib.h	—	Standard library header file.
dsp.h	—	Interface to the DSP Library for the dsPIC33F.
Include File		
PVMicroInverter.inc	—	PERIOD macro to calculate period value grid voltage.
	—	ZCD_Detect detect macro for software zero-crossing detect.

Resource Usage in Software

Table 4 lists the resources utilized by the reference design software when developed on a dsPIC33FJ16GS504 device.

TABLE 4: SOFTWARE RESOURCES

Resources	Components	Value
Memory	Program Memory/Flash	9357 Bytes 58%
	Data Memory/RAM	488 Bytes 23%
MIPS/Instruction Cycle	Current Loop	~280 cycles @ 57 kHz
	MPPT Loop	~125 cycles @ 125 Hz
	Load Balance Loop	~95 cycles @ 2kHz
	PLL	~170 cycles @ 57 kHz

MATLAB® Modeling

The control system design for the reference design is accomplished using the MATLAB Simulink® model. The various system gains and the parameter values of the PI controllers and the compensators are derived using this model.

Figure 41 shows the solar microinverter MATLAB model, Figure 42 shows the digital control system, and Figure 43 shows the two parallel interleaved flyback converters.

FIGURE 41: MATLAB® MODEL

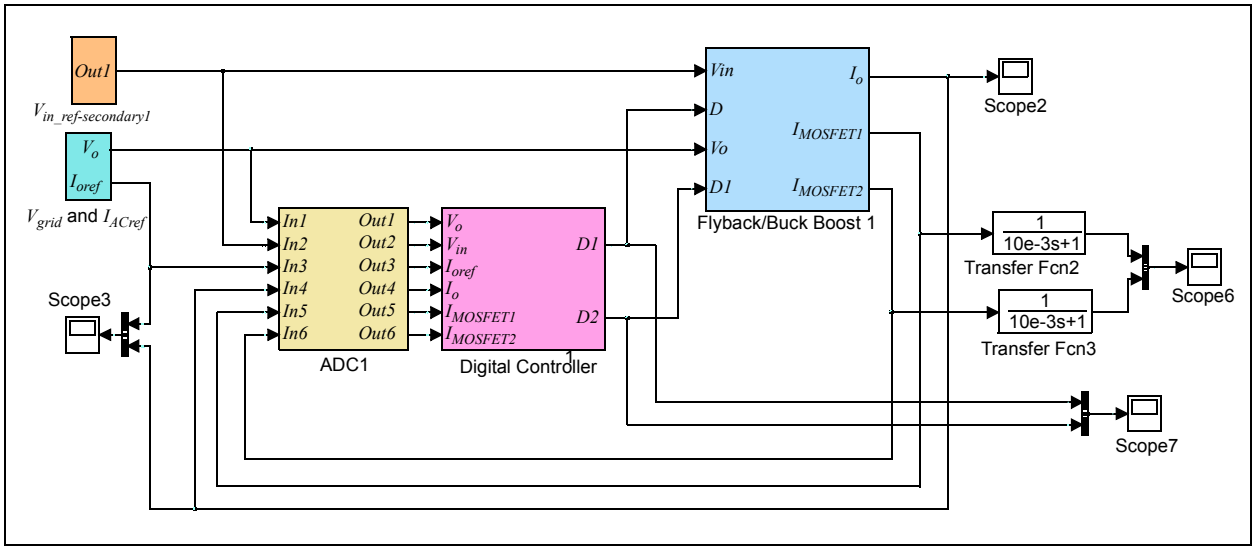


FIGURE 42: DIGITAL CONTROL SYSTEMS

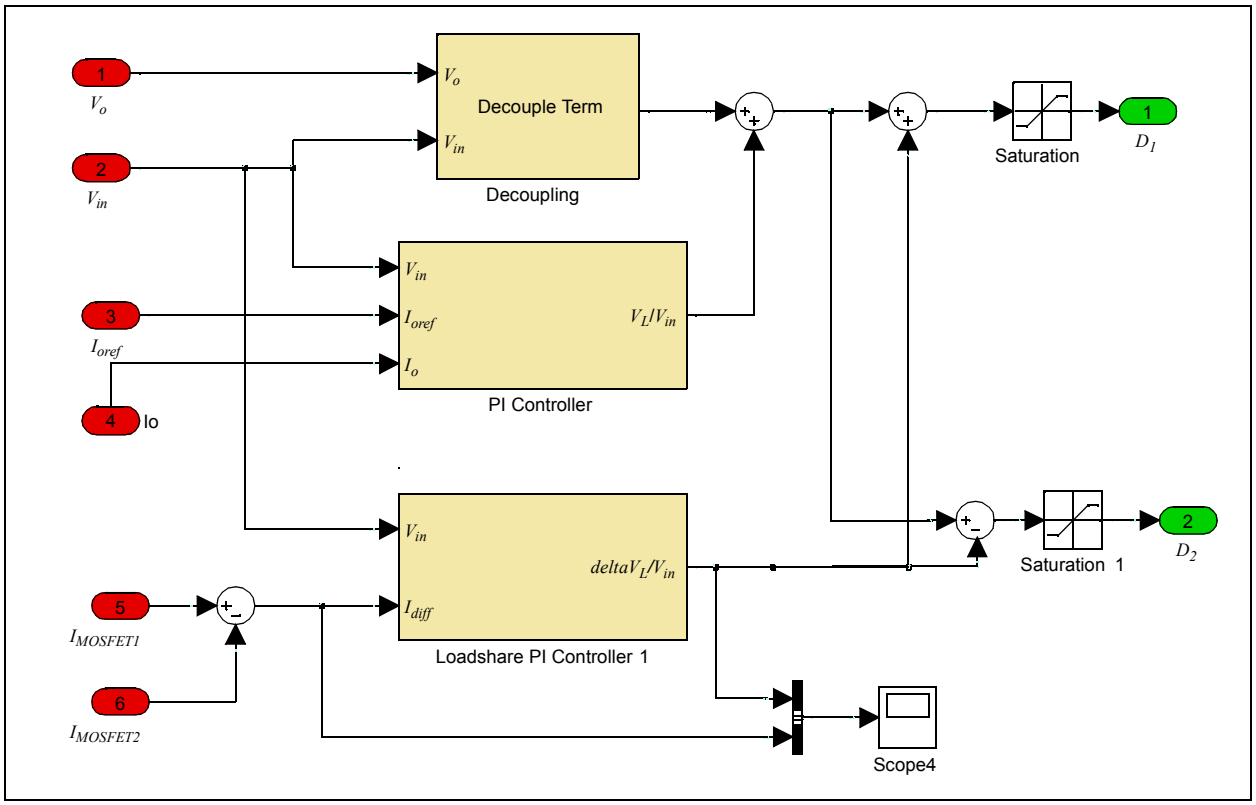
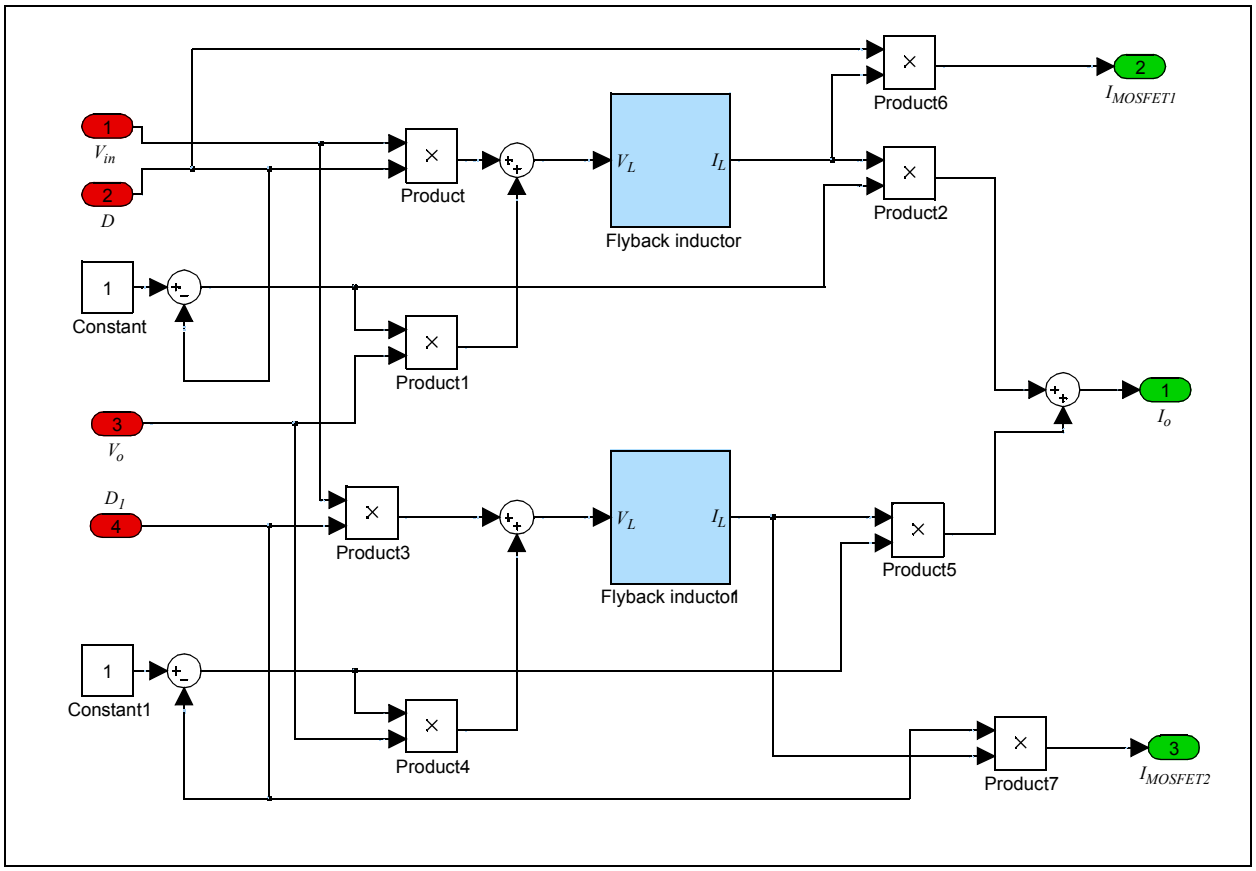


FIGURE 43: TWO PARALLEL INTERLEAVED FLYBACK CONVERTERS



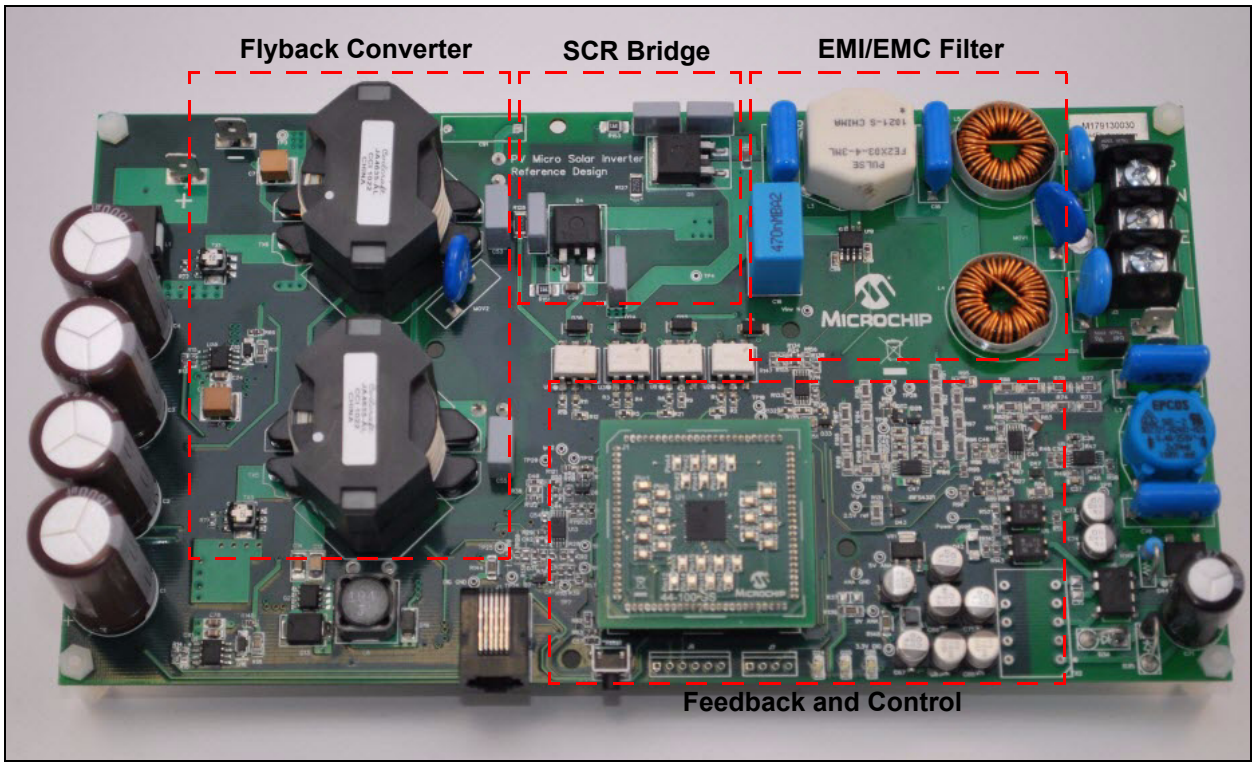
GRID-CONNECTED SOLAR MICROINVERTER REFERENCE DESIGN INSTALLATION AND CONFIGURATION

The reference design is intended to aid the user in the rapid evaluation and development of a grid-Connected microinverter using a dsPIC DSC.

This flexible and cost-effective design can be configured in different ways for use with Microchip's specialized Switch Mode Power Supply (SMPS) Digital Signal Controllers. The reference design supports the dsPIC33F "GS" device family. It offers a mounting option to connect either a 28-pin SOIC device or a generic 100-pin Plug-In Module (PIM). The system has two flyback circuits to control the grid current. The rated continuous PV panel power that can be connected to the system is 220 watts. Refer to **Appendix B: "Electrical Specifications"** for additional information.

Note:	Before using the reference design, carefully read the **"Hardware Design"** section.

FIGURE 44: GRID-CONNECTED SOLAR MICROINVERTER REFERENCE DESIGN BOARD



Getting Started

CONNECTING THE SYSTEM

Before connecting the system to either a PV panel or a single-phase grid, please conduct a visual inspection and make sure that no components are broken or damaged, and that no foreign objects have fallen inside the enclosure.

Make sure that the ON/OFF switch is in the OFF position, and ensure the red-tipped PV cable is connected to the positive input terminal and the yellow-tipped cable is connected to the negative terminal of the inverter system.

If the grid connection cable provided with the reference design has been misplaced or lost, it is recommended that cables used for connecting inverter output to the grid have a 5 Amp fuse. The grid connection wire should be double-insulated, 3-core flex cable with a minimum current rating of 10A (1 mm2 18 AWG). Care should be taken to ensure that stray strands of wire do not short to adjacent terminals of the enclosure and output terminal of the inverter. If possible, grid-connected wires should be stripped and tinned with solder before connecting to the reference design terminals. A computer power cable can also be used. The recommended output cable size is 1.0 to 1.5 mm2 (18-16 AWG) and should have a 600V rating. This cable should also be double insulated or have a protective ground screen.

Access to the terminal screws is provided via holes in the lid of the enclosure. A slotted screwdriver should be used. The system connections are shown in Figure 45.

CONNECTING THE HARDWARE

Before attempting to power-up the system, the following recommended hardware connection process must be completed.

To set up the system, complete the following steps:

1. Ensure the system is OFF by setting the ON/OFF switch to the OFF position.
2. Connect the grid connection cable to the inverter output and to the grid directly or through an auto-transformer (i.e., Variac).
3. Connect a differential probe and multimeter to the output terminal to measure the output voltage.
4. Cover the PV panel to make sure its output voltage is very low. A dark cloth or cardboard can be used.
5. Connect the multimeter/scope probe to read the PV voltage.
6. Connect the positive terminal of the PV panel cable to the positive terminal of the microinverter.
7. Connect the negative terminal of the PV panel cable to the negative terminal of the microinverter.
8. Increase the grid voltage to 100 V_{AC} if it is connected through the auto-transformer or the grid voltage. Make sure the multimeter/scope reads 100 V_{AC} at the output terminal of the reference design.
9. If it reads 110 V_{AC} voltage at the output terminal, this means the grid connection is okay.
10. Connect one of the wires (Phase/Neutral) connecting to grid and inverter output. The direction of the current probe should be current flowing to the grid.
11. Remove any covers from the PV panel.
12. The input of the solar microinverter voltage should be equal to the expected PV output voltage. If it is not, DO NOT turn the system on and contact a local Microchip Field Application Engineer.
13. If the solar microinverter voltage is equal to the expected PV output voltage, set the ON/OFF switch to the ON position to start supplying energy to the grid from the grid-connected PV panel.
14. Observe the grid voltage and current waveform. The current waveform should be sinusoidal and in phase with the grid voltage.

LABORATORY TEST RESULTS AND WAVEFORMS

Figure 45 through Figure 52 show the waveforms for the grid voltage, grid current, system islanding, and MPP voltage. In the following oscilloscope images, the waveforms are designated as follows:

- CH1 = Yellow → Solar microinverter input voltage
- CH2 = Green → Solar microinverter input current
- CH3 = Violet → Grid voltage
- CH4 = Magenta → Grid current

This information aids in validating the digital implementation on a dsPIC DSC device.

FIGURE 45: GRID VOLTAGE AND GRID CURRENT

FIGURE 46: SYSTEM ISLANDING: SYSTEM TURNED OFF WHEN GRID FAILS

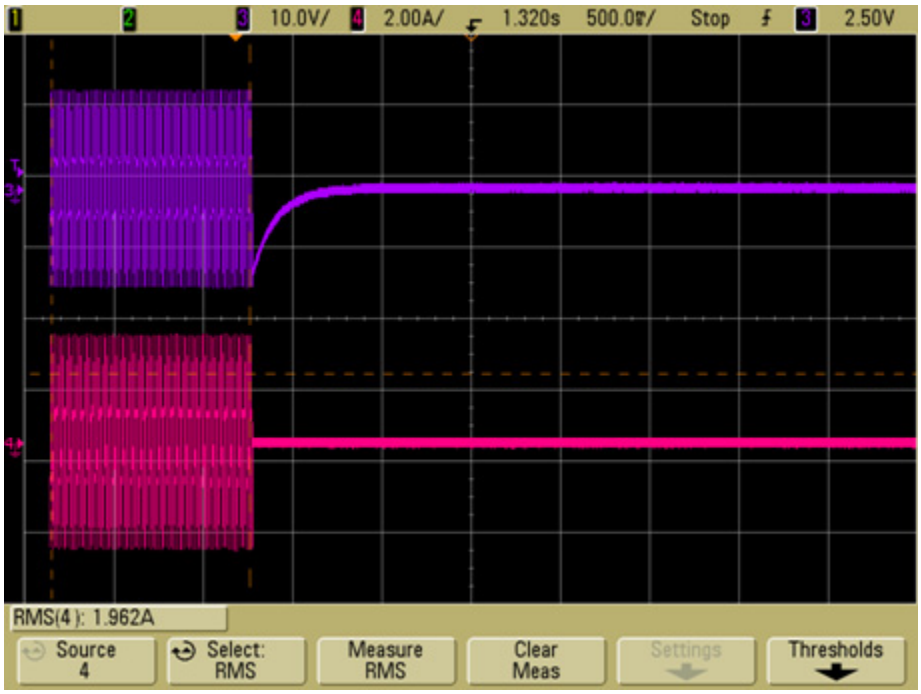


FIGURE 47: SYSTEM ISLANDING: SYSTEM TURNED OFF WHEN GRID FAILS AT PEAK OF AC VOLTAGE

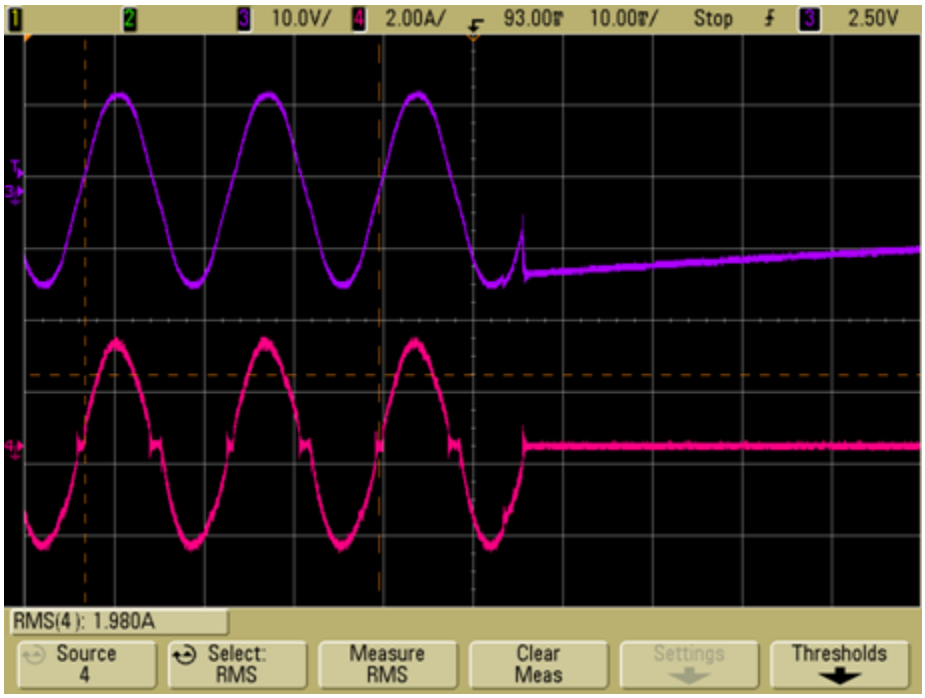


FIGURE 48: SYSTEM ISLANDING: SYSTEM TURNED OFF WHEN GRID FAILS AT ZERO OF AC VOLTAGE

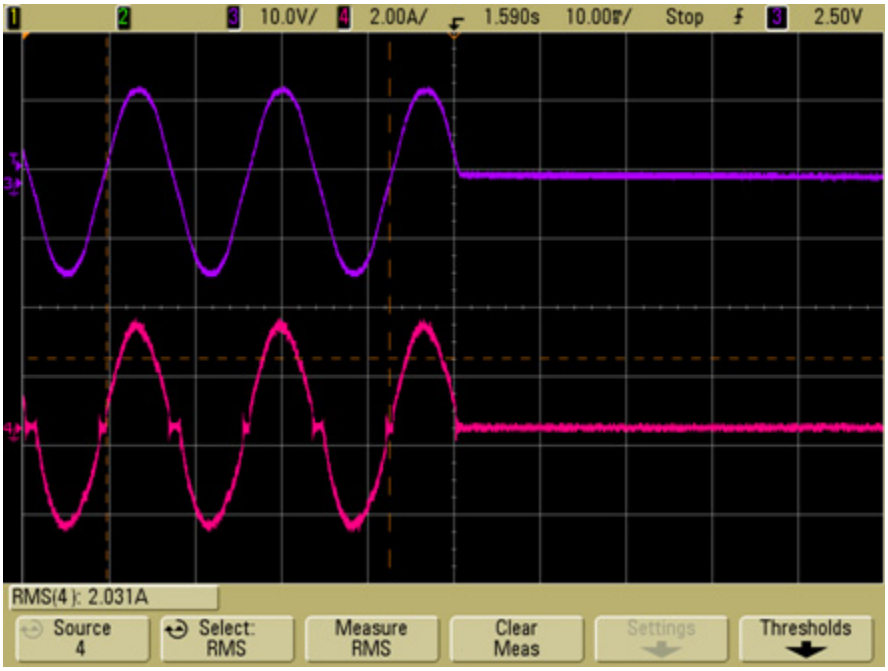


FIGURE 49: NIGHT_MODE: SYSTEM TURNED OFF WHEN INPUT VOLTAGE IS LESS THAN UNDERVOLTAGE LIMIT

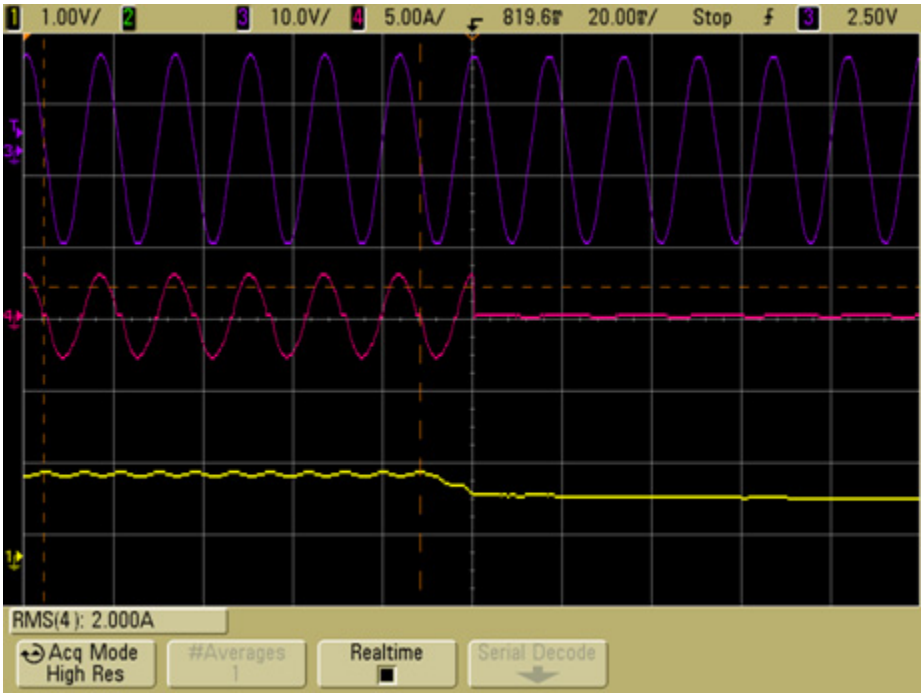


FIGURE 50: NIGHT_MODE: SYSTEM TURNED ON WHEN INPUT VOLTAGE IS MORE THAN UNDERVOLTAGE LIMIT

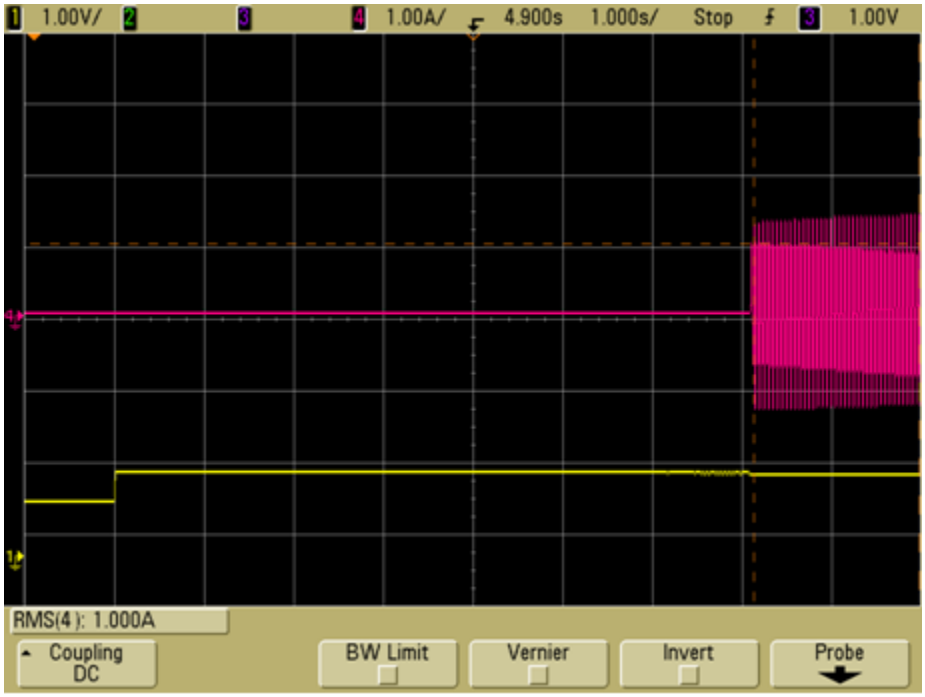


FIGURE 51: VOLTAGE AND CURRENT RIPPLE OF PV PANEL

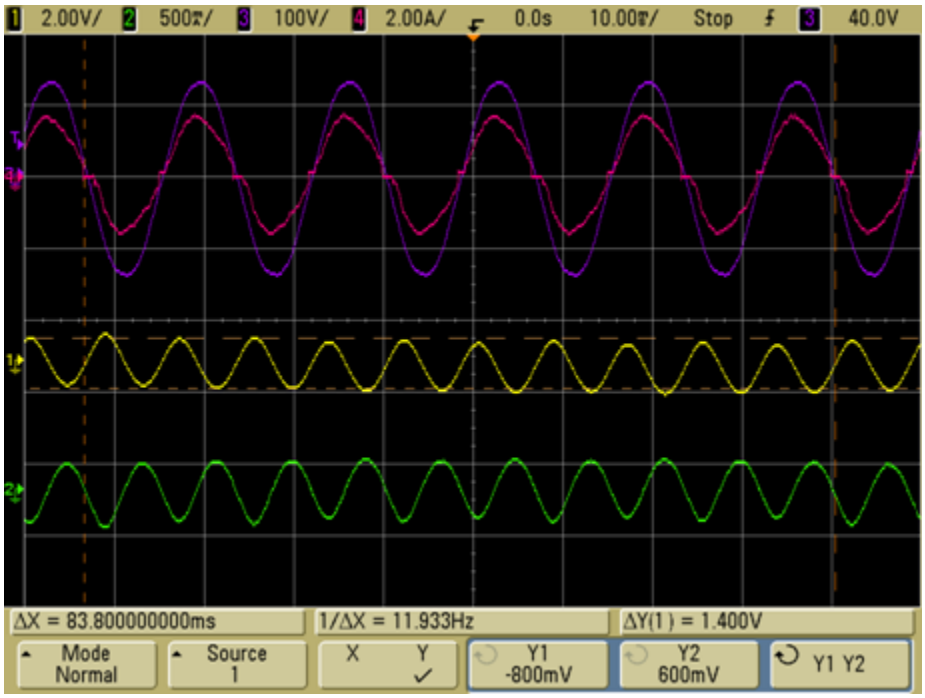
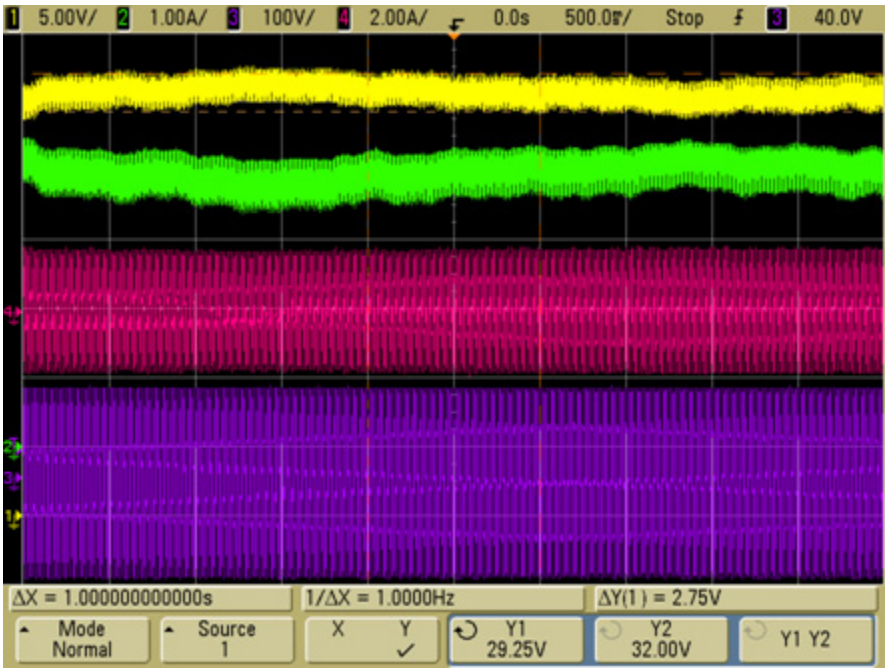


FIGURE 52: VOLTAGE AND CURRENT RIPPLE OF PV PANEL IN LARGE SCALE



APPENDIX A: SOURCE CODE

Software License Agreement

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APPENDIX B: ELECTRICAL SPECIFICATIONS

The reference design was tested with a 180 watt, 36V solar panel connected to 120 V_{AC} single-phase grid.

TABLE B-1: ELECTRICAL SPECIFICATIONS

Parameter	Description	Minimum	Maximum	Typical	Units
η	Efficiency	—	—	95	%
f_{im}	Grid Frequency	55	65	60	Hz
I_{in}	PV Panel Output Current	—	10		A
I_{out}	Grid Current	—	—	2.05	A
I_{sc}	Input Short Circuit Current	—	—	10	A
I_{THD}	Output Current THD	—	—	5	%
$MPPT$	Maximum Power Point Tracking	—	—	99.5%	—
PF	Output Power Factor	0.95	—	—	—
P_{MPP}	Maximum PV Power	—	220	220	W
P_{night}	Nighttime Power Consumption	—	1	0	W
P_{out}	Output Power	—	—	185	W
V_{grid}	Grid Voltage	90	140	120	V
V_{in}	PV Panel Voltage	25	55	36	V
V_{MPP}	Maximum Power Point PV Voltage	25	45	36	V

APPENDIX C: DESIGN PACKAGE

A complete design package for this reference design is available as a single WinZip® archive file. This archive can be downloaded from the Microchip corporate Web site at: **www.microchip.com**

C.1 Design Package Contents

The design package contains the following items:

- Reference design schematics
- Fabrication drawings
- Bill of materials
- Assembly drawings
- Hardware design Gerber files

APPENDIX D: GLOSSARY

TABLE D-1: SYMBOL AND TERM DESCRIPTIONS

Symbol/ Term	Description
α	Taylor coefficient
β	Taylor coefficient
EMC	Electromagnetic Compatibility
EMI	Electromagnetic Interference
I_{sc}	PV module short circuit current
MPP	Maximum Power Point
MPPT	Maximum Power Point Tracker
P_{MPP}	Power at MPP
PV	Photovoltaic
PWM	Pulse Width Modulation
THD	Total Harmonic Distortion
$\hat{U}$	Amplitude of PV voltage ripple
$UMPP$	Voltage at MPP
V_{ds}	MOSFET drain-to-source voltage
V_{in}	PV microinverter system input voltage
V_{open}	PV module open circuit voltage
$V_{rectified}$	Rectified voltage at inverter output
$V_{reflected}$	Secondary winding reflected voltage at primary of flyback transformer
W	Wattage
ω	Frequency in rad/sec

APPENDIX E: HARDWARE AND SOFTWARE CHANGES FOR 230 V_{AC} UNITS

This appendix describes the changes in hardware and software for a 230 V_{AC} unit as compared to a 110 V_{AC} unit.

E.1 Hardware Changes

- Grid Voltage Sense

  The feedback resistors, R99 and R100, have been changed to 4.7k to make sure the analog pin voltage of the dsPIC DSC is between 0 to 3.3V at maximum grid voltage (264 V_{AC}).

- Zero-Crossing Detect

  The feedback resistors, R81 and R82, have been changed to 4.7k to make sure the differential output voltage is between 0 to 5 V at maximum grid voltage (264 V_{AC}).

- Inverter Output Voltage Sense

  The feedback resistors, R111 and R112, have been changed to 4.7k to make sure the analog pin voltage of the dsPIC DSC is between 0 to 3.3V at maximum grid voltage (264 V_{AC}).

- Grid AC Current Sense

  The DC offset voltage resistor divider value was changed to R147 = 2.4K Ohm, and R155 = 3.3K Ohm. Also, the feedback gain resistor value of U14 was changed to R132 = R133 = 1.6K Ohm, and R135 = 5.1K Ohm to make sure the I_{AC} sense voltage is between 0 to 3.3V at full output power.

- PV Voltage Sense

  The PV voltage sense resistor divider network value was changed to R123 = 160K Ohm and R175 = 7.5K Ohm to make sure the AC voltage and PV voltage have the same normalized value in Q15 format.

- Flyback Transformer TX5 and TX6

  The flyback transformer turns ratio was changed to N_p = 6 and N_s = 70, and its part number. Please refer to the 230 V_{AC} unit Bill of Materials (BOM) for more information, which is included in the WinZip archive file for the reference design.

E.2 Software Changes

- Grid Voltage Frequency Limit

  The 230 V_{AC} unit is designed to work with 50 Hz grid frequency; therefore, its frequency limit of operation was changed to address 45 to 55 Hz.

- Grid Voltage Limit

  The undervoltage limit was changed to 180 V_{AC} and the overvoltage limit was changed to 264 V_{AC}. Refer to the reference design source code for more information.

- Inverter Output Voltage Limit

  The undervoltage limit was changed to 180 V_{AC} and the overvoltage limit was changed to 274 V_{AC}. Refer to the reference design source code for more information.

- Control Loop Coefficient

  The control loop coefficient is as per the modeling of the 230 V_{AC} unit. Refer to the reference design source code for more information.

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