Description

The SDT7535 is a highly integrated low cost current mode PWM controller. It is ideal for small power of offline AC-DC flyback converter applications. To minimize standby power consumption, PFM mode function provides continuously decrease the switching frequency modulation under light loading conditions. Under zero loading or very low loading conditions, the IC enters burst mode which completely shuts off PWM output. The SDT7535 is integrated a frequency-hopping function that helps reduce EMI emission of a power supply with minimum line filters. The built-in synchronized slope compensation enhances the stability of the system and avoids sub-harmonic oscillation.

Other protection functions include VDD over voltage protection, leading-edge blanking of the current sensing, cycle by cycle current limit and PWM output clamped at 16V to protect external MOSFET from over-voltage damage. It would provide the users a superior AC/DC power application of higher efficiency, low external component counts, and lower cost solution for applications.

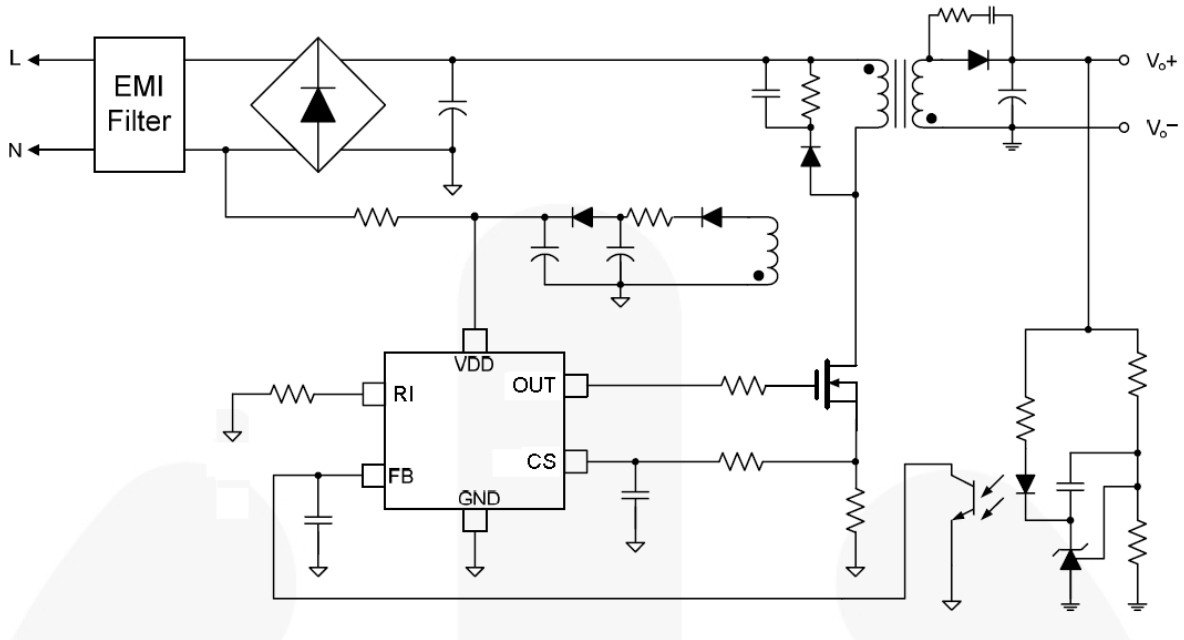
Features

- Very Low Startup Current (<20uA)
- Peak-Current Mode Control With Cycle By Cycle Current Limit
- Non-audible-noise Green Mode
- Under Voltage Lockout(UVLO)
- Leading-Edge Blanking(LEB)
- Programmable Switching Frequency With Frequency Hopping For Better EMI
- Internal Synchronized Slope Compensation
- VDD Over Voltage Protection(OVP)
- Over Load Protection(OLP)
- Short Circuit Protection(SCP)
- Clamped Gate Output voltage
- 300mA Driving Capability

Applications

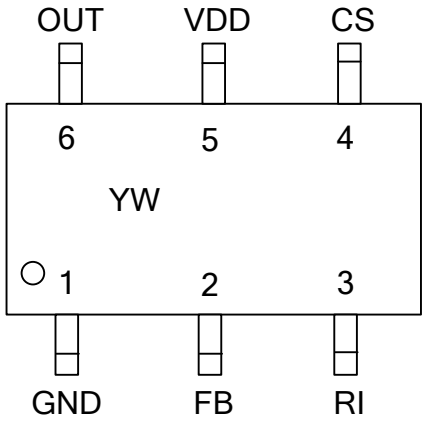
- Switching AC/DC Adaptor
- Battery Charger
- Open Frame Switching Power Supply

Typical Application



Pin Configuration

SOT23-6 Top View



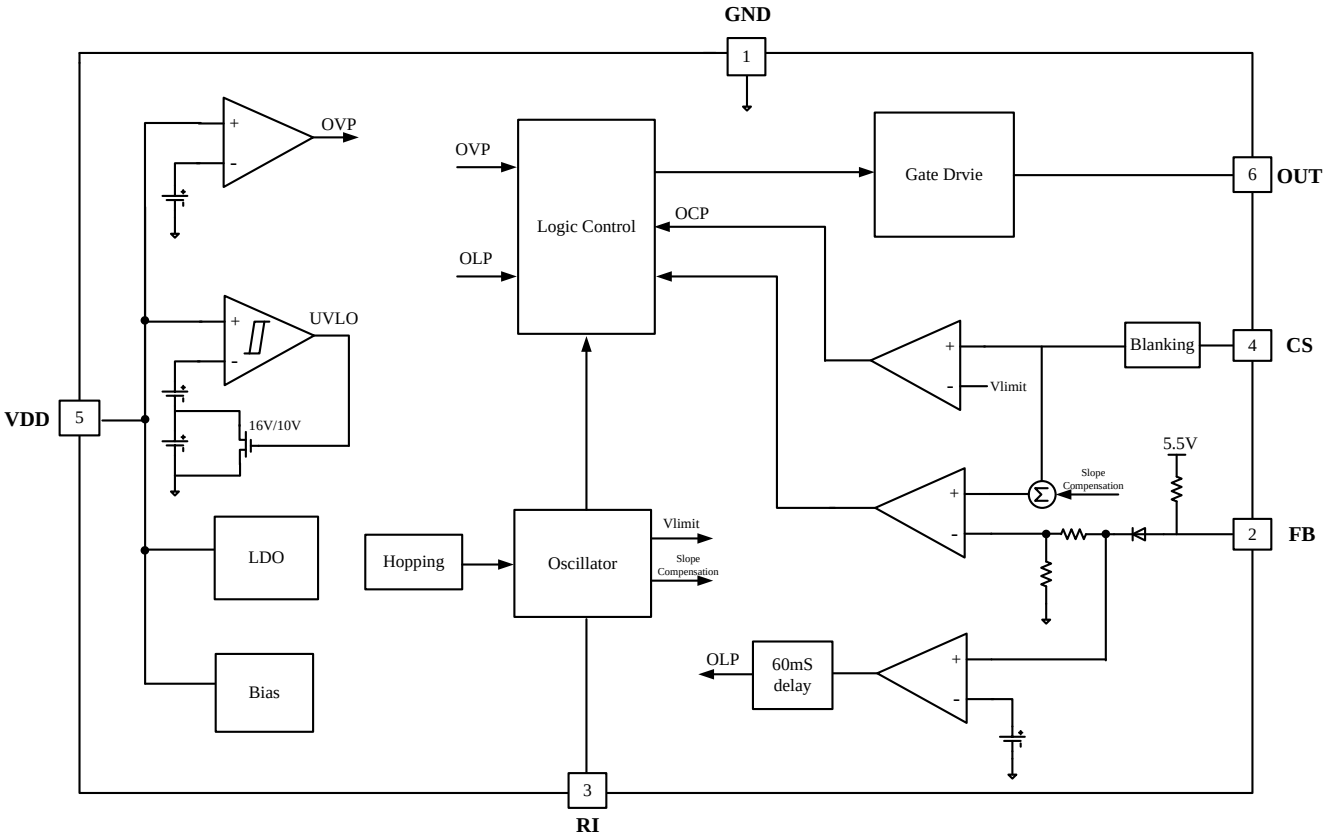
Y: Year code

W: week code

Pin Description

Name	Description
GND	Ground
FB	Voltage feedback pin, By connecting a photo-coupler to close the control loop and achieve the regulation.
RI	This pin is to program the switching frequency. By connecting a resistor to ground to set the switching frequency.
CS	Current sense pin, a resistor connects to sense the MOSFET current.
VDD	Power supply voltage pin.
OUT	Totem output to drive the external power MOSFET.

Block Diagram



Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only. All voltage values, except differential voltages, are given with respect to GND pin.

Symbol	Parameter	Min.	Max.	Unit
VDD	Supply Voltage		30	V
V_L	Input Voltage to FB, RI, CS pin	-0.3	7	V
P_D	Power Dissipation at TA<50℃		300	mW
θ_{JC}	Thermal Resistance (Junction-to-Case)		115	℃/W
T_J	Operating Junction Temperature	-40	+150	℃
T_{stg}	Storage Temperature Range	-55	+150	℃
T_L	Lead Temperature, Wave Soldering, 10 Seconds		+260	℃
ESD	Human Body Model		2.5	KV
	Machine Model		250	V

Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. It does not recommend exceeding them or designing to Absolute Maximum Ratings.

Symbol	Parameter	Min.	Max.	Unit
VDD	Supply Voltage	11	25	V
RI	RI Pin Resistor Value	50	130	Kohm
Fsw	Switch Frequency	50	130	KHz

Electrical Characteristics

VDD = 15V and TA = 25℃ unless otherwise noted.

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
Supply Section(VDD Pin)						
VDD_on	Turn-on Threshold Voltage		15	16	17	V
VDD_off	Turn-off Threshold Voltage		9	10	11	V
I_{VDD_ST}	Start-up Current			5	20	uA
VDD_ovp	VDD Over Voltage Protection		26	27.5	29	V
I_{VDD_OP}	Normal Operation Supply Current	C_L=1nF		2	3	mA
Feedback Section(FB Pin)						
Av	Input Voltage to Current Sense Attenuation			3		V/V
Z_{FB}	FB Input Impedance			5		Kohm
V_{FB_OPEN}	FB Pin Open Voltage		5.0	5.5	6.0	V
V_{FB_OLP}	Threshold Voltage For Open Loop Protection			4.3		V
T_{D_OLP}	Open Loop Protection Delay Time		50	60	70	mS
Current Sense Section(CS Pin)						
T_{LEB}	Leading Edge Blanking Time			250		nS
T_{PD}	Delay to Output			100		nS
V_{OCP_L}	Valley Threshold Voltage For Current Limit	Duty=0%		0.70		V
V_{OCP_H}	Flat Threshold Voltage For Current Limit	Duty>50%	0.90	0.95	1.00	V
Oscillator Section(RI Pin)						
Fsw	Switch Frquency	RI=100Kohm	60	65	70	KHz
$T_{hopping}$	Hopping Period			4.4		mS
$R_{hopping}$	Hopping Range			3		%
F_{DV}	Voltage Stability	VDD=11V~25V			1	%
F_{DT}	Temperature Stability	-40℃ ~150℃			3	%
Fsw_min	Green Mode Minimum Frequency			22		KHz
V_{FB_G}	FB Threshold Voltage For Frequency Reduction			2.4		V
V_{FB_B}	FB Threshold Voltage For Burst Mode			1.9		V
PWM Output Section(OUT Pin)						
V_{OL}	Output Voltage Low	I_O=20mA			1.0	V
V_{OH}	Output Voltage High	I_O=20mA	8.0			V
Tr	Rising Time	C_L=1nF		250		nS
Tf	Falling Time	C_L=1nF		80		nS
Vclamp	Output Clamping Voltage		14	16	18	V

Application Information

Operation Overview

The SDT7535 meets the green-power requirement and is intended for the use in those modern switching power suppliers and adaptors which demand higher power efficiency and power-saving. It integrated more functions to reduce the external components counts and the size. Its major features are described as below.

Startup Current and Under Voltage Lockout

The startup current of SDT7535 is set to be very low so that a large value startup resistor can be used to minimize the power loss. For AC to DC adaptor with universal input range design, a 2 MΩ, 1/8 W startup resistor and a 10uF/25V VDD hold capacitor could be used.

The turn-on and turn-off threshold of the SDT7535 is designed to 16V/10V. During startup, the hold-up capacitor must be charge to 16V through the startup resistor. The hysteresis is implemented to prevent the shutdown from the voltage dip during startup.

Internal Bias and Oscillator Operation

A resistor connected between RI pin and GND pin sets the internal constant current source to charge or discharge the internal fixed capacitor. The charge time and discharge time determines the internal clock speed and the switching frequency. Increasing the resistance will reduce the value of the input current and reduce the switching frequency. The relationship between RI and PWM switching frequency follows the below equation within the RI allowed range.

$$Fsw = \frac{6500}{RI(Kohm)} (KHz)$$

Green Mode Operation

The power dissipation of switching mode power supply is very important in zero load or light load condition. The major dissipation results from conduction loss、switching loss and consume of the control circuit. However, all of them relates to the switching frequency. There are many difference topologies has been implemented in different chip. The basic operation theory of all these approaches intends to reduce the switching frequency under light-load or no-load condition.

The SDT7535 uses feedback voltage (VFB) as an indicator of the output load and modulates the PWM frequency, as shown in Figure 1, such that the switching frequency decreases as load decreases. In heavy load conditions, the switching frequency is 65 KHz. Once VFB decreases below V_{FB-G}, the PWM frequency starts to linearly decrease from 65 KHz to 22 KHz to reduce the switching losses. As VFB decreases below V_{FB_B}, the switching frequency is fixed at 22 KHz. As VFB decreases below V_{FB_B}, the IC enters burst-mode operation and stops switching and the output voltage starts to drop, which causes the feedback voltage to rise. Once VFB rises above V_{FB_B}+0.1V, switching resumes. Burst mode alternately enables and disables switching, thereby reducing switching loss in standby mode.

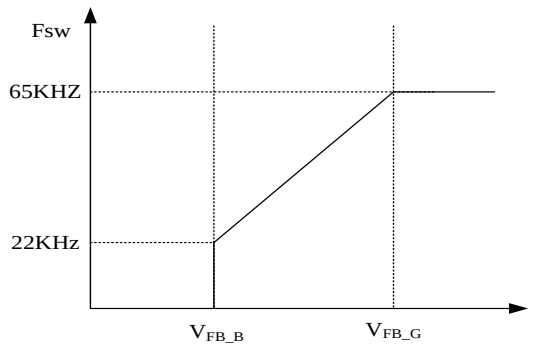


Figure 1

Frequency Hopping

EMI reduction is accomplished by frequency hopping, which spreads the energy over a wider frequency range than the bandwidth measured by the EMI test equipment. An internal frequency hopping circuit changes the switching frequency between 63 kHz and 67 kHz with a period of 4.4ms, as shown in Figure 2.

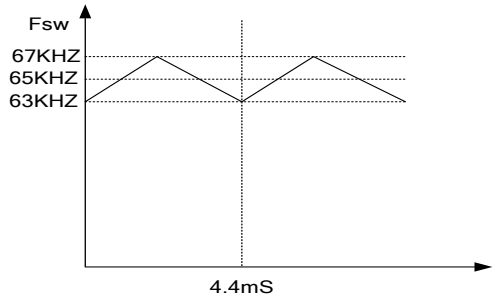


Figure 2

Constant Output Power Limit

SDT7535 has saw-limiter for pulse-by-pulse current limit, which guarantees almost constant power limit over different line voltages of universal input range. The conventional pulse-by-pulse current limiting scheme has a constant threshold for current limit comparator, which results in a higher power limit for high line voltage. SDT7535 has a saw tooth current limit threshold that increases progressively within a switching cycle, which provides lower current limit for high line and makes the actual power limit level almost constant over different line voltages of universal input range, as shown in Figure 3.

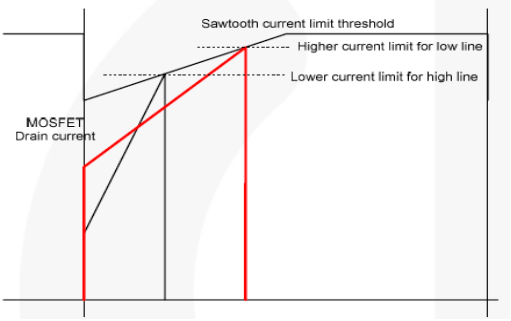


Figure 3

Leading-edge Blanking

Each time the power MOSFET is switched on, a turn-on spike occurs across the sense-resistor caused by primary-side capacitance and secondary-side rectifier reverse recovery. To avoid premature termination of the switching pulse, a leading-edge blanking time is built in. During this blanking period (250ns), the PWM comparator is disabled and cannot switch off the gate driver.

Over Load Protection and Short Circuit Protection (OLP/SCP)

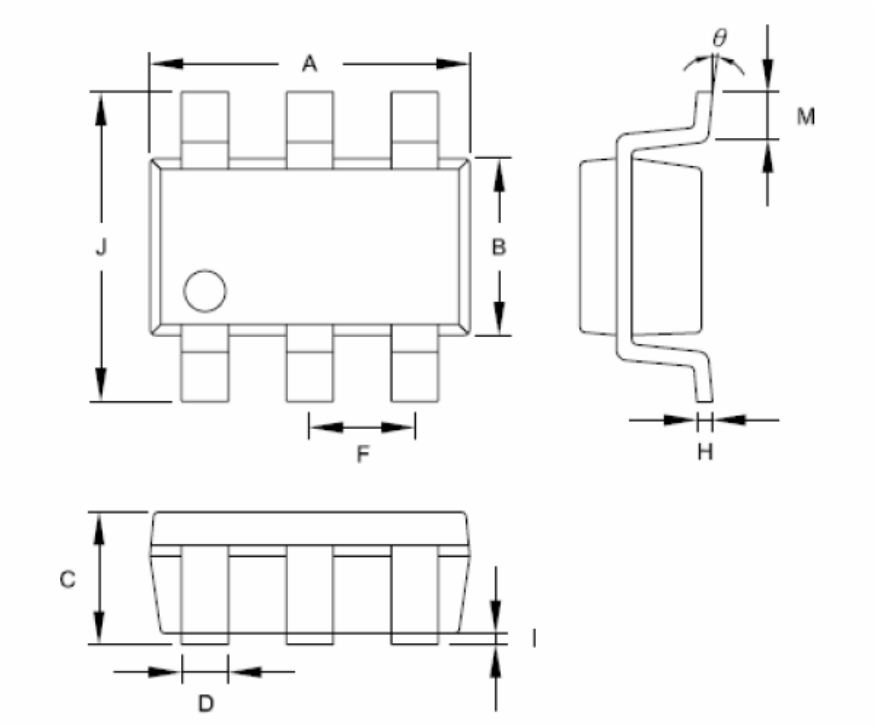
To protect the circuit from being damaged under over load condition or short condition, a smart OLP/SCP function is implemented in the SDT7535. In this case, the feedback system will force the voltage loop proceed toward the saturation and then pull up the voltage on FB pin . Whenever the FB voltage trips up to the V_{FB_OLP} threshold and stays longer than 60mS, the protection will activate and then turn off the gate output to stop the switching of power circuit. The 60mS delay time is to prevent the false trigger from the power-on and turn-off transient. By such protection mechanism, the average input power can be reduced to very low level so that the component temperature and stress can be controlled within the safe operating area.

VDD Over Voltage Protection (OVP)

VDD over voltage protection prevents IC damage caused by over voltage on the VDD pin. The OVP is triggered when VDD reaches 27.5V. A debounce time (typically 20μs) prevents false triggering by switching noise.

Package Information

SOT23-6



Symbol	Dimension in Millimeters		Dimensions in Inches	
	Min	Max	Min	Max
A	2.692	3.099	0.106	0.122
B	1.397	1.803	0.055	0.071
C	-------	1.450	-------	0.058
D	0.300	0.550	0.012	0.022
F	0.838	1.041	0.033	0.041
H	0.080	0.254	0.003	0.010
I	0.050	0.150	0.002	0.006
J	2.600	3.000	0.102	0.118
M	0.300	0.600	0.012	0.024
θ	0	10 °	0	10 °