High Accuracy Constant Current Off-Line High Brightness LED Driver

Features

- High accuracy constant current
- Constant frequency or constant off-time operation
- Works with high side current sensing
- Buck switch mode controller
- Internal 350V linear regulator (can be extended using external zener diodes)
- Internal 2% Voltage Reference
- High PWM dimming ratio
- Programmable MOSFET current limit
- Programmable slope compensation
- Output short circuit protection
- Output over voltage protection
- Enable & PWM dimming
- Soft start
- +0.2A/-0.4A GATE drive
- Synchronization capability
- Typical gain 1±1% (Current Monitor)
- Max. V_{SENSE} 500mV (Current Monitor)
- Max. quiescent current 50μA (Current Monitor)

Applications

- TFT flat panel backlighting
- AC/DC LED lamp
- LED traffic light
- T5, T8 LED line bar
- MR-16 lamp
- Signage or decorative LED lamp

General Description

The LD9102 is a current mode control LED driver IC embedded with high side current monitor. It has been designed for the purpose of controlling single buck switch mode PWM converters at a fixed frequency or fixed off-time mode.

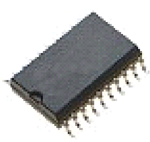
The high side current monitor is built to transfers a high side current measurement voltage to its ground referenced output with an accurate voltage gain of one. This monitor function features with a very wide input voltage range, high accuracy of transfer ratio, and low power consumption. A peak current control scheme is used by the controller (with programmable slope compensation). It includes an internal trans-conductance amplifier to modify the output current in closed loop. This allows high output current accuracy.

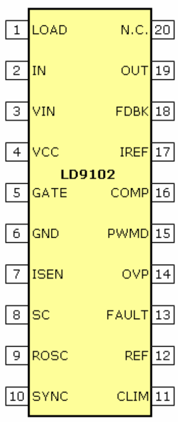
For high power applications, the IC also comprises a 0.2A source and 0.4A sink GATE driver. There is an internal 9 to 350V linear regulator which powers the IC. This makes it no longer necessary to separate power supply for the IC. The LD9102 provides a TTL compatible, PWM dimming input that can accept an external control signal with a duty ratio of 0-100% and a frequency of up to a few kilohertz.

The IC has the function of a FAULT output which, can be used to disconnect LEDs in the circumstance that there is a fault condition it will use an external disconnect FET.

The LD9102 based LED driver ideally suited to RGB backlight applications with DC inputs. The LD9102 based LED lamp drivers can reach efficiency of more than 90%.

Package Pin Out





Ordering Information

		Packing Options	
Part No.	Package	Tube(TU)	Tape & Reel(TR)
LD9102	SOP20 (G3)	LD9102G3-TU	LD9102G3-TR

- Package material default is "Green" package.

Product Marking

For SOP20 (G3)

LD8888 VV YYWW-AB SSSSS ●	Line 1: "LD" is a fixed character 8888: product name VV: Voltage Line 2: YYWW: year and week no. A: package material code B: the brevity code of assembly house Line 3: SSSSS: lot no.

Absolute Maximum Ratings

Parameter	Maximum	Unit
V_{IN}, V_{LOAD} to GND	-0.5~ +350	V
VCC to GND	-0.3~ +13.5	V
PWMD, GATE, I_{SEN}, all other pins to GND	-0.3~VCC+0.3	V
V_{OUT} to GND (Current Monitor)	-0.5~ +10.0	V
V_{SENSE}= V_{IN} - V_{LOAD} (Current Monitor)	-0.3~ +5.0	V
I_{LOAD} (Current Monitor)	-10.0~ +10.0	mA
Continuous Power Dissipation (T_A = +25°C)		
20-Pin SOIC, de-rate 10.0mW/°C above +25°C	1000	mW
Junction to ambient thermal impedance	82	°C/W
Operating ambient temperature range	-40~ +85	°C
Junction temperature	+125	°C
Storage temperature range	-65~ +150	°C

The values beyond the boundaries of absolute maximum rating may cause the damage to the device. Functional operation in this context is not implied. Continuous use of the device at the absolute rating level might influence device reliability. All voltages have their reference to device ground.

Electrical Characteristics

VIN=24V, T_A=25°C unless specified, otherwise minimum and maximum values are guaranteed by production testing requirements.

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Input						
Input DC supply voltage range	V_{INDC}	DC input voltage	9[*1]	–	350	V
Shut-down mode supply current	I_{INSD}	PWMD connected to GND, V_{INDC} = 24V	–	1.0	1.5	mA
Internal Regulator						
Internally regulated voltage	VCC	V_{INDC} = 9~350V, IDD(ext) = 0, PWMD= GND	7.25	7.75	8.25	V
VCC under voltage lockout threshold	UVLO	VCC rising	6.20	6.90	7.20	V
VCC under voltage lockout hysteresis	ΔUVLO	–	–	500	–	mV
Steady state external voltage that can be applied at the VCC pin[*2]	VCC(ext)	–	–	–	12	V
Reference						
REF pin voltage	V_{REF}	REF bypassed with a 0.1μF capacitor to GND; I_{REF}= 0; VCC = 7.75V; PWMD = GND	1.225	1.25	1.275	V
Line regulation of reference voltage	$V_{REFLINE}$	REF bypassed with a 0.1μF capacitor to GND; I_{REF} = 0; VCC = 7.25 – 12V; PWMD = GND	0	–	20	mV
Load regulation of reference voltage	$V_{REFLOAD}$	REF bypassed with a 0.1μF capacitor to GND; I_{REF} = 0-500μ; PWMD = GND	0	–	20	mV
PWM Dimming						
PWMD input low voltage	$V_{PWMD(lo)}$	VCC = 7.25V – 12V	–	–	0.80	V
PWMD input high voltage	$V_{PWMD(hi)}$	VCC = 7.25V – 12V	2.0	–	–	V
PWMD pull-down resistance	R_{PWMD}	V_{PWMD} = 5.0V	50	100	150	KΩ
Over Voltage Protection						
IC shut down voltage	V_{OVP}	VCC = 7.25 – 12V ; OVP rising	1.215	1.25	1.285	V

Notes:
1. See application section for minimum input voltage
2. Parameters are not guaranteed to be within specifications if the external VCC voltage is greater than VCC(ext) or if VCC < 7.25V.

Electrical Characteristics (Continued)

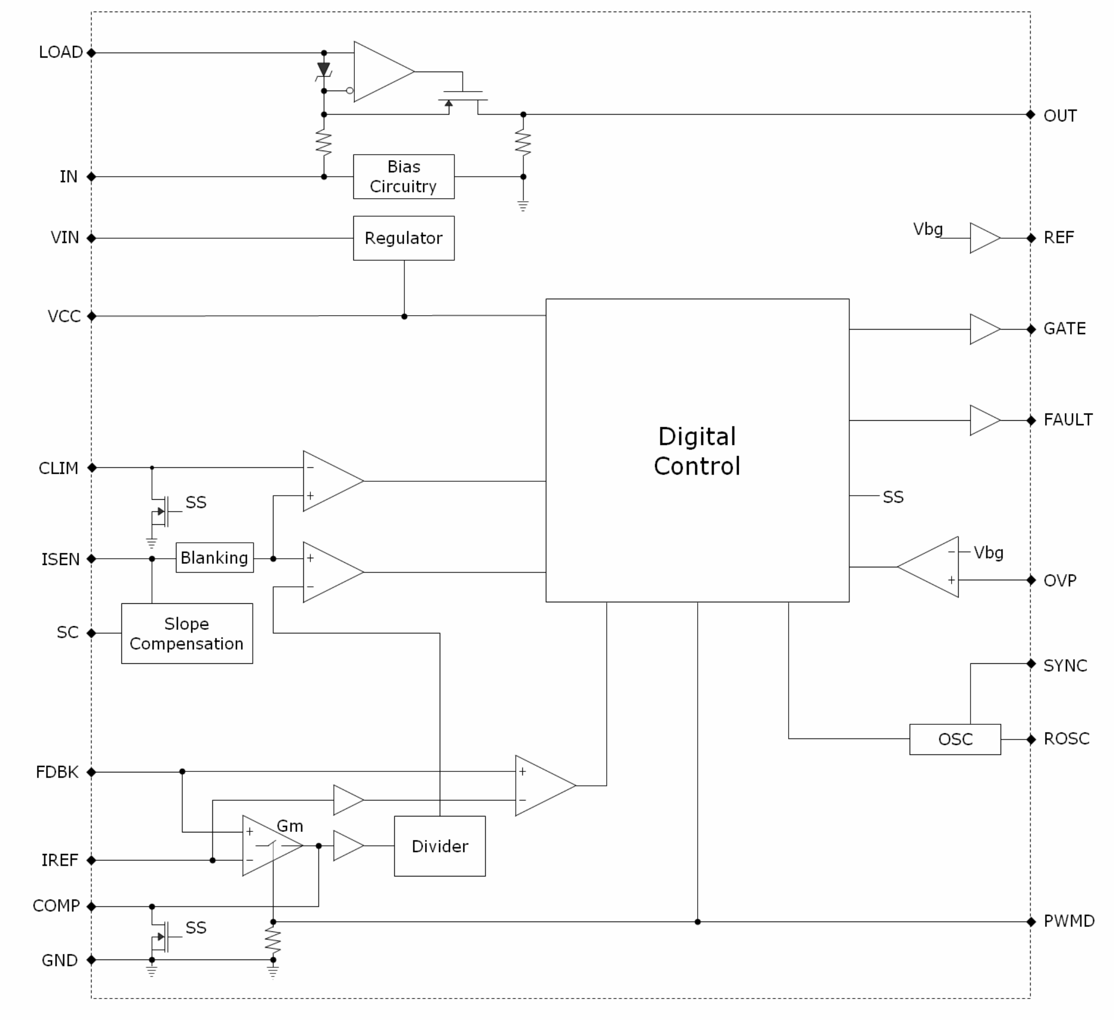
V_{IN}=24V, T_A=25°C unless specified, otherwise minimum and maximum values are guaranteed by production testing requirements.

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
GATE						
GATE short circuit current	I_{SOURCE}	V_{GATE} = 0V; VCC = 7.75V	0.2	–	–	A
GATE sinking current	I_{SINK}	V_{GATE} = 7.75V ; VCC = 7.75V	0.4	–	–	A
GATE output rise time	T_{RISE}	C_{GATE} = 1nF; VCC = 7.75V	–	50	100	ns
GATE output fall time	T_{FALL}	C_{GATE} = 1nF; VCC = 7.75V	–	25	100	ns
Current Sense						
Leading edge blanking	T_{BLANK}	–	100	–	500	ns
Delay to output of COMP comparator	T_{DELAY1}	COMP = VCC ; CLIM = REF; V_{ISEN} = 0 to 600mV step	–	–	300	ns
Delay to output of CLIMIT comparator	T_{DELAY2}	COMP = VCC ; CLIM = 300mV ; V_{ISEN} = 0 to 400mV step	–	–	300	ns
Comparator offset voltage	V_{OFFSET}	–	-20	–	20	mV
Oscillator						
Oscillator frequency	f_{OSC1}	R_{OSC} = 909KΩ	88	100	112	KHz
	f_{OSC2}	R_{OSC} = 261KΩ	308	350	392	
	f_{OSC3}	R_{OSC} = 2MΩ	40	45	50	
Maximum duty cycle	D_{MAX}	–	–	90	–	%
Sync output current	$I_{OUTSYNC}$	–	–	10	20	μA
Sync input current	I_{INSYNC}	VSYNC < 0.1V	0	–	200	μA
Output Short Circuit						
Propagation time for short circuit detection	T_{OFF}	I_{REF} = 200mV ; FDBK = 450mV; FAULT goes from high to low	–	–	500	ns
Fault output rise time	$T_{RISE,FAULT}$	1nF capacitor at FAULT pin	–	–	300	ns
Fault output fall time	$T_{FALL,FAULT}$	1nF capacitor at FAULT pin	–	–	200	ns
Amplifier gain at IREF pin	G_{FAULT}	I_{REF} = 200mV	1.8	2	2.2	–
Soft Start						
Current into CLIM pin when pulled low	I_{CLIM}	FAULT is low; 6.25KΩ between REF and CLIM	–	–	250	μA
Slope Compensation						
Current sourced out of SC pin	I_{SLOPE}	–	0	–	100	μA
Internal current mirror ratio	G_{SLOPE}	I_{SLOPE} = 50μA ; $RC_{SENENSE}$ = 1KΩ	1.8	2	2.2	–
Current Monitor						
Supply voltage range	V_{IN}	–	9.0	–	350	V
Quiescent supply current	I_Q	V_{IN}= 9~350V, V_{SENSE}= 0mV	–	–	100	μA
Output Resistance	R_{OUT}	–	–	3.6	–	KΩ
Output Voltage	V_{OUT}	V_{SENSE} =0mV	0	–	15	mV
		V_{SENSE} = 100mV	79	–	121	
		V_{SENSE} = 200mV	177	–	223	
		V_{SENSE} = 500mV	470	–	530	
Output rise time	t_{RISE}	V_{SENSE} step 5mV to 500mV, V_{IN}=24V	–	2.0	TBD	μS
		V_{SENSE} step 500mV to 0mV, V_{IN}=24V	–	2.0	TBD	
Output fall time	t_{FALL}	V_{SENSE} step 500mV to 0mV, V_{IN}=24V	–	2.0	TBD	μS

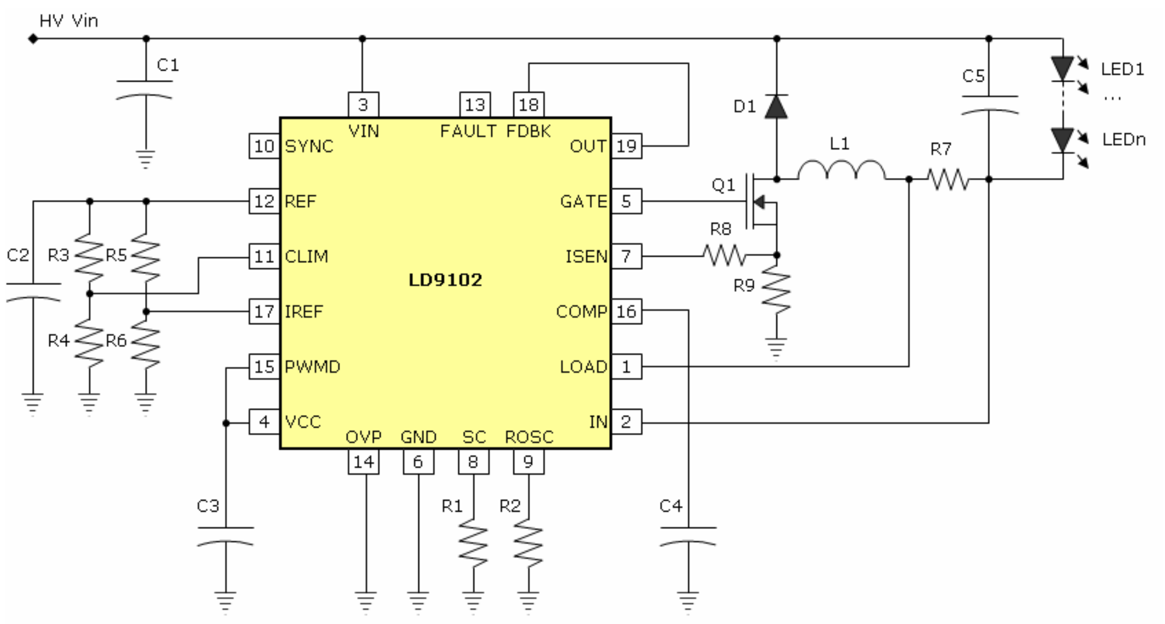
Pin Description

Pin #	Name	Description
1	LOAD	This pin is the negative side of current monitor.
2	IN	This pin is the positive side of current monitor.
3	VIN	This pin is the input of a 350V high voltage regulator.
4	VCC	This is a power supply pin for all internal circuits. It must be bypassed with a low ESR capacitor to GND (at least 0.1uF).
5	GATE	This pin is the output GATE driver for an external N-channel power MOSFET.
6	GND	Ground return for all circuits. This pin must be connected to the return path from the input.
7	ISEN	This pin is used to sense the drain current of the external power FET. It includes a built-in 100ns (min) blanking time.
8	SC	Slope compensation for current sense. A resistor between SC and GND will program the slope compensation. In case of constant off-time mode of operation, slope compensation is unnecessary and the pin can be left open.
9	ROSC	This pin sets the frequency or the off-time of the power circuit. A resistor between ROSC and GND will program the circuit in constant frequency mode. A resistor between ROSC and GATE will program the circuit in a constant off-time mode.
10	SYNC	This I/O pin may be connected to the SYNC pin of other LD9102 circuits and will cause the oscillators to lock to the highest frequency oscillator.
11	CLIM	This pin provides a programmable input current limit for the converter. The current limit can be set by using a resistor divider from the REF pin. Soft start can also be provided using this pin.
12	REF	This pin provides 2% accurate reference voltage. It must be bypassed with at least a 10nF - 0.22μF capacitor to GND.
13	FAULT	This pin is pulled to ground when there is an output short circuit condition or output over voltage condition. This pin can be used to drive an external MOSFET in the case of boost converters to disconnect the load from the source.
14	OVP	This pin provides the over voltage protection for the converter. When the voltage at this pin exceeds 1.25V, the GATE output of the LD9102 is turned off and FAULT goes low. The IC will turn on when the power is recycled.
15	PWMD	When this pin is pulled to GND (or left open), switching of the LD9102 is disabled. When an external TTL high level is applied to it, switching will resume.
16	COMP	Stable Closed loop control can be accomplished by connecting a compensation network between COMP and GND.
17	IREF	The voltage at this pin sets the output current level. The current reference can be set using a resistor divider from the REF pin.
18	FDBK	This pin provides output current feedback to the controller by using a current sense resistor.
19	OUT	This pin usually is connected to FDBK for providing current output feedback. There is a typical output resistance 3.6KΩ from this pin to the ground.
20	N.C.	No contact pin

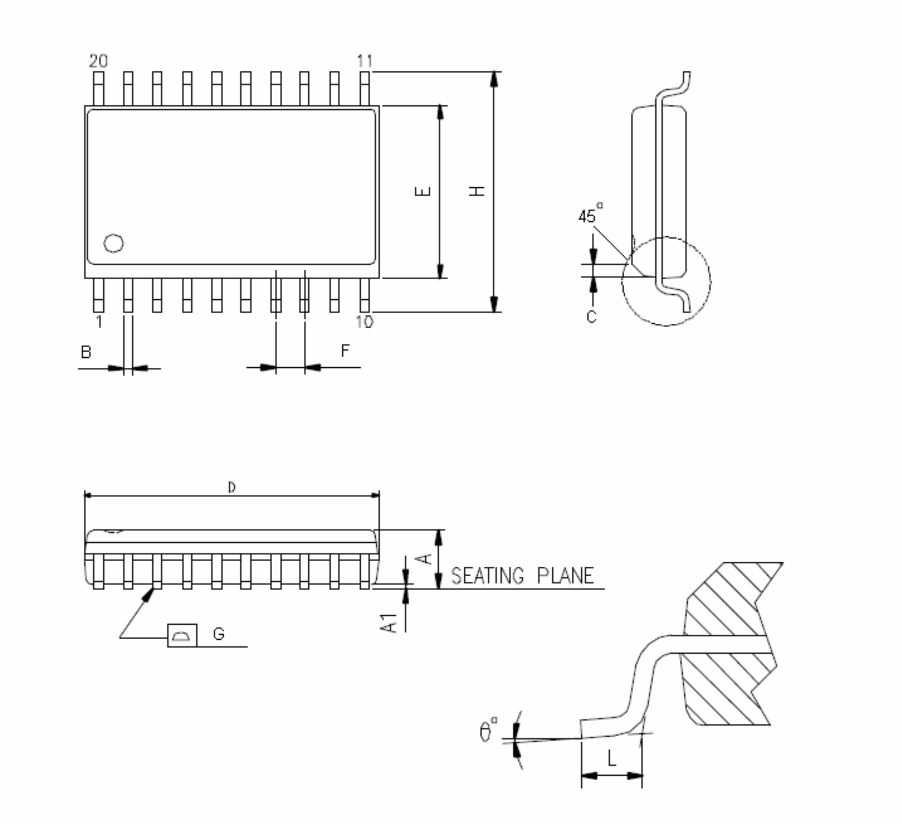
Functional Block Diagram



Typical Application Circuit



Package Outline
SOP-20:



Symbols	Dimensions in Millimeters			Dimensions in Inches		
	Minimum	Normal	Maximum	Minimum	Normal	Maximum
A	2.36	2.49	2.64	0.093	0.098	0.104
A1	0.10	-	0.30	0.004	-	0.012
B	0.33	0.41	0.51	0.013	0.016	0.020
C	-	0.51	-	-	0.020	-
D	12.60	12.80	12.90	0.496	0.504	0.508
E	7.39	7.49	7.59	0.291	0.295	0.299
F	-	1.27	-	-	0.050	-
G	-	-	0.10	-	-	0.004
H	10.01	10.31	10.64	0.394	0.406	0.419
L	0.38	0.81	1.27	0.015	0.032	0.050
Θ°	0°	-	8°	0°	-	8°